

USER GUIDE

UG525: Si34071 Isolated 24 V/2.2 A Output EVB

The Si34071 isolated Forward topology evaluation board is a reference design for a power supply in a Power over Ethernet (PoE) Powered Device (PD) application.

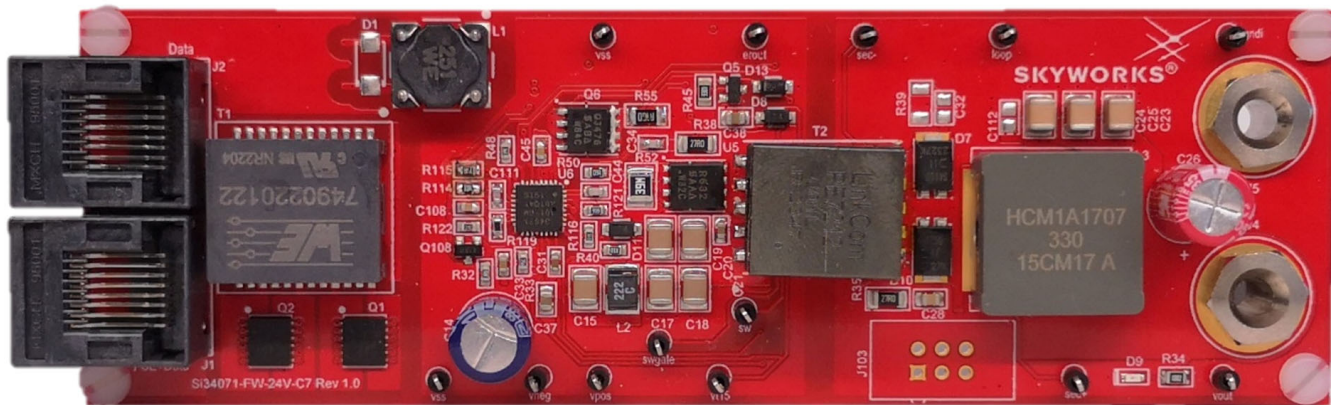
The Si34071-FW-24V-C7 board provides an isolated output of 24 V/2.2 A.

The Si34071-FW-24V-C7 board is shown below.

The Si34071 IC integrates an IEEE 802.3bt compatible PoE interface as well as a current-control-based dc/dc converter.

Key Features

- IEEE 802.3bt compliant
- Good EMI performance
- 89.7% efficiency
- High integration
- Simple 9600-baud UART interface
- Autoclass feature
- Low BOM cost
- Thermal shutdown protection
- 5x5 mm 32-pin QFN



Parameter	Condition	Specifications
Ordering part number	—	Si34071FW24V7KIT
PSE input voltage range	Connector J1	41.1 V to 57 V
PoE type/class	IEEE 802.3bt	Type 4 / Class 7
Output voltage/current	Connectors J4–J5	24 V / 2.2 A
Efficiency, end-to-end	$V_{IN} = 50\text{ V}$, 24 V output	89.7%
Switching frequency	$R33 = 95.3\text{ k}\Omega$	200 kHz
Radiated EMI test	EN 55032 Class B (30 MHz–1 GHz)	Passed (min. 12 dB margin)

1. Kit Description and Powering up the Si34071-FW-24V-C7 Board

The Si34071-FW-24V-C7 evaluation board is a low-cost, high-power, diode reset forward type PoE PD reference design. It provides IEEE 802.3bt interfacing and power supply control in a single chip solution with Si34071. The dc-dc converter utilizes diode reset demagnetization on the main power transformer and Schottky diode rectification at the secondary side saving BOM cost on the active clamp reset circuitry and synchronous rectification while achieving high conversion efficiency. Input FET bridges are used in order to further improve overall efficiency.

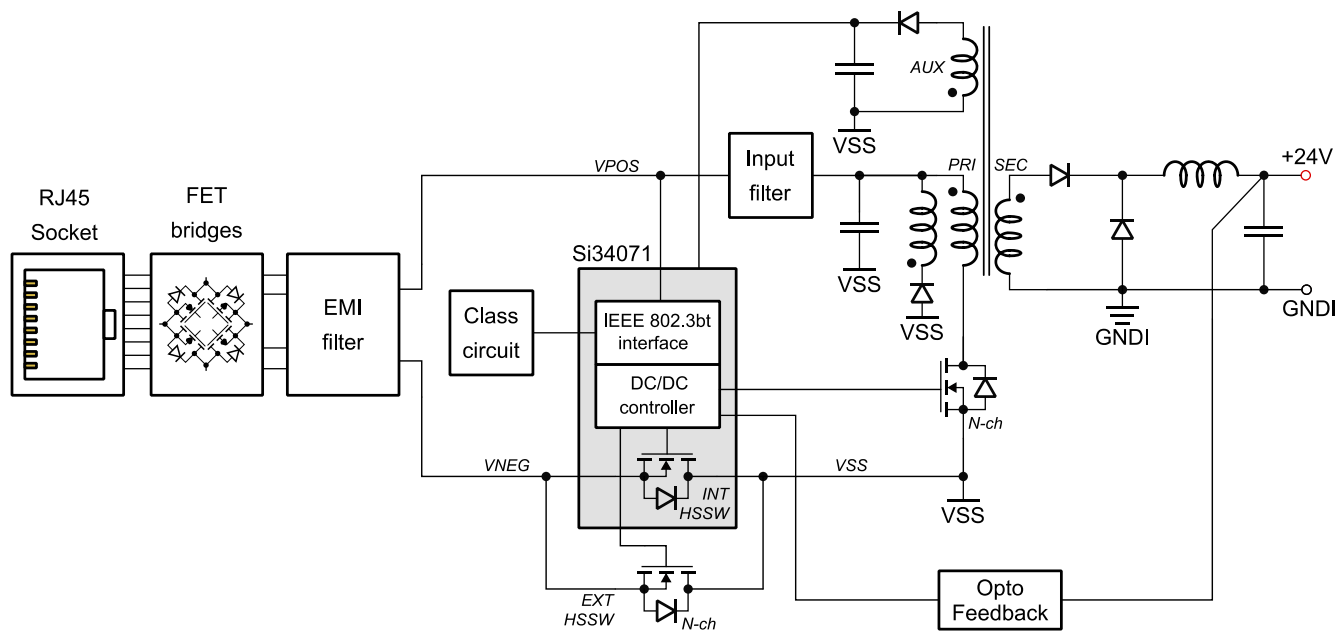


Figure 1. Simplified Block Diagram of the Si34071-FW-24V-C7

2. Schematics

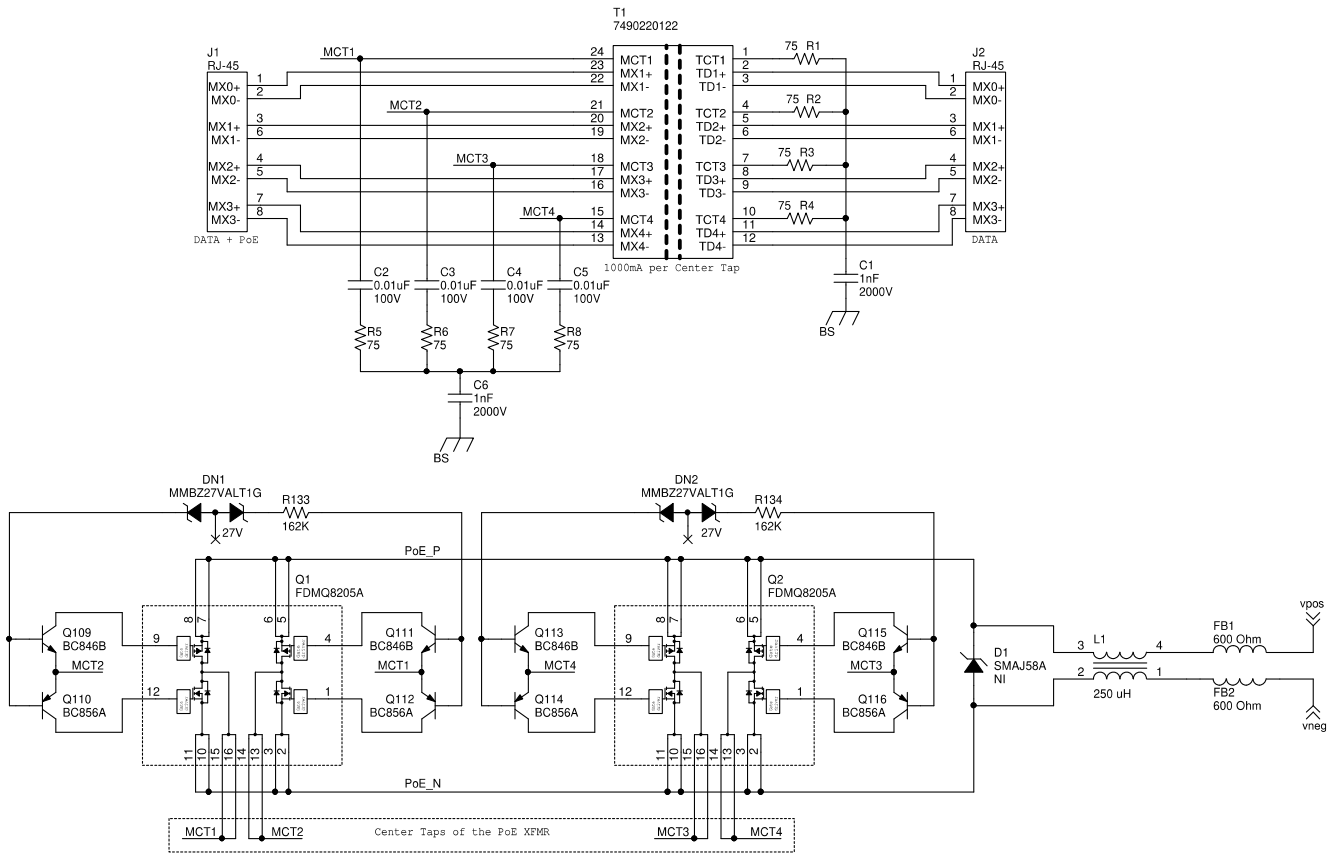


Figure 2. Si34071-FW-24V-C7 Schematic: Input Rectification

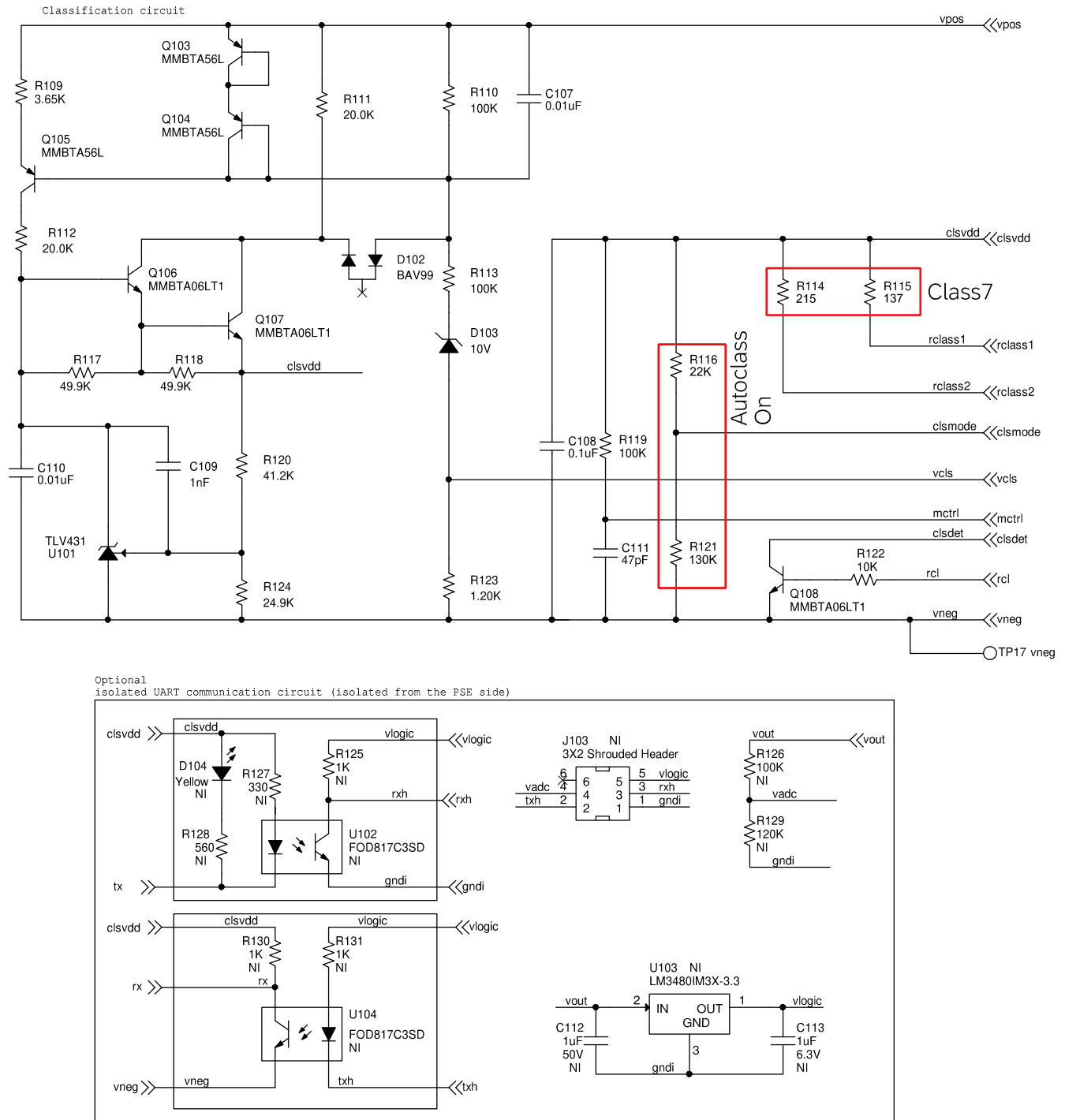


Figure 3. Si34071-FW-24V-C7 Schematic: Classification Circuit

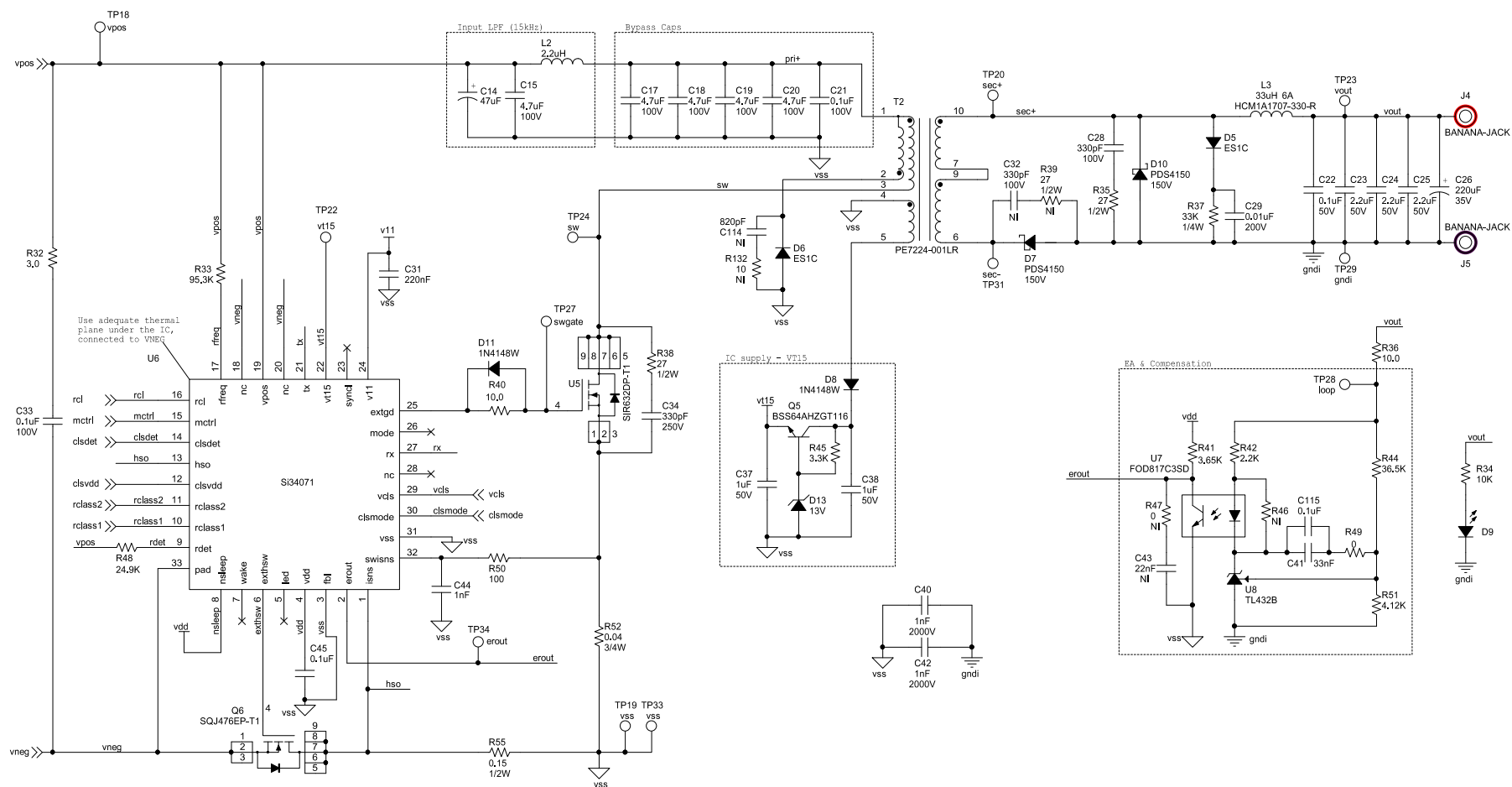


Figure 4. Si34071-FW-24V-C7 Schematic: DC-DC Converter

3. Getting Started: Powering Up the Si34071-FW-24V-C7 Board

Ethernet data and power are applied to the board through the PoE+Data RJ45 connector (J1). The board itself has no active Ethernet data transmission functionality, but, as a convenience, the Ethernet transformer secondary-side data is connected to the Data RJ45 connector (J2). The design can be used in Gigabit (10/100/1000) systems as well.

Power may be applied in the following ways:

- Using an IEEE 802.3bt-compliant (4 pair), PoE-capable PSE, or
- Using a laboratory power supply unit (PSU). The PSU connection is shown below:

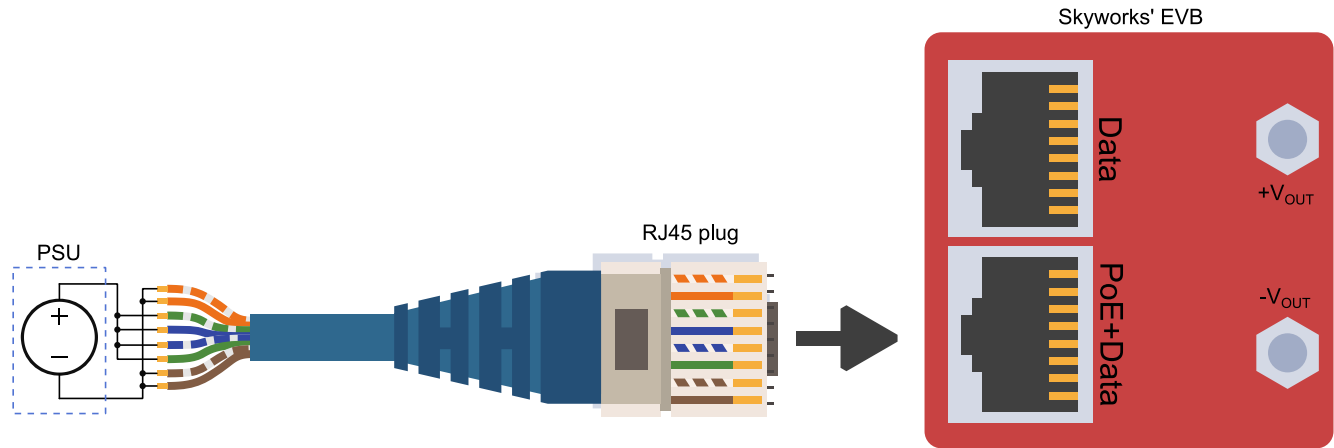


Figure 5. Four Pair Connection Using Laboratory Power Supply

Note: 4-pair connection is required for maximum power and highest conversion efficiency.

4. Conversion Efficiency of the Si34071-FW-24V-C7 Board

The end-to-end efficiency measurement data of the Si34071-FW-24V-C7 are shown below. Efficiency was measured from PoE (RJ45 connector) input to the 24 V output. The efficiency was measured at three different input voltage levels, 41.1 V, 50 V and 57 V.

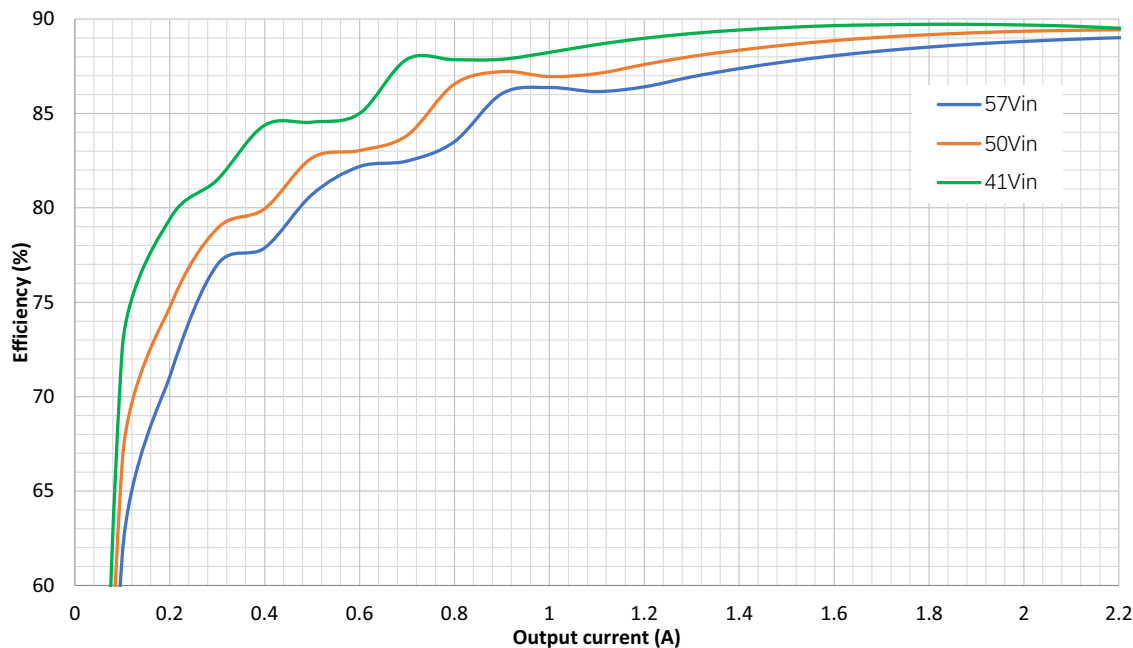


Figure 6. Si34071-FW-24V-C7 EVB End-to-End Conversion Efficiency Chart

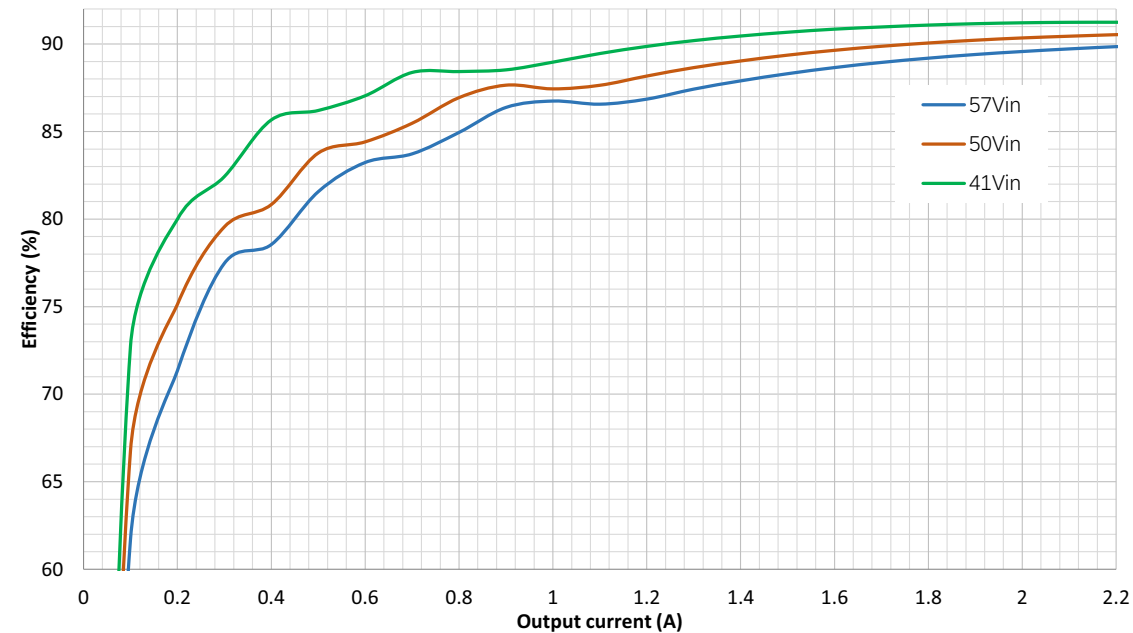


Figure 7. Si34071-FW-24V-C7 EVB DC-DC Efficiency Chart

5. Sifos® PoE Compatibility Test Results

The PDA-604A Powered Device Analyzer is a single-box comprehensive solution for testing IEEE 802.3at and IEEE 802.3bt PoE Powered Devices. Si34071-FW-24V-C7 EVB board has been successfully tested with the PDA-604A Powered Device Analyzer from SIFOS Technologies. [Table 1](#) shows the test results of the Sifos Technologies 802.3bt Conformance Test Suite Version 2.2.

Table 1. ALT A MDI ALT B MDI Test Results

Parameter	Cycle	1	Units	Min	Max	Average	Low Lim	High Lim	P/F
Detection								Det Cycles	3
SigType		SINGLE	—	—	—	—	SINGLE	SINGLE	P
Rdet_A		24.79	kΩ	24.79	24.79	24.79	23.7	26.3	P
Rdet_final_A		24.77	kΩ	24.77	24.77	24.77	23.7	26.3	P
Rdet_unpwr_A		>99.00	kΩ	99	99	99	<12.00	>45.00	P
Rdet_at_Vmin_A		24.81	kΩ	24.81	24.81	24.81	23.7	26.3	P
Rdet_at_Vmax_A		24.84	kΩ	24.84	24.84	24.84	23.7	26.3	P
Rdet_Voffset_A		1.2	VDC	1.2	1.2	1.2	0	1.9	P
Cdet_A		0.11	μF	0.11	0.11	0.11	0.05	0.12	P
Cdet_final_A		0.1	μF	0.1	0.1	0.1	0.05	0.12	P
Rdet_B		24.84	kΩ	24.84	24.84	24.84	23.7	26.3	P
Rdet_final_B		24.89	kΩ	24.89	24.89	24.89	23.7	26.3	P
Rdet_unpwr_B		>99.00	kΩ	99	99	99	<12.00	>45.00	P
Rdet_at_Vmin_B		25.02	kΩ	25.02	25.02	25.02	23.7	26.3	P
Rdet_at_Vmax_B		25.05	kΩ	25.05	25.05	25.05	23.7	26.3	P
Rdet_Voffset_B		1.2	VDC	1.2	1.2	1.2	0	1.9	P
Cdet_B		0.1	μF	0.1	0.1	0.1	0.05	0.12	P
Cdet_final_B		0.1	μF	0.1	0.1	0.1	0.05	0.12	P
Classification									
ClassNum_A		7		7	7	—	7	7	P
class_sig_EV1-2_min_A		41.7	mA	41.7	41.7	41.7	36.0	44.0	P
class_sig_EV1-2_max_A		42.4	mA	42.4	42.4	42.4	36.0	44.0	P
class_sig_EV3-5_min_A		19.8	mA	19.8	19.8	19.8	17.0	20.0	P
class_sig_EV3-5_max_A		20.0	mA	20.0	20.0	20.0	17.0	20.0	P
MarkI_A		2.33	mA	2.33	2.33	2.33	0.25	4.00	P
Tclass_max_A		3.4	ms	3.4	3.4	3.4	0.2	5.0	P
Iclass_EV1_at_Vmin_A		40.3	mA	40.3	40.3	40.3	36.0	44.0	P
Iclass_EV1_at_Vmax_A		40.7	mA	40.7	40.7	40.7	36.0	44.0	P
Class_Reset_A		1		1	1	—	1	1	P
Autoclass		1		1	1	—	1	1	P

Table 1. ALT A MDI ALT B MDI Test Results (Continued)

Parameter	Cycle	1	Units	Min	Max	Average	Low Lim	High Lim	P/F
Tacs		84.0	ms	84.0	84.0	84.0	75.5	87.5	P
ClassNum_B		7		7	7	—	7	7	P
class_sig_EV1-2_min_B		41.8	mA	41.8	41.8	41.8	36.0	44.0	P
class_sig_EV1-2_max_B		42.2	mA	42.2	42.2	42.2	36.0	44.0	P
class_sig_EV3-5_min_B		19.8	mA	19.8	19.8	19.8	17.0	20.0	P
class_sig_EV3-5_max_B		20.0	mA	20.0	20.0	20.0	17.0	20.0	P
MarkI_B		2.40	mA	2.40	2.40	2.40	0.25	4.00	P
Tclass_max_B		3.4	ms	3.4	3.4	3.4	0.2	5.0	P
Iclass_EV1_at_Vmin_B		40.8	mA	40.8	40.8	40.8	36.0	44.0	P
Iclass_EV1_at_Vmax_B		40.6	mA	40.6	40.6	40.6	36.0	44.0	P
Class_Reset_B		1		1	1	—	1	1	P
Power-Up / Down									
linrush_init		172.3	mA	172.3	172.3	172.3	0.0	800.0	INFO
linrush_tdel		176.300	mA	176.3	176.3	176.3	0.0	257.4	P
Tinrush		50.0	ms	50.0	50.0	50.0	0.0	50.0	P
linrush_init_A		83.9	mA	83.9	83.9	83.9	0.0	600.0	INFO
linrush_tdel_A		93.500	mA	93.5	93.5	93.5	0.0	257.4	P
Tinrush_A		50.0	ms	50.0	50.0	50.0	0.0	50.0	P
linrush_init_B		88.8	mA	88.8	88.8	88.8	0.0	600.0	INFO
linrush_tdel_B		82.800	mA	82.8	82.8	82.8	0.0	257.4	P
Tinrush_B		50.0	ms	50.0	50.0	50.0	0.0	50.0	P
Vrefl_A		1.2	VDC	1.2	1.2	1.2	0.0	2.8	P
Vrefl_B		1.1	VDC	1.1	1.1	1.1	0.0	2.8	P
Von		36.3	VDC	36.3	36.3	36.3	30.0	42.0	P
Voff		32.6	VDC	32.6	32.6	32.6	30.0	42.0	P
Vhyst		3.7	VDC	3.7	3.7	3.7	2.8	12.0	INFO

Table 1. ALT A MDI ALT B MDI Test Results (Continued)

Parameter	Cycle	1	Units	Min	Max	Average	Low Lim	High Lim	P/F
2 Pair Powered Type-1 PHY		PSE Emulation		On Time	30 s	Off Time	10 s	Vport	56.0
2 Pair Powered Type-3 PHY		PSE Emulation		On Time	30 s	Off Time	10 s	Vport	44.2
4 Pair Powered Type-3 PHY		PSE Emulation		On Time	-1 s	Off Time	10 s	Vport	-1.0
4 Pair Powered Type-4 PHY		PSE Emulation		On Time	60 s	Off Time	10 s	Vport	44.2
MinI_4		8.9	mA	8.9	8.9	8.90	0.0	1476.0	P
Vport-2P_4_A		44.0	VDC	44.0	44.0	44.0	42.9	57.0	INFO
Vport-2P_4_B		43.9	VDC	43.9	43.9	43.9	42.9	57.0	INFO
Ppeak_4		8.74	W	8.74	8.74	8.74	0.0	65.1	P
Pport_4		3.71	W	3.71	3.71	3.71	0.0	62.0	P
PeakViolation_4		0		0	0	—	0	0	P
MPSViolation_4		0		0	0	—	0	0	P
TcutWindowViolation_4		0		0	0	—	0	0	P
DutyCycleViolation_4		0		0	0	—	0	0	P

Table 2. ALT A MDI-X ALT B MDI Test Results

Parameter	Cycle	1	Units	Min	Max	Average	Low Lim	High Lim	P/F
Detection								Det Cycles	3
SigType		24.86	k Ω	24.86	24.86	24.86	23.70	26.30	P
Rdet_A		24.79	k Ω	24.79	24.79	24.79	23.70	26.30	P
Rdet_final_A		>99.00	k Ω	99.00	99.00	99.00	<12.00	>45.00	P
Rdet_unpwr_A		24.91	k Ω	24.91	24.91	24.91	23.70	26.30	P
Rdet_at_Vmin_A		24.86	k Ω	24.86	24.86	24.86	23.70	26.30	P
Rdet_at_Vmax_A		1.2	VDC	1.2	1.2	1.2	0.0	1.9	P
Rdet_Voffset_A		0.11	μ F	0.11	0.11	0.11	0.05	0.12	P
Cdet_A		0.10	μ F	0.10	0.10	0.10	0.05	0.12	P
Cdet_final_A		24.86	k Ω	24.86	24.86	24.86	23.70	26.30	P
Rdet_B		24.82	k Ω	24.82	24.82	24.82	23.70	26.30	P
Rdet_final_B		>99.00	k Ω	99.00	99.00	99.00	<12.00	>45.00	P
Rdet_unpwr_B		25.12	k Ω	25.12	25.12	25.12	23.70	26.30	P
Rdet_at_Vmin_B		25.15	k Ω	25.15	25.15	25.15	23.70	26.30	P
Rdet_at_Vmax_B		1.2	VDC	1.2	1.2	1.2	0.0	1.9	P
Rdet_Voffset_B		0.10	μ F	0.10	0.10	0.10	0.05	0.12	P
Cdet_B		0.10	μ F	0.10	0.10	0.10	0.05	0.12	P
Classification									
ClassNum_A		7		7	7	—	7	7	P
class_sig_EV1-2_min_A		41.7	mA	41.7	41.7	41.7	36.0	44.0	P
class_sig_EV1-2_max_A		42.2	mA	42.2	42.2	42.2	36.0	44.0	P
class_sig_EV3-5_min_A		19.8	mA	19.8	19.8	19.8	17.0	20.0	P
class_sig_EV3-5_max_A		20.0	mA	20.0	20.0	20.0	17.0	20.0	P
MarkI_A		2.34	mA	2.34	2.34	2.34	0.25	4.00	P
Tclass_max_A		3.4	ms	3.4	3.4	3.4	0.2	5.0	P
Iclass_EV1_at_Vmin_A		40.9	mA	40.9	40.9	40.9	36.0	44.0	P
Iclass_EV1_at_Vmax_A		40.8	mA	40.8	40.8	40.8	36.0	44.0	P
Class_Reset_A		1		1	1	—	1	1	P
Autoclass		1		1	1	—	1	1	P
Tacs		84.0	ms	84.0	84.0	84.0	75.5	87.5	P
ClassNum_B		7		7	7	—	7	7	P
class_sig_EV1-2_min_B		41.7	mA	41.7	41.7	41.7	36.0	44.0	P
class_sig_EV1-2_max_B		42.2	mA	42.2	42.2	42.2	36.0	44.0	P
class_sig_EV3-5_min_B		19.8	mA	19.8	19.8	19.8	17.0	20.0	P
class_sig_EV3-5_max_B		20.0	mA	20.0	20.0	20.0	17.0	20.0	P

Table 2. ALT A MDI-X ALT B MDI Test Results (Continued)

Parameter	Cycle	1	Units	Min	Max	Average	Low Lim	High Lim	P/F
MarkI_B		2.40	mA	2.40	2.40	2.40	0.25	4.00	P
Tclass_max_B		3.4	ms	3.4	3.4	3.4	0.2	5.0	P
Iclass_EV1_at_Vmin_B		41.1	mA	41.1	41.1	41.1	36.0	44.0	P
Iclass_EV1_at_Vmax_B		40.9	mA	40.9	40.9	40.9	36.0	44.0	P
Class_Reset_B		1		1	1	—	1	1	P
Power-Up / Down									
linrush_init		171.9	mA	171.9	171.9	171.9	0.0	800.0	INFO
linrush_tdel		101.400	mA	101.4	101.4	101.4	0.0	256.6	P
Tinrush		50.0	ms	50.0	50.0	50.0	0.0	50.0	P
linrush_init_A		83.5	mA	83.5	83.5	83.5	0.0	600.0	INFO
linrush_tdel_A		76.200	mA	76.2	76.2	76.2	0.0	256.6	P
Tinrush_A		50.0	ms	50.0	50.0	50.0	0.0	50.0	P
linrush_init_B		88.4	mA	88.4	88.4	88.4	0.0	600.0	INFO
linrush_tdel_B		82.800	mA	82.8	82.8	82.8	0.0	256.6	P
Tinrush_B		50.0	ms	50.0	50.0	50.0	0.0	50.0	P
Vrefl_A		1.2	VDC	1.2	1.2	1.2	0.0	2.8	P
Vrefl_B		1.1	VDC	1.1	1.1	1.1	0.0	2.8	P
Von		36.3	VDC	36.3	36.3	36.3	30.0	42.0	P
Voff		32.5	VDC	32.5	32.5	32.5	30.0	42.0	P
Vhyst		3.8	VDC	3.8	3.8	3.8	2.8	12.0	INFO
2 Pair Powered Type-1 PHY		PSE Emulation		On Time	30 s	Off Time	10 s	Vport	56.0
2 Pair Powered Type-3 PHY		PSE Emulation		On Time	30 s	Off Time	10 s	Vport	44.2
4 Pair Powered Type-3 PHY		PSE Emulation		On Time	–1 s	Off Time	10 s	Vport	–1.0
4 Pair Powered Type-4 PHY		PSE Emulation		On Time	60 s	Off Time	10 s	Vport	44.2
MinI_4		8.9	mA	8.9	8.9	8.9	0.0	1473.0	P
Vport-2P_4_A		44.1	VDC	44.1	44.1	44.1	42.9	57.0	INFO
Vport-2P_4_B		44.0	VDC	44.0	44.0	44.0	42.9	57.0	INFO
Ppeak_4		8.01	W	8.01	8.01	8.01	0.0	65.1	P
Pport_4		3.71	W	3.71	3.71	3.71	0.0	62.0	P
PeakViolation_4		0		0	0	—	0	0	P
MPSViolation_4		0		0	0	—	0	0	P
TcutWindowViolation_4		0		0	0	—	0	0	P
DutyCycleViolation_4		0		0	0	—	0	0	P

Table 3. ALT A MDI ALT B MDI-X Test Results

Parameter	Cycle	1	Units	Min	Max	Average	Low Lim	High Lim	P/F
Detection								Det Cycles	3
SigType		SINGLE	—	—	—	—	SINGLE	SINGLE	P
Rdet_A		24.81	kΩ	24.81	24.81	24.81	23.70	26.30	P
Rdet_final_A		24.86	kΩ	24.86	24.86	24.86	23.70	26.30	P
Rdet_unpwr_A		>99.00	kΩ	99.00	99.00	99.00	<12.00	>45.00	P
Rdet_at_Vmin_A		24.95	kΩ	24.95	24.95	24.95	23.70	26.30	P
Rdet_at_Vmax_A		24.93	kΩ	24.93	24.93	24.93	23.70	26.30	P
Rdet_Voffset_A		1.2	VDC	1.2	1.2	1.2	0.0	1.9	P
Cdet_A		0.10	μF	0.10	0.10	0.10	0.05	0.12	P
Cdet_final_A		0.11	μF	0.11	0.11	0.11	0.05	0.12	P
Rdet_B		24.77	kΩ	24.77	24.77	24.77	23.70	26.30	P
Rdet_final_B		24.86	kΩ	24.86	24.86	24.86	23.70	26.30	P
Rdet_unpwr_B		>99.00	kΩ	99.00	99.00	99.00	<12.00	>45.00	P
Rdet_at_Vmin_B		25.04	kΩ	25.04	25.04	25.04	23.70	26.30	P
Rdet_at_Vmax_B		25.07	kΩ	25.07	25.07	25.07	23.70	26.30	P
Rdet_Voffset_B		1.2	VDC	1.2	1.2	1.2	0.0	1.9	P
Cdet_B		0.10	μF	0.10	0.10	0.10	0.05	0.12	P
Cdet_final_B		0.10	μF	0.10	0.10	0.10	0.05	0.12	P
Classification									
ClassNum_A		7		7	7	—	7	7	P
class_sig_EV1-2_min_A		41.7	mA	41.7	41.7	41.7	36.0	44.0	P
class_sig_EV1-2_max_A		42.2	mA	42.2	42.2	42.2	36.0	44.0	P
class_sig_EV3-5_min_A		19.9	mA	19.9	19.9	19.9	17.0	20.0	P
class_sig_EV3-5_max_A		20.0	mA	20.0	20.0	20.0	17.0	20.0	P
MarkI_A		2.33	mA	2.33	2.33	2.33	0.25	4.00	P
Tclass_max_A		3.4	ms	3.4	3.4	3.4	0.2	5.0	P
Iclass_EV1_at_Vmin_A		40.8	mA	40.8	40.8	40.8	36.0	44.0	P
Iclass_EV1_at_Vmax_A		40.8	mA	40.8	40.8	40.8	36.0	44.0	P
Class_Reset_A		1		1	1	—	1	1	P
Autoclass		1		1	1	—	1	1	P
Tacs		84.0	ms	84.0	84.0	84.0	75.5	87.5	P
ClassNum_B		7		7	7	—	7	7	P
class_sig_EV1-2_min_B		41.7	mA	41.7	41.7	41.7	36.0	44.0	P
class_sig_EV1-2_max_B		42.2	mA	42.2	42.2	42.2	36.0	44.0	P
class_sig_EV3-5_min_B		19.8	mA	19.8	19.8	19.8	17.0	20.0	P

Table 3. ALT A MDI ALT B MDI-X Test Results (Continued)

Parameter	Cycle	1	Units	Min	Max	Average	Low Lim	High Lim	P/F
class_sig_EV3-5_min_B		19.8	mA	19.8	19.8	19.8	17.0	20.0	P
class_sig_EV3-5_max_B		20.0	mA	20.0	20.0	20.0	17.0	20.0	P
MarkI_B		2.40	mA	2.40	2.40	2.40	0.25	4.00	P
Tclass_max_B		3.4	ms	3.4	3.4	3.4	0.2	5.0	P
Iclass_EV1_at_Vmin_B		40.8	mA	40.8	40.8	40.8	36.0	44.0	P
Iclass_EV1_at_Vmax_B		40.8	mA	40.8	40.8	40.8	36.0	44.0	P
Class_Reset_B		1		1	1	—	1	1	P
Power-Up / Down									
linrush_init		171.5	mA	171.5	171.5	171.5	0.0	800.0	INFO
linrush_tdel		97.000	mA	97.0	97.0	97.0	0.0	256.9	P
Tinrush		50.0	ms	50.0	50.0	50.0	0.0	50.0	P
linrush_init_A		82.7	mA	82.7	82.7	82.7	0.0	600.0	INFO
linrush_tdel_A		75.800	mA	75.8	75.8	75.8	0.0	256.9	P
Tinrush_A		50.0	ms	50.0	50.0	50.0	0.0	50.0	P
linrush_init_B		88.8	mA	88.8	88.8	88.8	0.0	600.0	INFO
linrush_tdel_B		83.200	mA	83.2	83.2	83.2	0.0	256.9	P
Tinrush_B		50.0	ms	50.0	50.0	50.0	0.0	50.0	P
Vrefl_A		1.2	VDC	1.2	1.2	1.2	0.0	2.8	P
Vrefl_B		1.1	VDC	1.1	1.1	1.1	0.0	2.8	P
Von		36.4	VDC	36.4	36.4	36.4	30.0	42.0	P
Voff		32.6	VDC	32.6	32.6	32.6	30.0	42.0	P
Vhyst		3.8	VDC	3.8	3.8	3.8	2.8	12.0	INFO
2 Pair Powered Type-1 PHY		PSE Emulation		On Time	30 s	Off Time	10 s	Vport	56.0
2 Pair Powered Type-3 PHY		PSE Emulation		On Time	30 s	Off Time	10 s	Vport	44.2
4 Pair Powered Type-3 PHY		PSE Emulation		On Time	–1 s	Off Time	10 s	Vport	–1.0
4 Pair Powered Type-4 PHY		PSE Emulation		On Time	60 s	Off Time	10 s	Vport	44.2
MinI_4		9.0	mA	9.0	9.0	9.0	0.0	1472.9	P
Vport-2P_4_A		44.1	VDC	44.1	44.1	44.1	42.9	57.0	INFO
Vport-2P_4_B		44.0	VDC	44.0	44.0	44.0	42.9	57.0	INFO
Ppeak_4		7.96	W	7.96	7.96	7.96	0.0	65.1	P
Pport_4		3.71	W	3.71	3.71	3.71	0.0	62.0	P
PeakViolation_4		0		0	0	—	0	0	P
MPSViolation_4		0		0	0	—	0	0	P
TcutWindowViolation_4		0		0	0	—	0	0	P
DutyCycleViolation_4		0		0	0	—	0	0	P

Table 4. ALT A MDI-X ALT B MDI-X Test Results

Parameter	Cycle	1	Units	Min	Max	Average	Low Lim	High Lim	P/F
Detection								Det Cycles	3
SigType		SINGLE	—	—	—	—	SINGLE	SINGLE	P
Rdet_A		24.84	kΩ	24.84	24.84	24.84	23.70	26.30	P
Rdet_final_A		24.74	kΩ	24.74	24.74	24.74	23.70	26.30	P
Rdet_unpwr_A		>99.00	kΩ	99.00	99.00	99.00	<12.00	>45.00	P
Rdet_at_Vmin_A		24.99	kΩ	24.99	24.99	24.99	23.70	26.30	P
Rdet_at_Vmax_A		24.90	kΩ	24.90	24.90	24.90	23.70	26.30	P
Rdet_Voffset_A		1.2	VDC	1.2	1.2	1.2	0.0	1.9	P
Cdet_A		0.11	μF	0.11	0.11	0.11	0.05	0.12	P
Cdet_final_A		0.10	μF	0.10	0.10	0.10	0.05	0.12	P
Rdet_B		24.77	kΩ	24.77	24.77	24.77	23.70	26.30	P
Rdet_final_B		24.82	kΩ	24.82	24.82	24.82	23.70	26.30	P
Rdet_unpwr_B		>99.00	kΩ	99.00	99.00	99.00	<12.00	>45.00	P
Rdet_at_Vmin_B		25.12	kΩ	25.12	25.12	25.12	23.70	26.30	P
Rdet_at_Vmax_B		25.07	kΩ	25.07	25.07	25.07	23.70	26.30	P
Rdet_Voffset_B		1.2	VDC	1.2	1.2	1.2	0.0	1.9	P
Cdet_B		0.11	μF	0.11	0.11	0.11	0.05	0.12	P
Cdet_final_B		0.10	μF	0.10	0.10	0.10	0.05	0.12	P
Classification									
ClassNum_A		7		7	7	—	7	7	P
class_sig_EV1-2_min_A		41.7	mA	41.7	41.7	41.7	36.0	44.0	P
class_sig_EV1-2_max_A		42.2	mA	42.2	42.2	42.2	36.0	44.0	P
class_sig_EV3-5_min_A		19.9	mA	19.9	19.9	19.9	17.0	20.0	P
class_sig_EV3-5_max_A		20.0	mA	20.0	20.0	20.0	17.0	20.0	P
MarkI_A		2.33	mA	2.33	2.33	2.33	0.25	4.00	P
Tclass_max_A		3.4	ms	3.4	3.4	3.4	0.2	5.0	P
lclass_EV1_at_Vmin_A		41.0	mA	41.0	41.0	41.0	36.0	44.0	P
lclass_EV1_at_Vmax_A		40.8	mA	40.8	40.8	40.8	36.0	44.0	P
Class_Reset_A		1		1	1	—	1	1	P
Autoclass		1		1	1	—	1	1	P
Tacs		84.0	ms	84.0	84.0	84.0	75.5	87.5	P
ClassNum_B		7		7	7	—	7	7	P
class_sig_EV1-2_min_B		41.8	mA	41.8	41.8	41.8	36.0	44.0	P
class_sig_EV1-2_max_B		42.2	mA	42.2	42.2	42.2	36.0	44.0	P
class_sig_EV3-5_min_B		19.9	mA	19.9	19.9	19.9	17.0	20.0	P

Table 4. ALT A MDI-X ALT B MDI-X Test Results (Continued)

Parameter	Cycle	1	Units	Min	Max	Average	Low Lim	High Lim	P/F
class_sig_EV3-5_max_B		20.0	mA	20.0	20.0	20.0	17.0	20.0	P
MarkI_B		2.40	mA	2.40	2.40	2.40	0.25	4.00	P
Tclass_max_B		3.4	ms	3.4	3.4	3.4	0.2	5.0	P
Iclass_EV1_at_Vmin_B		40.8	mA	40.8	40.8	40.8	36.0	44.0	P
Iclass_EV1_at_Vmax_B		40.8	mA	40.8	40.8	40.8	36.0	44.0	P
Class_Reset_B		1		1	1	—	1	1	P
Power-Up / Down									
linrush_init		171.2	mA	171.2	171.2	171.2	0.0	800.0	INFO
linrush_tdel		50.800	mA	50.8	50.8	50.8	0.0	256.7	P
Tinrush		50.0	ms	50.0	50.0	50.0	0.0	50.0	P
linrush_init_A		83.9	mA	83.9	83.9	83.9	0.0	600.0	INFO
linrush_tdel_A		40.900	mA	40.9	40.9	40.9	0.0	256.7	P
Tinrush_A		50.0	ms	50.0	50.0	50.0	0.0	50.0	P
linrush_init_B		87.3	mA	87.3	87.3	87.3	0.0	600.0	INFO
linrush_tdel_B		77.900	mA	77.9	77.9	77.9	0.0	256.7	P
Tinrush_B		50.0	ms	50.0	50.0	50.0	0.0	50.0	P
Vrefl_A		1.2	VDC	1.2	1.2	1.2	0.0	2.8	P
Vrefl_B		1.1	VDC	1.1	1.1	1.1	0.0	2.8	P
Von		36.3	VDC	36.3	36.3	36.3	30.0	42.0	P
Voff		32.5	VDC	32.5	32.5	32.5	30.0	42.0	P
Vhyst		3.8	VDC	3.8	3.8	3.8	2.8	12.0	INFO
2 Pair Powered Type-1 PHY		PSE Emulation		On Time	30 s	Off Time	10 s	Vport	56.0
2 Pair Powered Type-3 PHY		PSE Emulation		On Time	30 s	Off Time	10 s	Vport	44.2
4 Pair Powered Type-3 PHY		PSE Emulation		On Time	–1 s	Off Time	10 s	Vport	–1.0
4 Pair Powered Type-4 PHY		PSE Emulation		On Time	60 s	Off Time	10 s	Vport	44.2
MinI_4		8.6	mA	8.6	8.6	8.6	0.0	1472.9	P
Vport-2P_4_A		44.0	VDC	44.0	44.0	44.0	42.9	57.0	INFO
Vport-2P_4_B		44.1	VDC	44.1	44.1	44.1	42.9	57.0	INFO
Ppeak_4		7.94	W	7.94	7.94	7.94	0.0	65.1	P
Pport_4		3.71	W	3.71	3.71	3.71	0.0	62.0	P
PeakViolation_4		0		0	0	—	0	0	P
MPSViolation_4		0		0	0	—	0	0	P
TcutWindowViolation_4		0		0	0	—	0	0	P
DutyCycleViolation_4		0		0	0	—	0	0	P

6. Feedback Loop Phase and Gain Measurement Results (Bode Plots)

The Si34071 device integrates a current mode-controlled switching mode power supply controller circuit. Therefore, the application is a closed-loop system. To guarantee a stable output voltage of a power supply and to reduce the influence of input supply voltage variations and load changes on the output voltage, the feedback loop should be stable. To verify the stability of the loop, the complex loop gain has been measured.

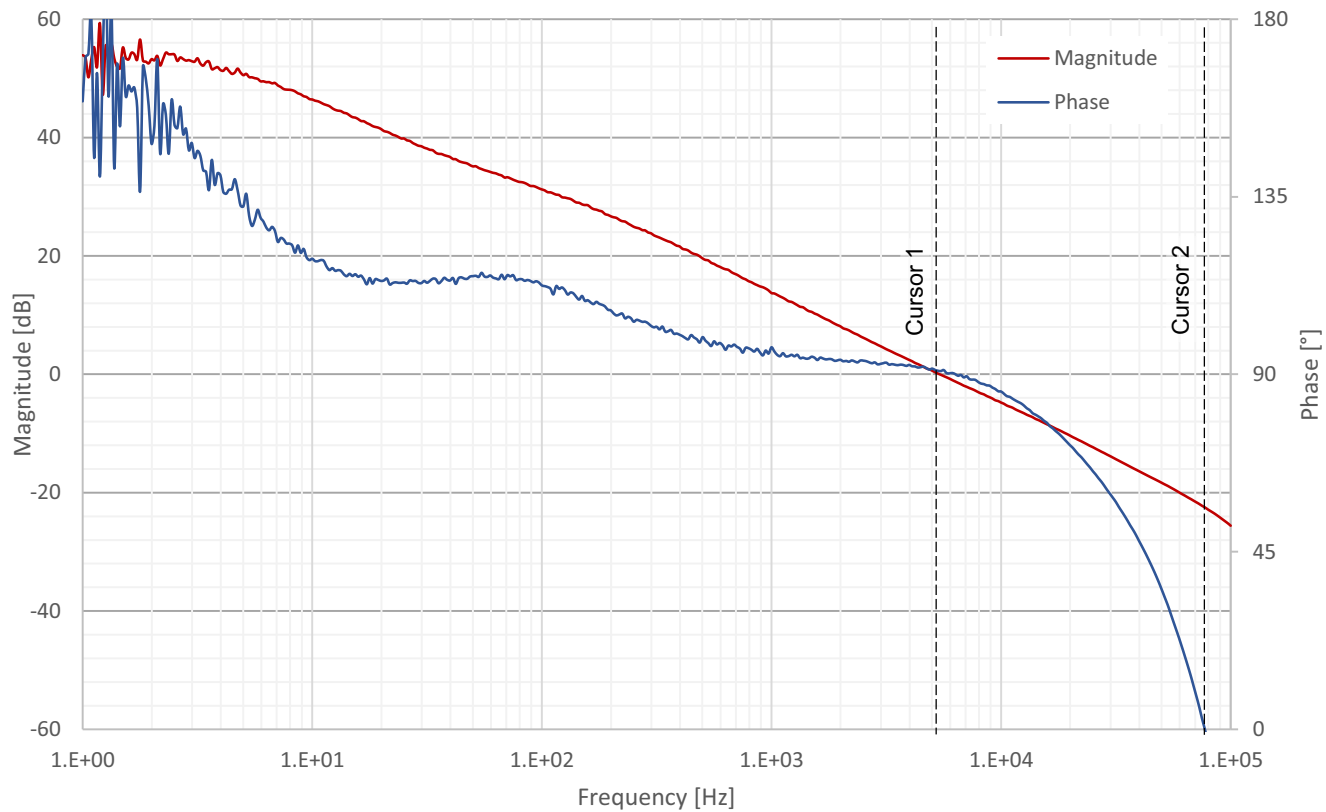


Figure 8. Si34071-FW-24V-C7 EVB Measured Loop-Gain at 12 Ω Load

	Frequency	Gain	Phase
Cursor 1 (Phase Margin)	5.4 kHz	0 dB	90°
Cursor 2 (Gain Margin)	77.2 kHz	-22.5 dB	0°

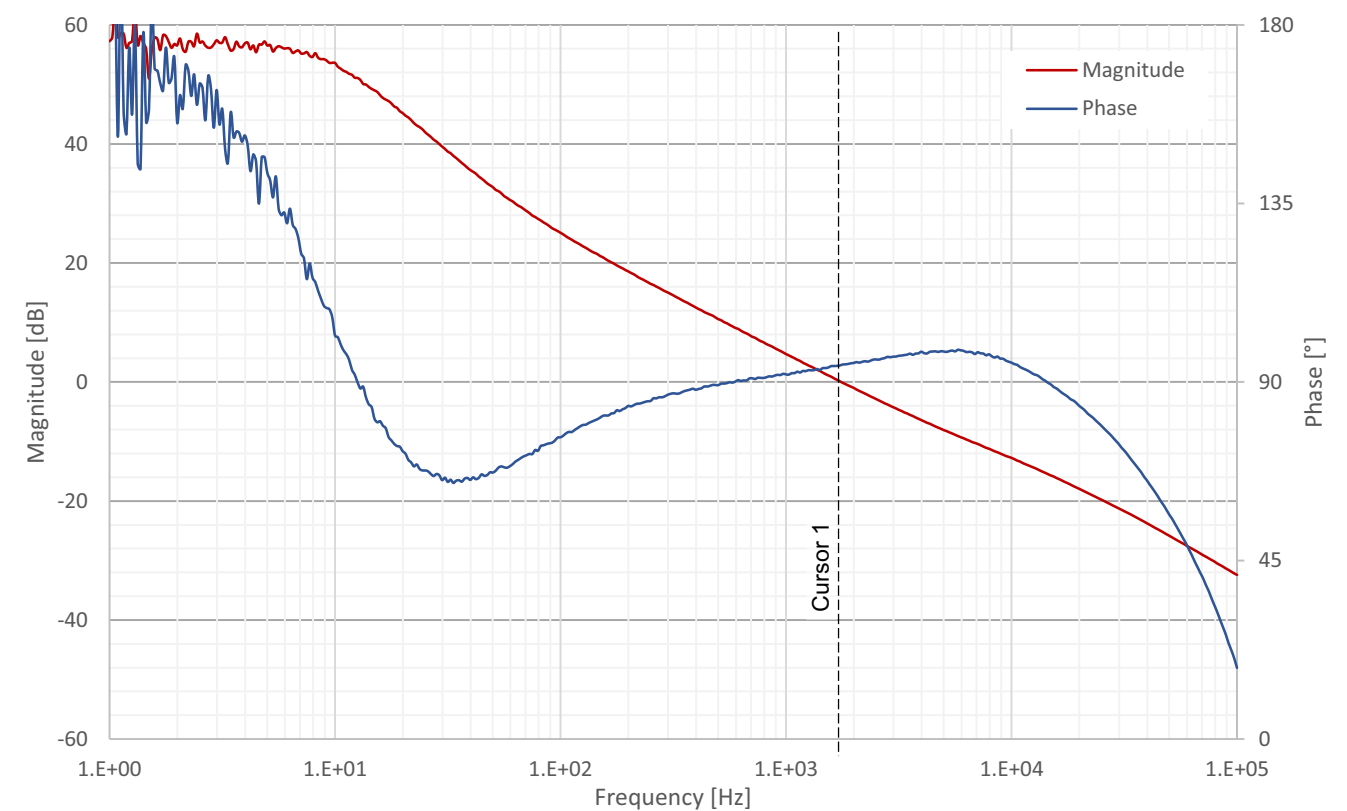


Figure 9. Si34071-FW-24V-C7 EVB Measured Loop-Gain at 100 Ω Load

	Frequency	Gain	Phase
Cursor 1 (Phase Margin)	1.7 kHz	0 dB	94.3°
Cursor 2 (Gain Margin)	>100 kHz	< -32 dB	0°

7. Load Step Transient Measurement Results

The Si34071-FW-24V-C7 output has been tested with a load step function to verify the converter output dynamic response. The output was tested with a 10%→90% and a 90%→10% load step.

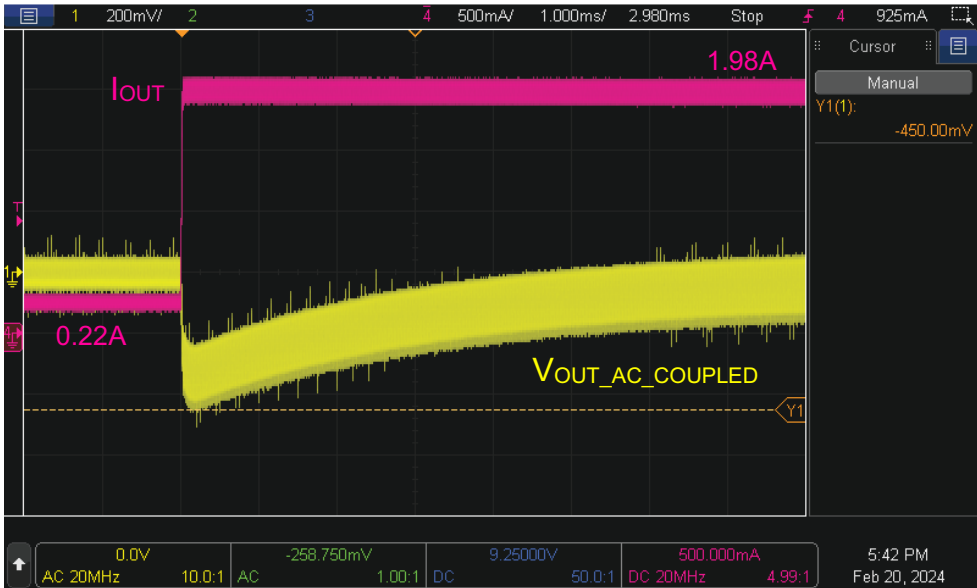


Figure 10. 24 V Output Load-Step Response (Current Step: 0.22 A → 1.98 A)

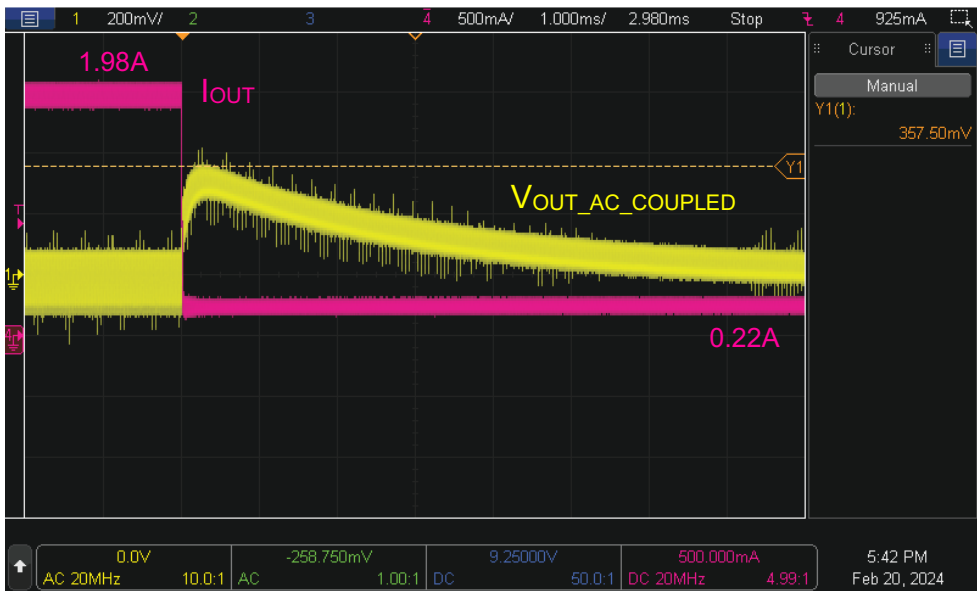


Figure 11. 5 V Output Load-Step Response (Current Step: 1.98 A → 0.22 A)

Current Step	Undershoot/Overshoot
10% to 90%	–450 mV
90% to 10%	+357 mV

8. Output Voltage Ripple

The Si34071-FW-24V-C7 board’s output voltage ripple has been measured at no-load (0 A) and full-load (2.2 A) conditions with 50 V input voltage. Figure 12 and Figure 13 show the respective results.

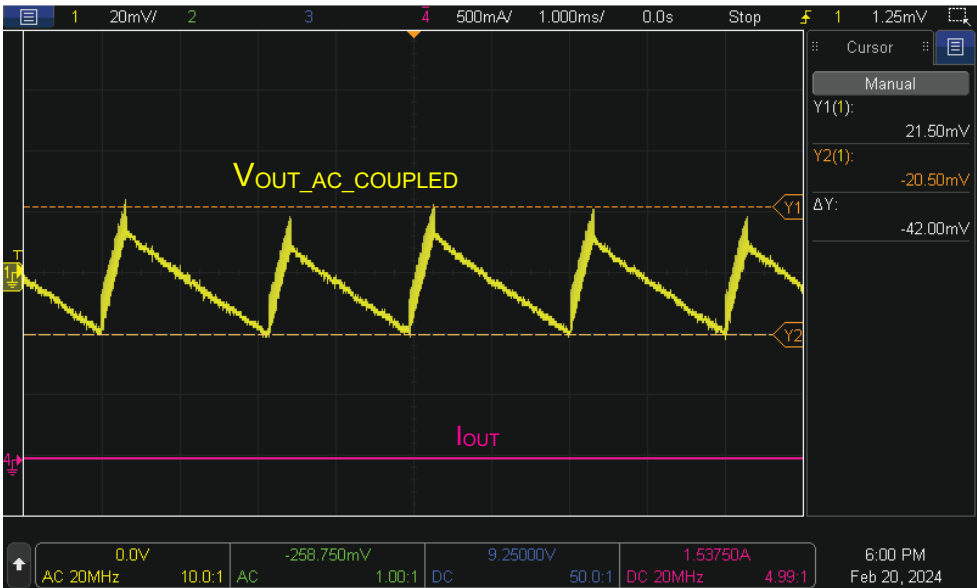


Figure 12. Si34071-FW-24V-C7 Output Voltage Ripple at No-Load Condition (42 mV)

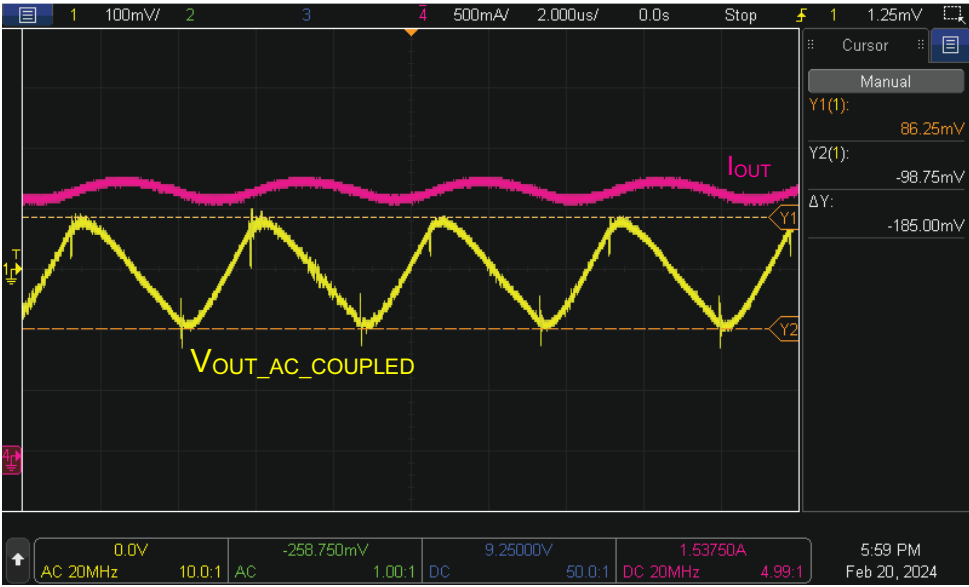


Figure 13. Si34071-FW-24V-C7 Output Voltage Ripple at Full-Load Condition (185 mV)

9. Soft Start Protection

The Si34071 device has an integrated dynamic soft-start protection mechanism to avoid stressing the components by the sudden current or voltage changes associated with the initial charging of the output capacitors.

The Si34071 intelligent adaptive soft-start mechanism does not require any external component to install. The controller continuously measures the input current of the PD and dynamically adjusts the internal I_{PEAK} limit during soft-start, that way adjusting the output voltage ramp-up time in a function of the attached load.

The controller lets the output voltage to rise faster in no load (or light load) condition. With heavy load at the output, the controller slows down the output voltage ramp to avoid exceeding the desired regulated output voltage value.

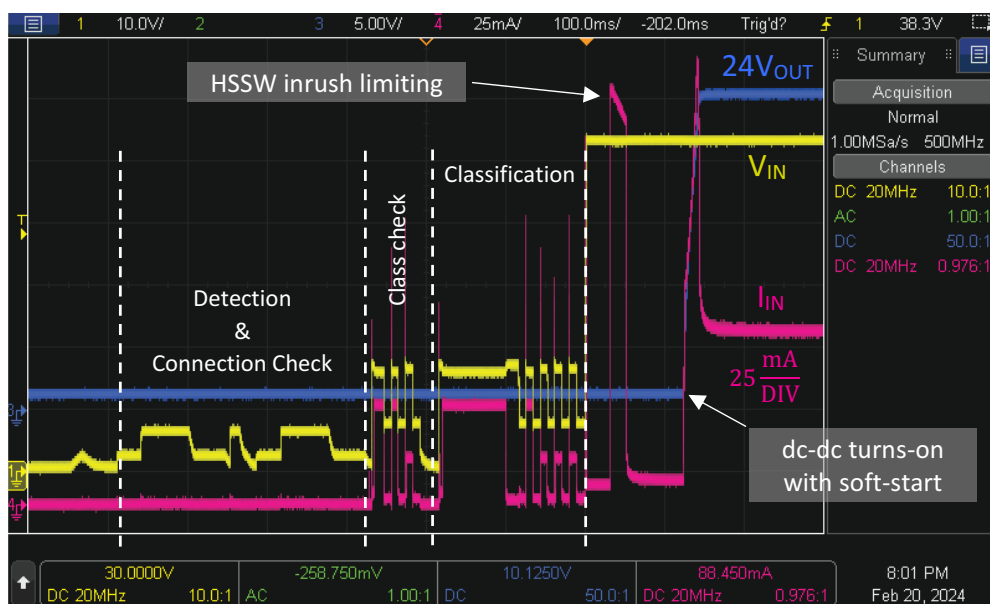


Figure 14. Soft Start Waveforms at Low Load Condition

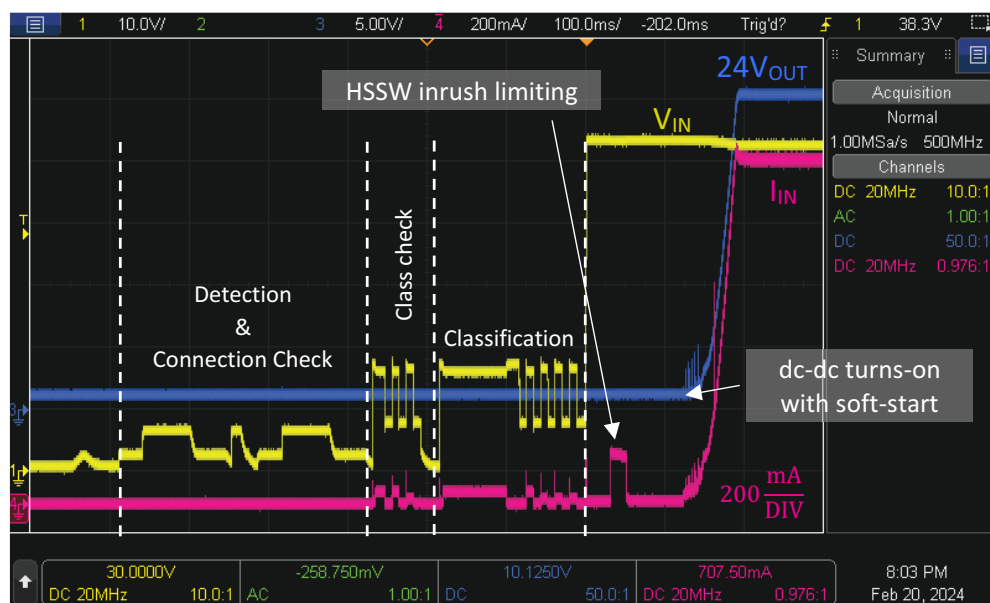


Figure 15. Soft Start Waveforms at Full Load Condition (2.2 A)

10. Output Short Protection

The Si34071 device has an integrated output short-protection mechanism that protects the IC itself and the surrounding external components from overheating, overvoltage, and overcurrent in case of an electrical short on the output. In case of output short, the energy is not reducing from the output filter inductor because the duty cycle and the voltage on the inductor is very low. To avoid overstressing the components in output short condition, the Si34071 sequentially resets itself and restarts with soft-start as long as the output short condition persists. [Figure 16](#) shows both the most stressed secondary freewheeling diode (D10) and the resultant input current. Both stay at safe levels under output short conditions.

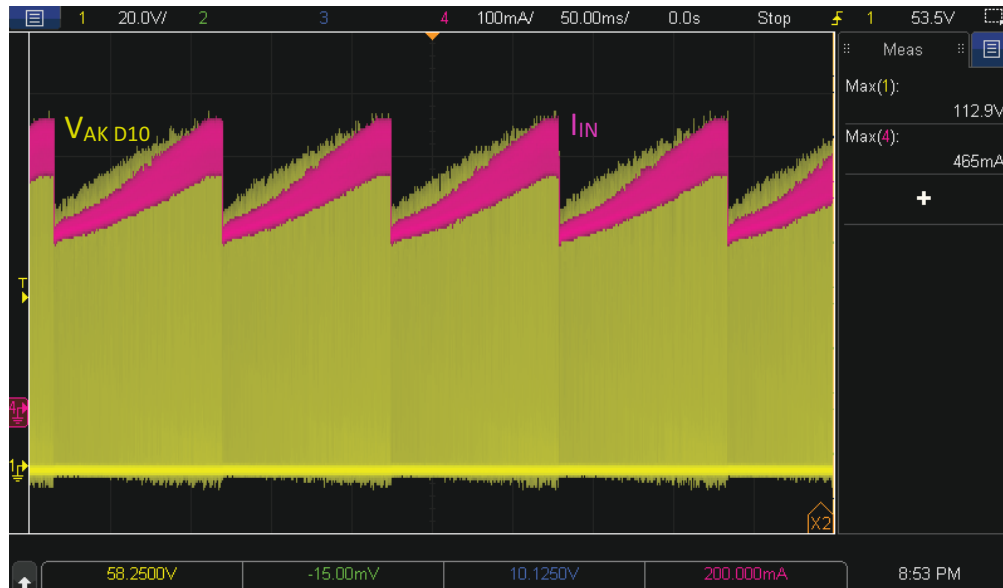


Figure 16. Si34071-FW-24V-C7 Output Short Protection Mechanism

11. Adjustable EVB Current Limit

Average current limit can be set by the RSENSE (R55) resistor. When the voltage on RSENSE reaches the internally fixed $-270\text{ mV}_{\text{Typ}}$ ($-305\text{ mV}_{\text{Min}}$, $-255\text{ mV}_{\text{Max}}$ referenced to V_{SS}), the Si34071 internal current limit circuit restarts the controller with soft-start protecting the application from overcurrent. In a Class 7 application, the recommended value for R_{SENSE} is $150\text{ m}\Omega$. Based on this value the average input current limit is given by the following formula:

$$R_{\text{SENSE}} = 150\text{ m}\Omega$$

$$I_{\text{LIMIT}} = \frac{270\text{ mV}}{150\text{ m}\Omega} = 1.8\text{ A}$$

Equation 1. Average Input Current Limit

12. Tunable Switching Frequency

The switching frequency of the oscillator is selected by choosing an external resistor R33 connected between the RFREQ and VPOS pins. The following figure will aid in selecting the RFREQ value to achieve the desired switching frequency.

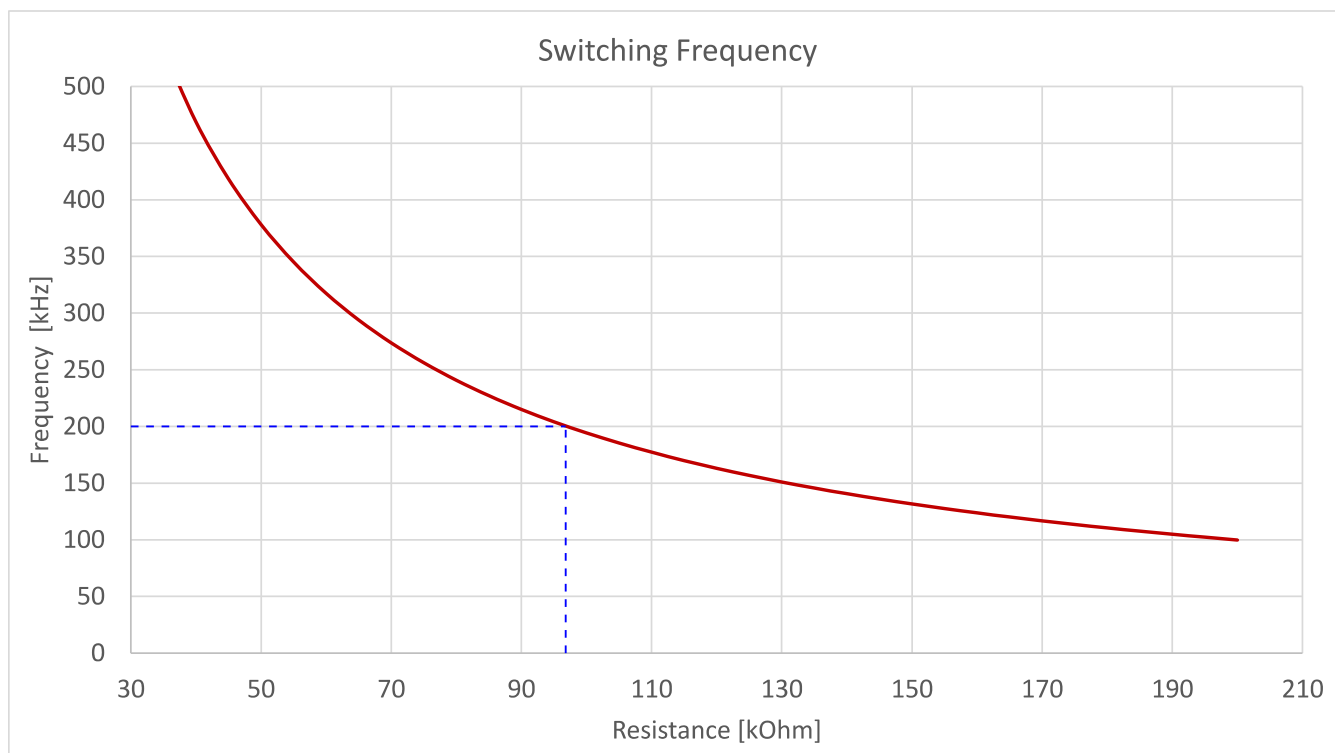


Figure 17. Switching Frequency vs. RFREQ

The selected switching frequency for Si34071-FW-24V-C7 is 200 kHz, which is achieved by setting resistor R33 to 95.3 k Ω .

13. Secondary Side Rectification

The Si34071-FW-24V-C7 EVB uses Schottky diode rectification on the secondary side of the transformer to save BOM cost. Figure 18 shows the secondary side rectification related part of the schematic.

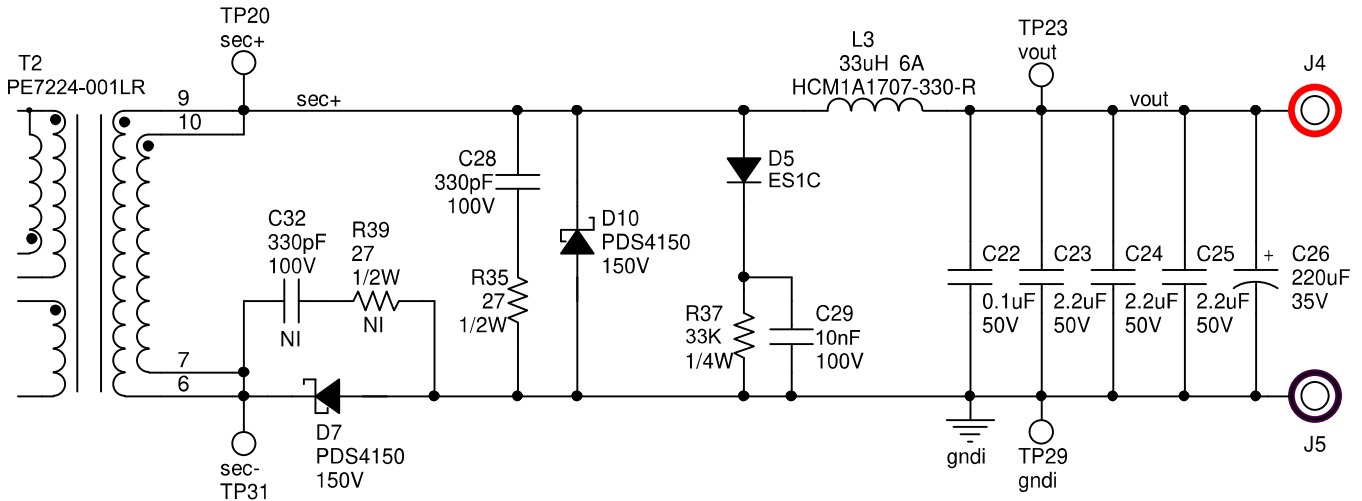


Figure 18. Self-Driven Synchronous Rectification

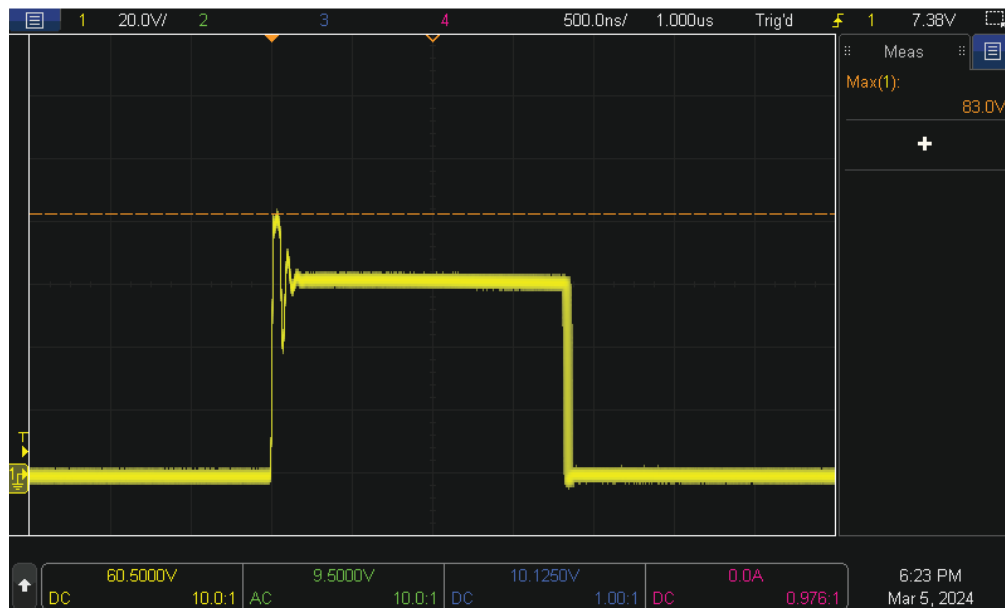


Figure 19. Voltage of Secondary Freewheeling Diode (D10) at Full Load



Figure 20. Voltage of Secondary Forward Diode (D7) at Full Load

14. Maintain Power Signature

The Si34071-FW-24V-C7 EVB offers both 802.3at and 802.3bt compliant MPS signature generation. For more information, see “AN1179: Si34071 802.3bt PD PoE Interface”.

15. Radiated Emissions Measurement Results—EN55032 Class B

Radiated emissions have been measured of the Si34071-FW-24V-C7 board with 50 V input voltage and full load connected to the output. As shown below, the Si34071-FW-24V-C7 is fully compliant with the international EN 55032 class B emissions standard.

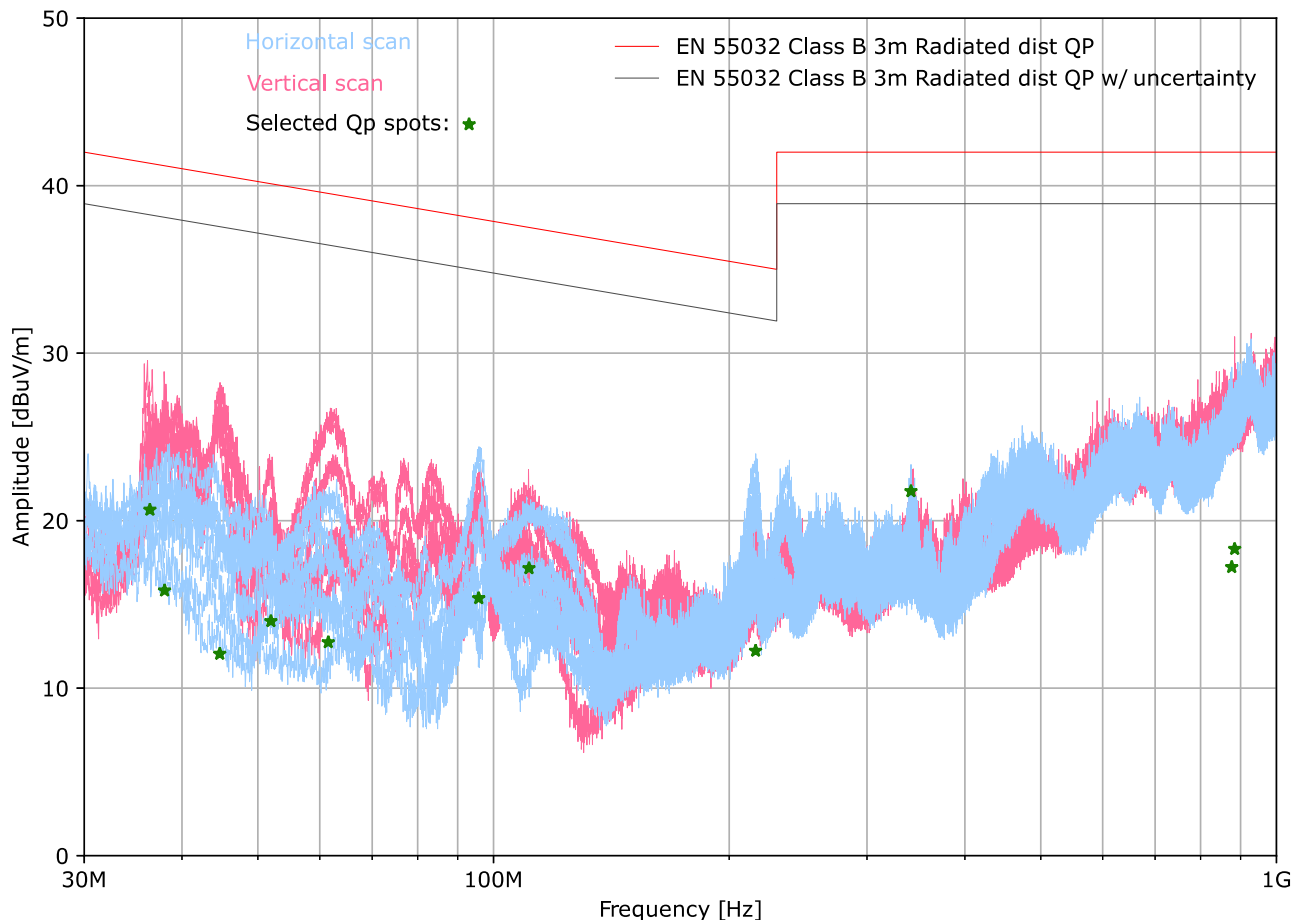


Figure 21. Si34071-FW-24V-C7 Radiated Emission Measurement Results

Radiated EMI Measurement Process:

The EVB is measured at full load with peak (Pk) detection in both vertical and horizontal polarizations. This is a relatively fast process that produces a purple curve (vertical polarization) and a blue curve (horizontal polarization).

Next, specific frequencies are selected (green stars) for quasi-peak (Qp) measurements. The board is measured again at those specific frequencies with a quasi-peak detector, which is a very slow but accurate measurement. The green stars represent the final results of the measurement process. To achieve results meeting the limits, the green stars should be below the highlighted EN 55032 Class B limit line (grey line).

16. Conducted Emissions Measurement Results—EN55032

The Si34071-FW-24V-C7 board's conducted emissions have been measured with both quasi-peak (QPk) and average (Avg) detectors. The following figures show the conducted EMI measurement setup and results.

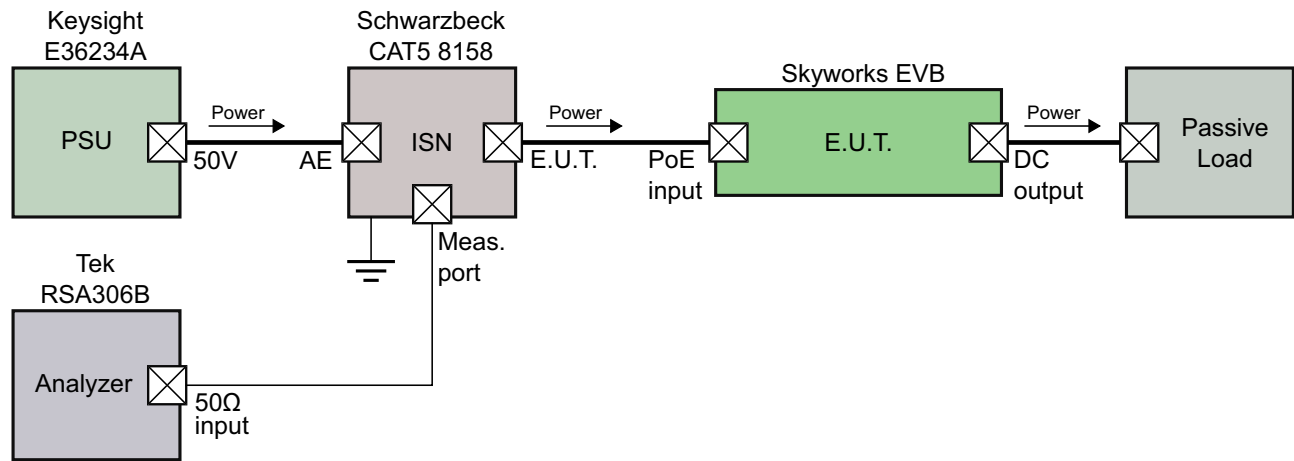


Figure 22. Conducted EMI Measurement Setup for PoE Input

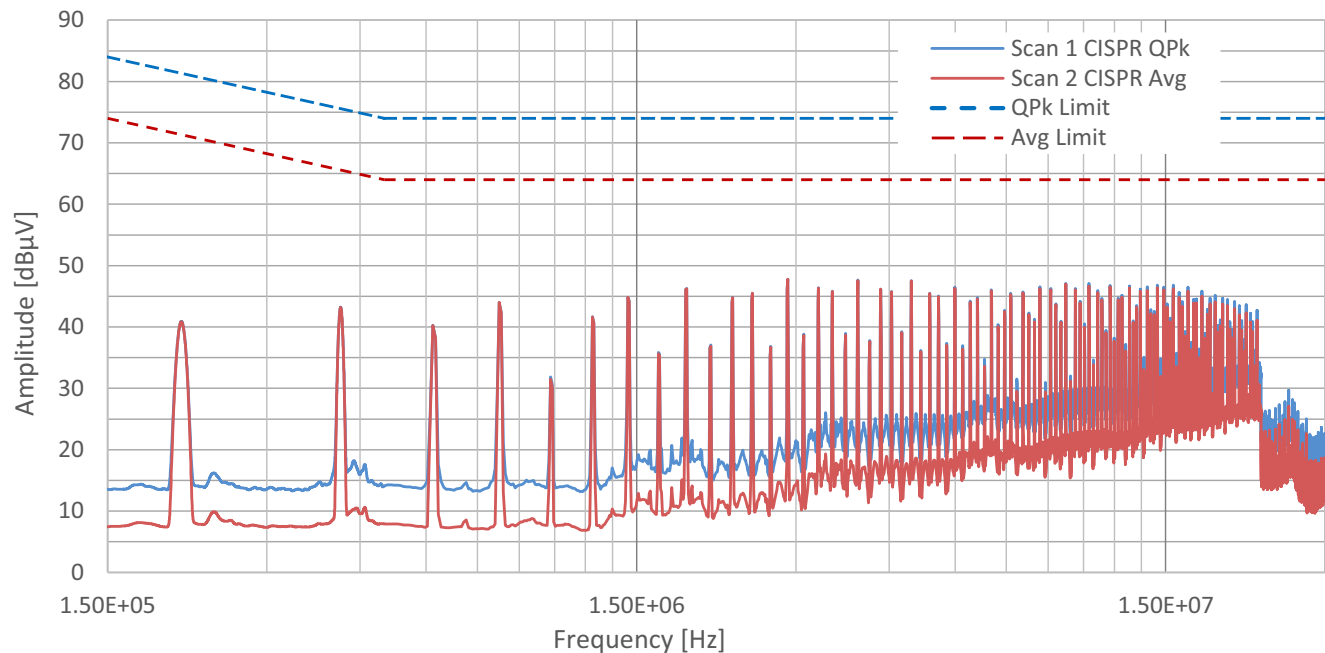


Figure 23. Conducted Emissions Measurement on PoE Input, 50 V Input, Full Load

17. Thermal Measurements

The thermal image of the Si34071-FW-24V-C7 board at 25 °C ambient temperature is shown in Figure 24.

Test Condition	Specification
Input voltage	50 V
Input Current	1203 mA
Output voltage	24.56 V
Output current	2.2 A
Ambient temperature	25 °C

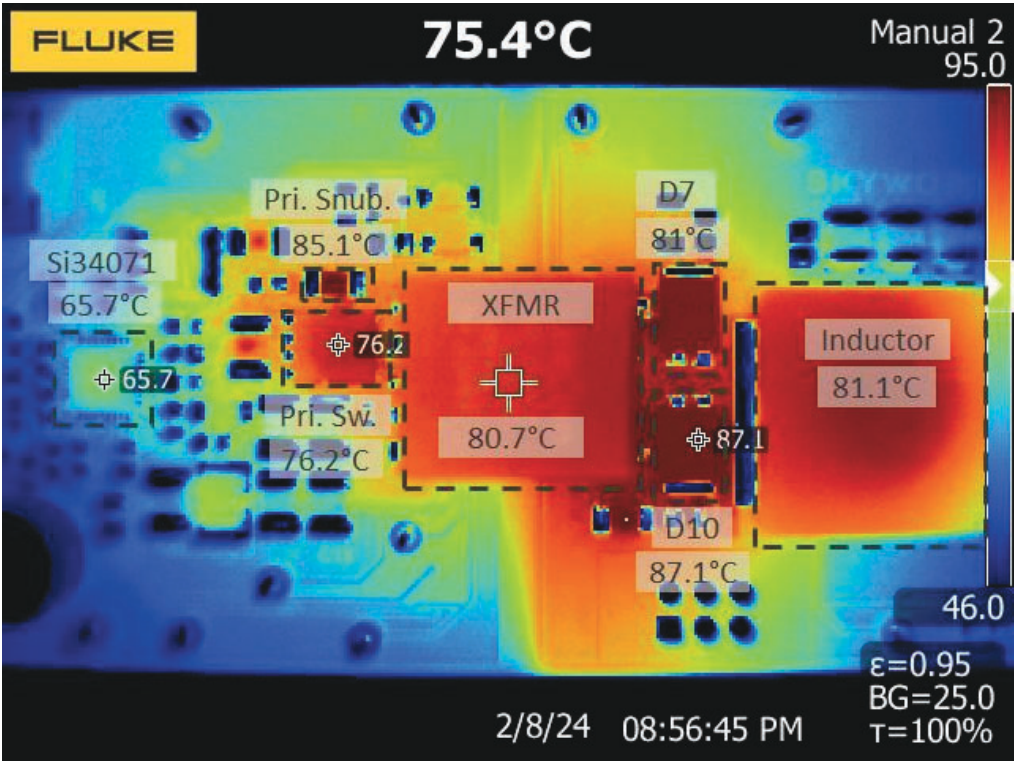


Figure 24. Thermal Image of the Top Side

18. Layout

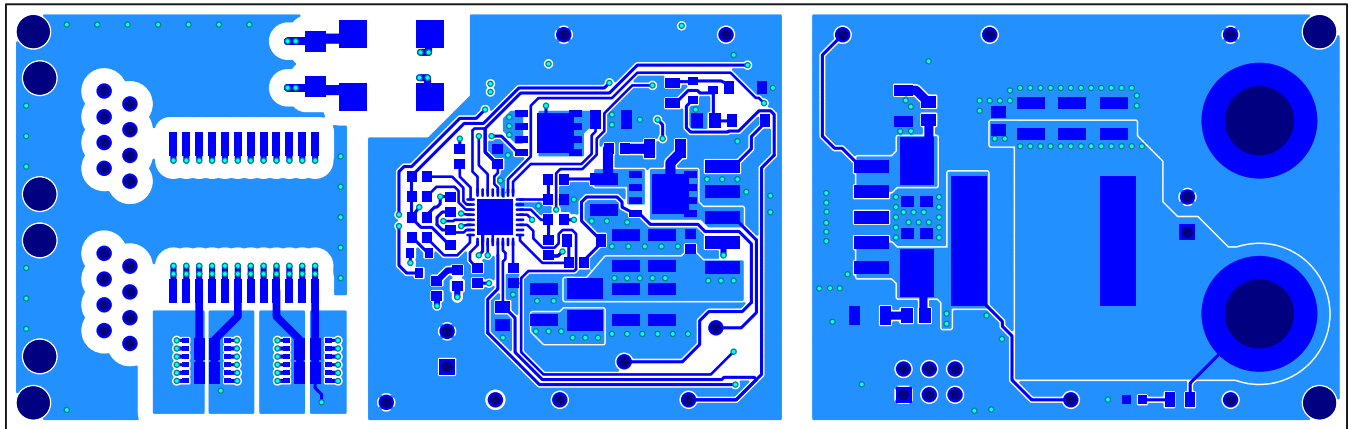


Figure 25. Top Layer

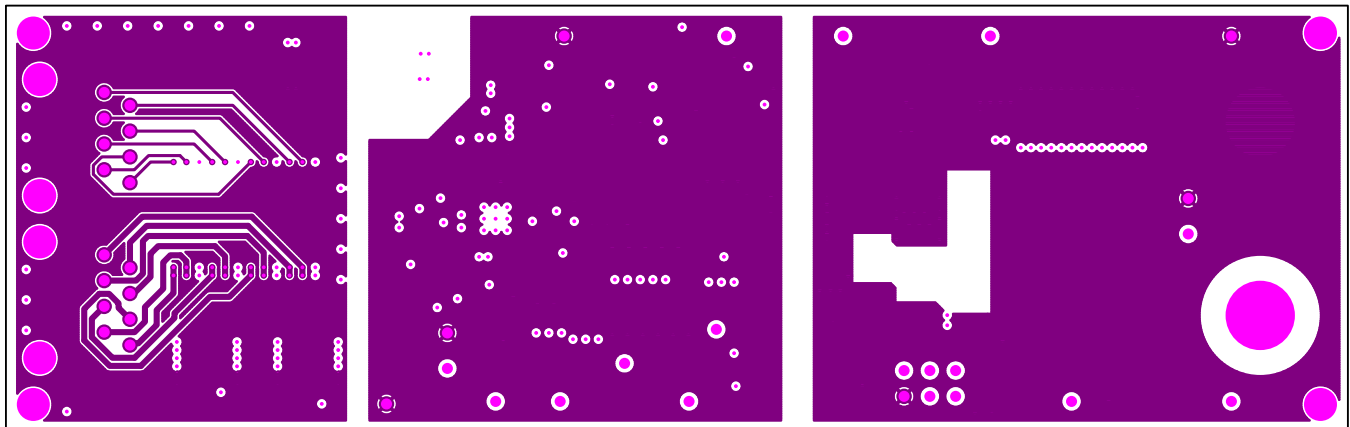


Figure 26. Internal 1 Layer

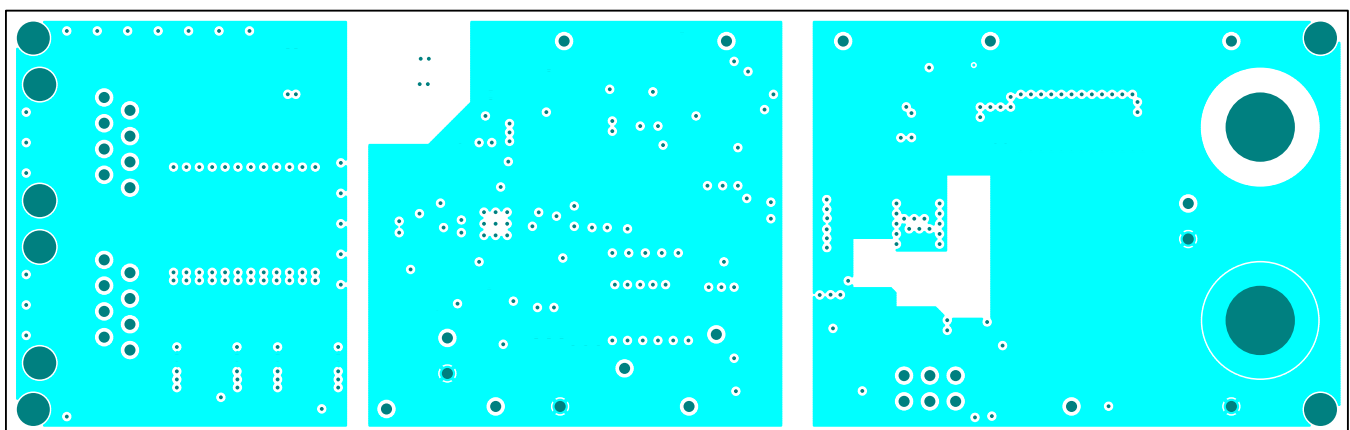


Figure 27. Internal 2 Layer

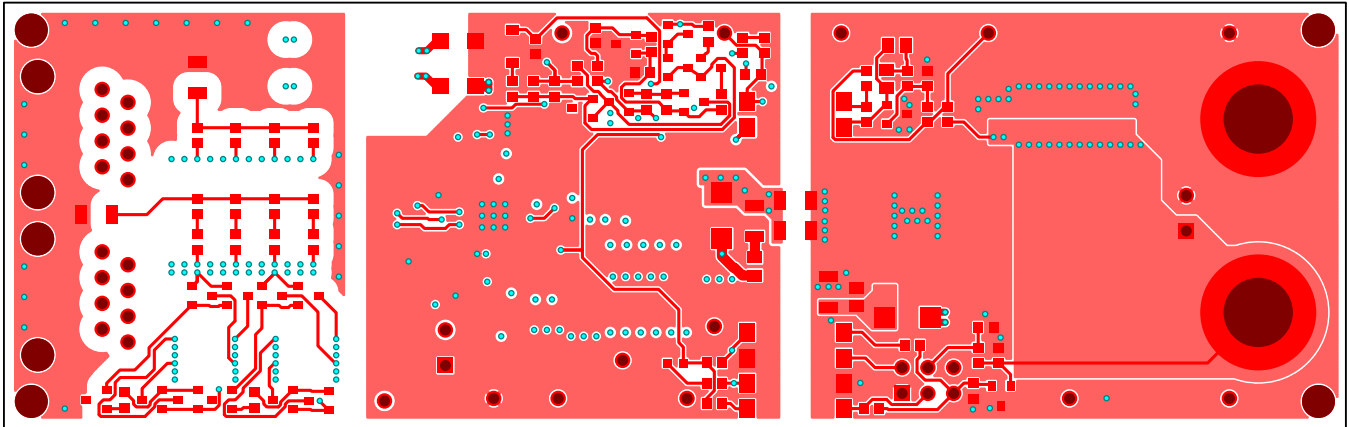


Figure 28. Bottom Layer

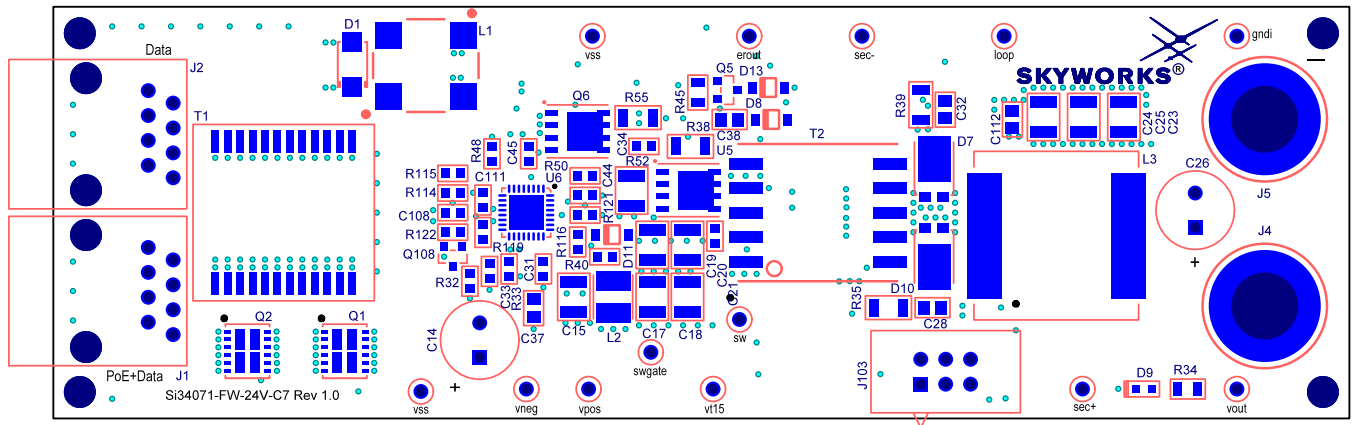


Figure 29. Assembly Top

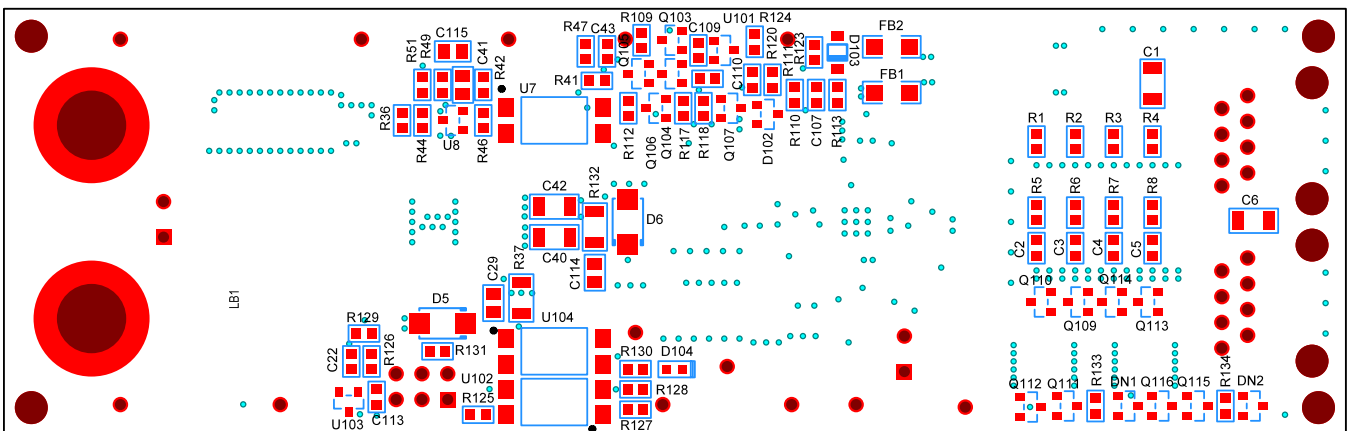


Figure 30. Assembly Bottom

19. Bill of Materials

Table 5. Si34071-FW-24V-C7 Bill of Materials

Designator	Qty	Description	Manufacturer	Manufacturer PN
C1, C6, C4, C8, C72, C42	4	1 nF, 2000 V, ±5%, X7R	Kemet	C1206C102JGRACU
C108	1	0.1 μF, 25 V, ±10%, X7R	Venkel	C0603X7R250-104K
C109	1	1 nF, 100 V, ±10%, X7R	Venkel	C0603X7R101-102K
C111	1	47 pF, 100 V, ±10%, X7R	Venkel	C0603X7R101-470K
C115	1	0.1 μF, 50 V, ±10%, X7R	Venkel	C0805X7R500-104K
C14	1	47 μF, 100 V, ±20%, Alum_Elec	Panasonic	ECA2AM470
C15, C17, C18, C19, C20	5	4.7 μF, 100 V, ±10%, X7R	Venkel	C1210X7R101-475KNE
C2, C3, C4, C5, C107, C110	6	0.01 μF, 100 V, ±10%, X7R	Venkel	C0603X7R101-103K
C21, C33	2	0.1 μF, 100 V, ±10%, X7R	Venkel	C0603X7R101-104K
C22	1	0.1 μF, 50 V, ±10%, X7R	Venkel	C0603X7R500-104K
C23, C24, C25	3	2.2 μF, 50 V, ±10%, X7R	Kemet	C1210C225K5RACTU
C26	1	220 μF, 35 V, ±20%, Alum_Elec	Würth	860020574012
C28	1	330 pF, 100 V, ±20%, X7R	Venkel	C0805X7R101-331M
C29	1	0.01 μF, 200 V, ±10%, X7R	Venkel	C0805X7R201-103K
C31	1	220 nF, 16V, ±5%, X7R	Kemet	C0603C224J4RACTU
C34	1	330 pF, 250 V, ±20%, COG	TDK	C1608COG2E331J
C37, C38	2	1 μF, 50 V, ±10%, X7R	Samsung	CL21B105KBFNNNE
C41	1	33 nF, 50 V, ±10%, X7R	Venkel	C0805X7R500-333KNE
C44	1	1 nF, 50 V, ±5%, COG	Venkel	C0603COG500-102J
C45	1	0.1 μF, 10 V, ±10%, X7R	Venkel	C0603X7R100-104K
D102	1	BAV99, 100 V, Dual, Switch	Diodes Inc.	BAV99-7-F
D103	1	10 V, 10 V, 5%, Zener	On Semi	MMSZ4697T1G
D13	1	13 V, 13 V, 5%, Zener	On Semi	MMSZ4700T1G
D5, D6	2	ES1C, 150 V, Fast	Diodes Inc.	ES1C
D7, D10	2	PDS4150, 150 V, Schottky	Diodes Inc.	PDS4150-13
D8, D11	2	1N4148W, 100 V, Single	Diodes Inc.	1N4148W-7-F
D9	1	GREEN, 2.0 V, SMT	LUMEX INC	SML-LXFP0603SUGCTR
DN1, DN2	2	27 V, 27 V, Zener, Dual	On Semi	MMBZ27VALT1G
FB1, FB2	2	600 Ω, SMT	Würth	742792118
J1, J2	2	RJ-45, Receptacle	MOLEX	095501-2881
J4, J5	2	BND_POST, BANANA	ABBATRON	101
L1	1	250 μH, 80 VDC, Ethernet	Würth	744272251
L2	1	2.2 μH, ±20%, Unshielded	Murata	84222C
L3	1	33 μH, ±20%, Shielded	Eaton	HCM1A1707-330-R

Table 5. Si34071-FW-24V-C7 Bill of Materials (Continued)

Designator	Qty	Description	Manufacturer	Manufacturer PN
Q1, Q2	2	FDMQ8205A, FET Bridge	OnSemi	FDMQ8205A
Q103, Q104, Q105	3	MMBTA56L, -80 V, PNP	On Semi	MMBTA56L
Q106, Q107, Q108	3	MMBTA06LT1, 80 V, NPN	On Semi	MMBTA06LT1
Q109, Q111, Q113, Q115	4	BC846B, 65 V, NPN	Nexperia	BC846B
Q110, Q112, Q114, Q116	4	BC856A, -65 V, PNP	Diodes Inc.	BC856A
Q5	1	BSS64AHZGT116, 100 V, NPN	Rohm Semi.	BSS64AHZGT116
Q6	1	SQJ476EP-T1, 100 V, N-CHNL	Vishay	SQJ476EP-T1_GE3
R1, R2, R3, R4, R5, R6, R7, R8	8	75 Ω , $\pm 0.5\%$, ThickFilm	Susumu	RR0816Q-750-D
R110, R113, R119	3	100 k Ω , $\pm 1\%$, ThickFilm	Venkel	CR0603-10W-1003F
R111, R112	2	20.0 k Ω , $\pm 1\%$, ThickFilm	Venkel	CR0603-16W-2002F
R114	1	215 Ω , $\pm 1\%$, ThickFilm	Venkel	CR0603-10W-2150F
R115	1	137 Ω , $\pm 1\%$, ThickFilm	Venkel	CR0603-10W-1370FT
R116	1	22.1 k Ω , $\pm 1\%$, ThickFilm	Panasonic	CR0603-10W-2212F
R117, R118	2	49.9 k Ω , $\pm 1\%$, ThickFilm	Venkel	CR0603-10W-4992F
R120	1	41.2 k Ω , $\pm 1\%$, ThickFilm	Venkel	CR0603-10W-4122F
R121	1	130 k Ω , $\pm 1\%$, ThickFilm	Venkel	CR0603-10W-1303FT
R122	1	10 k Ω , $\pm 1\%$, ThickFilm	Venkel	CR0603-16W-1002F
R123	1	1.20 k Ω , $\pm 1\%$, ThickFilm	Venkel	CR0603-10W-1201F
R133, R134	2	162 k Ω , $\pm 1\%$, ThickFilm	Venkel	CR0603-16W-1623F
R32	1	3.0 Ω , $\pm 5\%$, ThickFilm	Venkel	CR0603-10W-3R0JT
R33	1	95.3 k Ω , $\pm 1\%$, ThickFilm	Venkel	CR0603-16W-9532F
R34	1	10 k Ω , $\pm 1\%$, ThickFilm	Venkel	CR0805-8W-1002F
R35, R38	2	27 Ω , $\pm 1\%$, ThickFilm	TE	CRGP1206F27R
R36, R40	2	10.0 Ω , $\pm 1\%$, ThickFilm	Venkel	CR0603-16W-10R0F
R37	1	33 k Ω , $\pm 5\%$, ThickFilm	Venkel	CR1206-4W-333JT
R41, R109	2	3.65 k Ω , $\pm 1\%$, ThickFilm	Venkel	CR0603-16W-3651FT
R42	1	2.2 k Ω , $\pm 1\%$, ThickFilm	Venkel	CR0603-10W-2201F
R44	1	36.5 k Ω , $\pm 1\%$, ThickFilm	Venkel	CR0603-16W-3652F
R45	1	3.3 k Ω , $\pm 1\%$, ThickFilm	Venkel	CR0805-10W-3301F
R47, R49	2	0 Ω , ThickFilm	Venkel	CR0603-16W-000
R48, R124	2	24.9 k Ω , $\pm 1\%$, ThickFilm	Venkel	CR0603-10W-2492F
R50	1	100 Ω , $\pm 1\%$, ThickFilm	Venkel	CR0603-10W-1000F
R51	1	4.12 k Ω , $\pm 1\%$, ThickFilm	Venkel	CR0603-10W-4121F
R52	1	0.04 Ω , $\pm 1\%$, ThickFilm	Venkel	LCR1210-R040FT
R55	1	0.15 Ω , $\pm 1\%$, ThickFilm	Venkel	LCR1206-R150F

Table 5. Si34071-FW-24V-C7 Bill of Materials (Continued)

Designator	Qty	Description	Manufacturer	Manufacturer PN
T1	1	7490220122, Ethernet Jack	Würth	7490220122
T2	1	PE7224-001LR, 24 V, FORWARD	LinkCom	PE7224-001LR
U101	1	TLV431, SHUNT	TI	TLV431BCDBZR
U5	1	SIR632DP-T1, 150 V, N-CHNL	Vishay	SIR632DP-T1-RE3
U6	1	Si34071, 120 V, PD	Skyworks	Si34071-A01-GM
U7	1	FOD817C3SD,	Vishay	FOD817C3SD
U8	1	TL432B, 36 V, VREF	TI	TL432BCDBZR
Not Installed Components				
C112	1	1 μ F, 50 V, $\pm$ 10%, X7R	Samsung	CL21B105KBFNNNE
C113	1	1 μ F, 6.3 V, $\pm$ 10%, X5R	Venkel	C0603X5R6R3-105K
C114	1	820 pF, 200 V, $\pm$ 10%, C0G	Venkel	C0805C0G201-821KNE
C32	1	330 pF, 100 V, $\pm$ 20%, X7R	Venkel	C0805X7R101-331M
C43	1	22 nF, 16 V, $\pm$ 20%, X7R	Venkel	C0603X7R160-223M
D1	1	SMAJ58A, 58 V	Littelfuse	SMAJ58A
D104	1	LED, Yellow	Vishay	TLMY1000-GS08
J103	1	3X2 Shrouded Header	3M	30306-6002HB
R126	1	100 k Ω , $\pm$ 1%, ThickFilm	Venkel	CR0603-10W-1003F
R127	1	330 Ω , $\pm$ 1%, ThickFilm	Venkel	CR0603-16W-3300F
R128	1	560 Ω , $\pm$ 1%, ThickFilm	Venkel	CR0603-10W-5600F
R129	1	120 k Ω , $\pm$ 1%, ThickFilm	Venkel	CR0603-10W-1203F
R132	1	10 Ω , $\pm$ 1%, ThickFilm	Venkel	CR1206-4W-10R0F
R39	1	27 Ω , $\pm$ 1%, ThickFilm	TE	CRGP1206F27R
R46, R125, R130, R131	4	1 k Ω , $\pm$ 1%, ThickFilm	Venkel	CR0603-10W-1001F
U102, U104	2	FOD817C3SD	Vishay	FOD817C3SD
U103	1	LM3480IM3X-3.3	TI	LM3480IM3-3.3

20. Si34071-FW-24V-C7 Design and Layout Checklist

Complete EVB design databases can be found on the Skyworks [Power over Ethernet](#) page. Skyworks strongly recommends using these EVB schematics and layout files as a starting point to ensure robust performance and avoid common mistakes in the schematic capture and PCB layout processes.

Below is a recommended design checklist that can assist in trouble-free development of robust PD designs.

Refer also to the “[Si34071 Data Sheet](#)” and “[AN1130: Si3404/06x PoE-PD Controller Design Guide](#)” when using the following checklist.

1. Design Planning Checklist:
 - a. Determine if your design requires an isolated or non-isolated topology. For more information, see AN1130.
 - b. Skyworks strongly recommends using the EVB schematics and layout files as a starting point as you begin integrating the Si34071 into your system design process.
 - c. Determine your load's power requirements (i.e., VOUT and IOUT consumed by the PD, including the typical expected transient surge conditions).
 - d. Based on your required PD power level, select the appropriate class resistors (R114, R115, R116, R121) value by referring to “[AN1179: Si34071 802.3bt PD PoE Interface](#)”.
2. General Design Checklist:
 - a. Non-standard PoE injectors turns on the PD without detection and classification phases. In most cases, dV/dt is not controlled and could violate IEEE requirements. To ensure robustness with those injectors, please include a $3\ \Omega$ resistor in place of R32.
 - b. If industrial temperature range (-40 to $+85\ ^\circ\text{C}$) of operation is required then some components need to be replaced. For stable operation at low temperatures up to $-40\ ^\circ\text{C}$, change the following parts in your design: C26 aluminum electrolytic capacitor with a $100\ \mu\text{F}/35\ \text{V}$ aluminum polymer capacitor (for example: Würth Elektronik 870135675003), change R41 to 2.2k, change R42 to 3.9k and if the input rectifiers are FET bridges install low-leakage Schottky diodes (for example BAT46ZFILM) in parallel with the FETs body diode as noted in AN1179. At the high temperature range, up to $+85\ ^\circ\text{C}$, detection resistance R48 change may be needed, for more information, see AN1179.
3. Layout Guidelines:
 - a. Make sure VNEG pin of the Si34071 is connected to the backside of the QFN package with an adequate thermal plane.
 - b. Use solid primary side VSS plane under switching circuits to make a low impedance return path. A solid VSS plane can greatly reduce the radiated emission of the board.
 - c. Keep the trace length from the switching FET to VSS as short as possible. Make all the high current traces as short, direct, and thick as possible. It is a good practice on a standard PCB board to make the traces an absolute minimum of 15 mils (0.381 mm) per ampere.
 - d. Usually, one standard via handles 200 mA of current. If the trace needs to conduct a significant amount of current from one plane to the other, use multiple vias.
 - e. Keep the high di/dt circular area of the loop from the primary forward FET to the transformer and returning from the input filter capacitors (C17..C21) to VSS as small a diameter as possible. Also, minimize the high di/dt circular area of the loop from the output of the transformer to the rectifier diodes (D7/D10) as small as possible.
 - f. Keep the high dv/dt traces as short as possible.
 - g. Keep the feedback and loop stability components as far from the transformer and noisy power traces as possible.

To help ensure first-pass success, contact our customer support by submitting a help ticket and uploading your schematics and layout files for review.

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