



SKYWORKS®

USER GUIDE

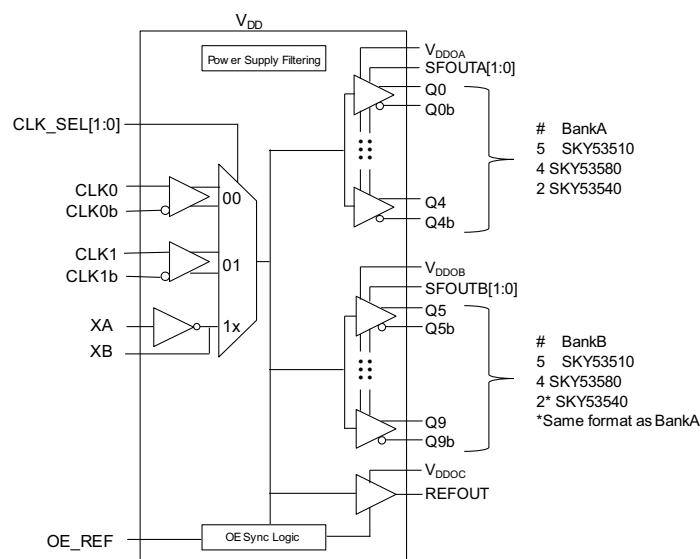
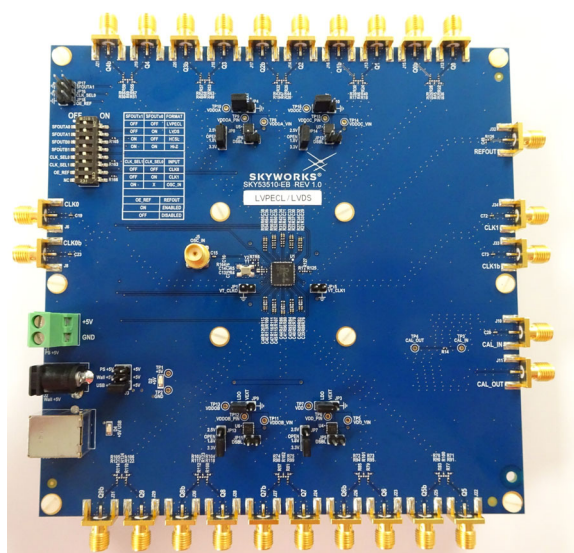
UG523: SKY53510 Customer Evaluation Board User Guide

The SKY53510 Customer Evaluation Board (CEVB) is used to evaluate Skyworks' 10-output low additive jitter clock buffer, whose input clocks can be sourced by a low-jitter clock source, such as the Si5518, to evaluate Skyworks' best-in-class buffered output clock jitter in 5G/eCPRI/SyncE/IEEE 1588 applications.

This document is intended to assist the user in configuring the switches and jumpers, various board features, and general board setup for measuring supply currents, signal integrity, propagation delay, output-to-output skew, additive jitter, and input mux isolation. Also included are the board schematics and BOM.

Key Features

- Ultra-low additive jitter for 10 output clocks
- Powered from USB, Wall Wart, or External supply
- Designed for quick setup and “ease of use”
- Calibration traces included which match the input (to DUT) and output (from DUT) trace length and layout geometry to simplify propagation delay measurements
- Precision 0.1 Ω resistors to simplify supply current measurements
- All DUT configuration centralized in an 8-position switch
- Designed to accommodate all LVDS, LVPECL, and HCSL configurations (e.g., ac/dc-coupled, 1.8 V, 2.5 V, 3.3 V, and source- or end-terminated HCSL)
- Plug and Play – no software setup required
- XTAL/Ext Clk input option
- CMOS output clock (only available on output REFOUT)



1. Functional Block Diagram

Below is a functional block diagram of the SKY53510 CEVB. This evaluation board can be powered by connecting to your PC's USB connector or by an external +5 V dc power source. Note that VDD should always be selected to be equal to or higher than the highest VDDOx supply voltage.

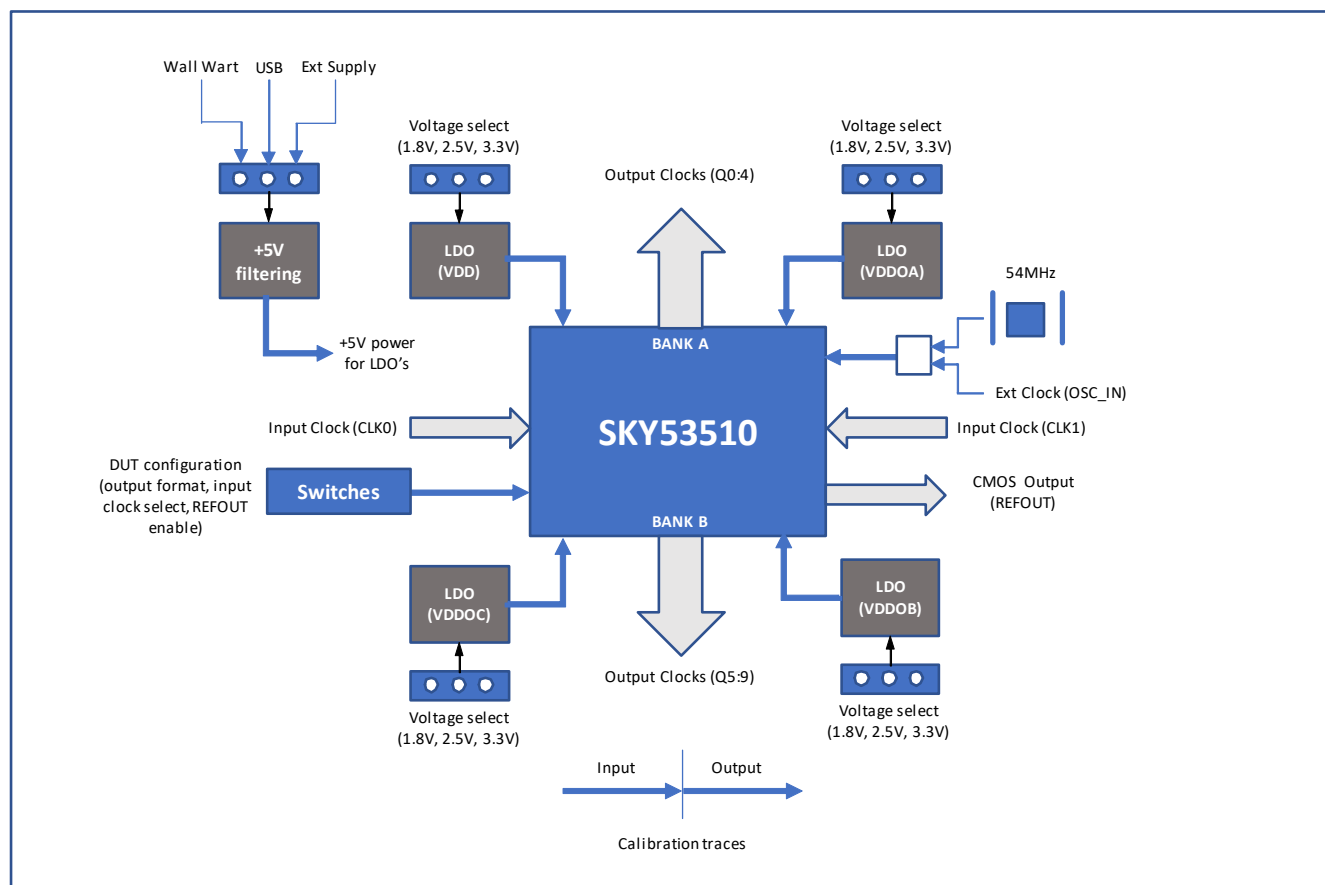


Figure 1. SKY53510 CEVB Functional Block Diagram

2. Quick Start Guide

This section provides an overview of the EVB board. Important board jumpers, switches, and LEDs and their locations are described in [Figure 2](#) below.

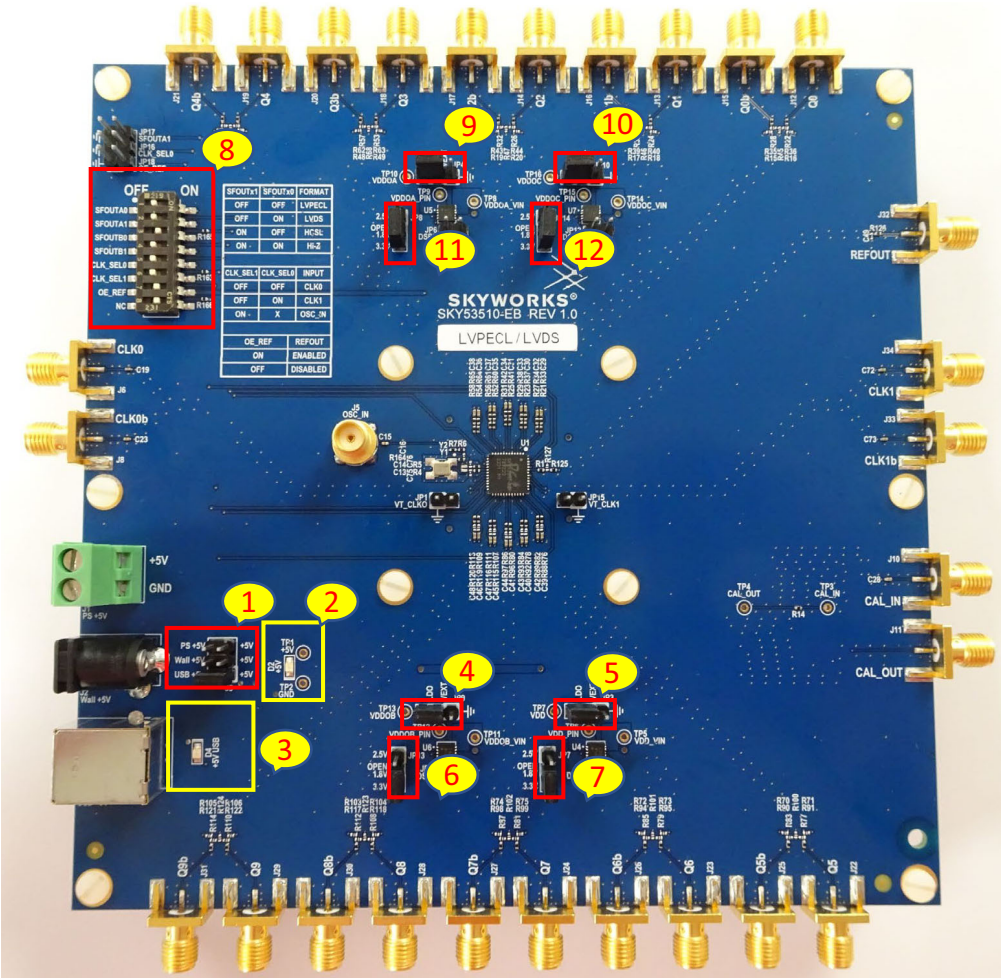


Figure 2. Jumpers, Switches, and LED Locations

The board is shipped with the jumpers in their default configuration +5 V from USB, LDO power, and +3.3 V for each supply: V_{DD} , V_{DDOA} , V_{DDOB} , and V_{DDOC} . It is, however, recommended to double-check. Refer to [Table 1](#) below for a description of each jumper, switch, and LED. Note that Pin 1 of each jumper has a bold outline on the silkscreen.

Table 1. Jumpers, Switches, and LED Description and Default Configuration

Callout	RefDes	Schematic Page	Description	Default Configuration	Options
1	J3	3	External +5 select	USB +5 V	Wall Wart (Wall +5 V) Power Supply (PS +5 V)
2	D2	3	LED green; should illuminate when +5 V source is applied and J3 jumper installed.		
3	D4	3	LED blue; should illuminate when USB source is applied.		
4	JP9	9	V _{DDOB} source select	LDO (Pins 2,3 jumped)	VEXT: supply on pin 2; Gnd on Pin 1
5	JP3	9	V _{DD} source select	LDO (Pins 2,3 jumped)	VEXT: supply on pin 2; Gnd on Pin 1
6	JP13	9	V _{DDOB} voltage select	+3.3 V (Pins 2,3 jumped)	+2.5 V (Pins 1,2 jumped) +1.8 V (jumper removed)
7	JP7	9	V _{DD} voltage select	+3.3 V (Pins 2,3 jumped)	+2.5 V (pins 1,2 jumped) +1.8 V (jumper removed)
8	SW1	8	DUT configuration select	User-defined Refer to table on silkscreen for switch settings.	
9	JP4	9	V _{DDOA} source select	LDO (Pins 2,3 jumped)	VEXT: supply on Pin 2, Gnd on Pin 1
10	JP10	9	V _{DDOC} source select	LDO (Pins 2,3 jumped)	VEXT: supply on Pin 2, Gnd on Pin 1
11	JP8	9	V _{DDOA} voltage select	+3.3 V (Pins 2,3 jumped)	+2.5 V (Pins 1,2 jumped) +1.8 V (jumper removed)
12	JP14	9	V _{DDOC} voltage select	+3.3 V (Pins 2,3 jumped)	+2.5 V (Pins 1,2 jumped) +1.8 V (jumper removed)
none	JP1, JP5, JP6, JP11, JP12, JP15, JP16, JP17, JP18	5, 8, 9	various	No jumper installed	JP5, JP6, JP11, JP12: disables the LDO when installed JP16, JP17, JP18: used for measuring startup, enable, and disable times JP1, JP15: external input bias voltage

Perform the following tasks before taking measurements:

1. Apply a +5 V source and position the J3 jumper in the corresponding position.
2. Decide whether to source each supply voltage via on-board LDO or externally (Callouts 4, 5, 9, 10).
3. Decide what voltage you want for each supply (Callouts 6, 7, 11, 12).
4. Configure switch SW1 (Callout 8) for Bank A, B output format, Input clock select, and Refclk enable.
5. Apply an input to either CLK0, CLK1, or choose the on-board XTAL.
6. Connect an output to your test equipment and start taking measurements.

3. Signal Path and Configuration Settings (SW1)

The SKY53510 supports both single-ended and differential input clocks (CLK0, CLK1) along with an external fundamental mode crystal (the CEVB is populated with a 54 MHz crystal) which can be bypassed via minor board modification to allow the input to be driven by an external single-ended clock (OSC_IN). The selection of input clock is pin-controlled via switch SW1 according to the following table.

Table 2. Configuration of Switch SW1 for Input Clock Selection

CLK_SEL1 SW1 pos 6	CLK_SEL0 SW1 pos 5	INPUT
OFF	OFF	CLK0
OFF	ON	CLK1
ON	X	XTAL/OSC_IN

Refer to “6. Crystal Oscillator Interface” on page 8 for instructions on how to modify the board to accept an external single-ended clock.

The board provides access to ten of the SKY53510 device’s differential outputs. There are five outputs assigned to Bank A (Q0:Q4) and five assigned to Bank B (Q5:Q9). The five differential outputs on each bank can be configured for the following formats: LVPECL, LVDS, HCSL, or Hi-Z. The selection of output clock format is pin-controlled via switch SW1 according to Table 3.

Table 3. Configuration of Switch SW1 for Output Clock Format Selection

SFOUTA1 SW1 pos 2	SFOUTA0 SW1 pos 1	SFOUTB1 SW1 pos 4	SFOUTB0 SW1 pos 3	FORMAT
Bank A		Bank B		
OFF	OFF	OFF	OFF	LVPECL
OFF	ON	OFF	ON	LVDS
ON	OFF	ON	OFF	HCSL
ON	ON	ON	ON	Hi-Z

An additional LVCMOS output is assigned to REFOUT which can be enabled or disabled via pin-control of switch SW1 according to the following table.

Table 4. Configuration of Switch SW1 for Enable/Disable of Output REFOUT (LVCMOS)

OE_REF SW1 pos 7	REFOUT
ON	ENABLED
OFF	DISABLED

4. External Power and Voltage Supply Circuits

The power supply section of the CEVB provides flexibility to apply +5 V power to the board via three optional sources: USB, wall wart, or lab dc power supply.

Figure 3 shows these three power sources and the power selection jumper (J3). Refer to schematic page 3.

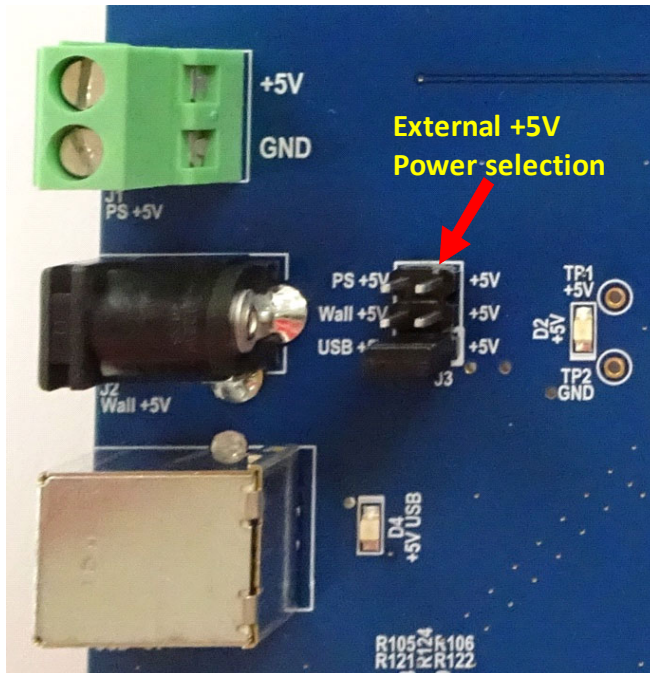


Figure 3. External +5 V Power and Selection Circuit

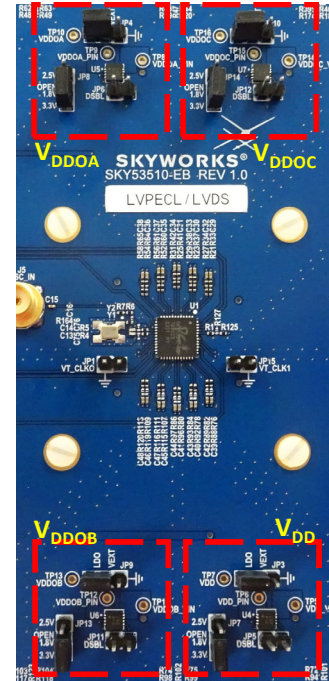


Figure 4. LDO Circuit

There are four LDO circuits on-board that take the selected +5 V supply and regulate it to either +3.3 V, +2.5 V, or +1.8 V that sources different circuits of the SKY53510 buffer. The voltage to each of these buffer circuits is jumper-controlled independently for V_{DD} (JP7), V_{DDOA} (JP8), V_{DDOB} (JP13), and V_{DDOC} (JP14). Each LDO circuit includes a jumper that, when installed, disables the LDO (JP5, JP6, JP11, and JP12 for V_{DD} , V_{DDOA} , V_{DDOB} , and V_{DDOC} , respectively). The LDO can also be bypassed and the buffer circuit sourced externally via jumpers JP3 (V_{DD}), JP4 (V_{DDOA}), JP9 (V_{DDOB}), and JP10 (V_{DDOC}) by applying a dc voltage to jumper Pin 2 and ground to jumper Pin 1. Figure 4 above shows these four LDO circuits. Refer to the schematic on page 9. While V_{DD} and V_{DDOx} are independent, V_{DD} must always be greater than or equal to V_{DDOx} .

5. Clock Inputs

The SMA inputs (CLK0/0b and CLK1/1b) can be configured to accept a differential or single-ended clock. Best phase noise performance is achieved with a low-noise, differential input clock (default configuration for both inputs) with a high input slew rate. Although most applications will use ac-coupled, differential inputs and thus not require any board modifications, for other input termination options, see [Table 5](#) below for component and termination voltage changes.

Table 5. Input Termination Component Map

Input Type	CLK0				CLK1				VT_CLKx JP1, JP15
	C19, C23	R8	R12	C21	C72, C73	R160	R161	C74	
ac-coupled, differential	0.1 μ F	49.9 Ω	49.9 Ω	0.1 μ F	0.1 μ F	49.9 Ω	49.9 Ω	0.1 μ F	N/C
dc-coupled LVPECL	0 Ω	49.9 Ω	49.9 Ω	0.1 μ F	0 Ω	49.9 Ω	49.9 Ω	0.1 μ F	$V_{DD} - 2$ V
dc-coupled LVDS	0 Ω	49.9 Ω	49.9 Ω	0.1 μ F	0 Ω	49.9 Ω	49.9 Ω	0.1 μ F	N/C
dc-coupled HCSL (src)	0 Ω	Remove	Remove	0.1 μ F	0 Ω	Remove	Remove	0.1 μ F	N/C
dc-coupled HCSL (end)	0 Ω	49.9 Ω	49.9 Ω	0 Ω	0 Ω	49.9 Ω	49.9 Ω	0 Ω	N/C
dc-coupled LVCMOS	0 Ω	Remove	0 Ω	1 k Ω	0 Ω	Remove	0 Ω	1 k Ω	V_{DD}
ac-coupled LVCMOS	Not Allowed								

To apply an input termination voltage (only needed for LVCMOS and dc-coupled LVPECL) connect a dc supply to Pin 2 of headers JP1 (CLK0) and/or JP15 (CLK1). [Figure 5](#) shows their location.

Two calibration traces are provided to simplify propagation delay and output-to-output skew measurements. The trace connected to the CAL_IN SMA is an exact match in length and trace geometry to the input traces (CLK0/0b, CLK1/1b). The trace connected to the CAL_OUT SMA is an exact match in length and trace geometry to the output traces (Q0/0b:Q9/9b). Details on the recommended methodology for making these measurements is provided in “[8. Making Measurements](#)” on page 10. Refer to [Figure 32. SKY53510 CEVB Schematic \(5 of 9\)](#).

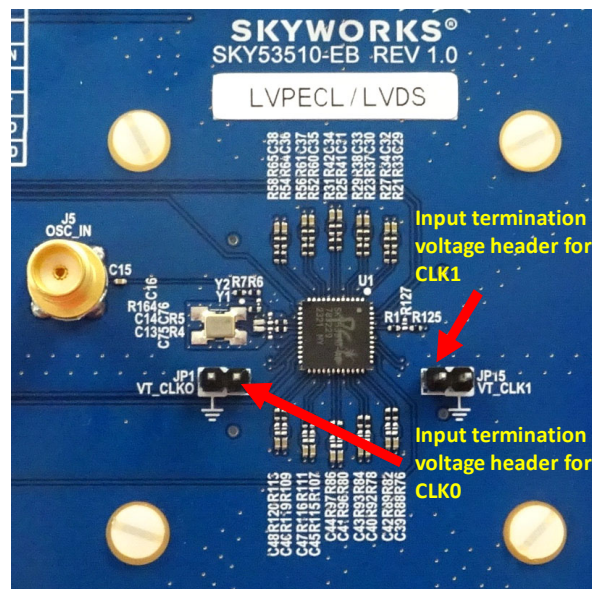


Figure 5. Location of Headers for External Input Termination Voltages

6. Crystal Oscillator Interface

The SKY53510 has an integrated crystal oscillator interface (XA/XB) that supports a fundamental mode crystal ranging from 24 to 54 MHz. If the crystal input is selected (refer to [Table 2 on page 5](#)), the onboard crystal on either footprint Y1 or Y2 will start up and the oscillator clock can be measured on any enabled output. The board default configuration includes a 3.2 x 2.5 mm 54 MHz crystal on Y1. Alternatively, a 5.0 x 3.2 mm crystal can be populated on Y2 on a merged footprint with Y1.

The crystal shunt caps (C13 = 8 pF and C14 = 6.8 pF) and the series resistor (R4 = 316 Ω) are specifically chosen for optimal performance of the TXC 7M54072001 54 MHz crystal.

Note: other crystal vendors or frequencies may require a different value of R4.

To configure a single-ended external clock input on OSC_IN (J5), remove 0 Ω resistor R164 and install a 0.1 μ F cap (or 0 Ω resistor) at C16. Note that these components share a common pad therefore only one can be installed at a time. [Figure 6](#) shows where these components are located.

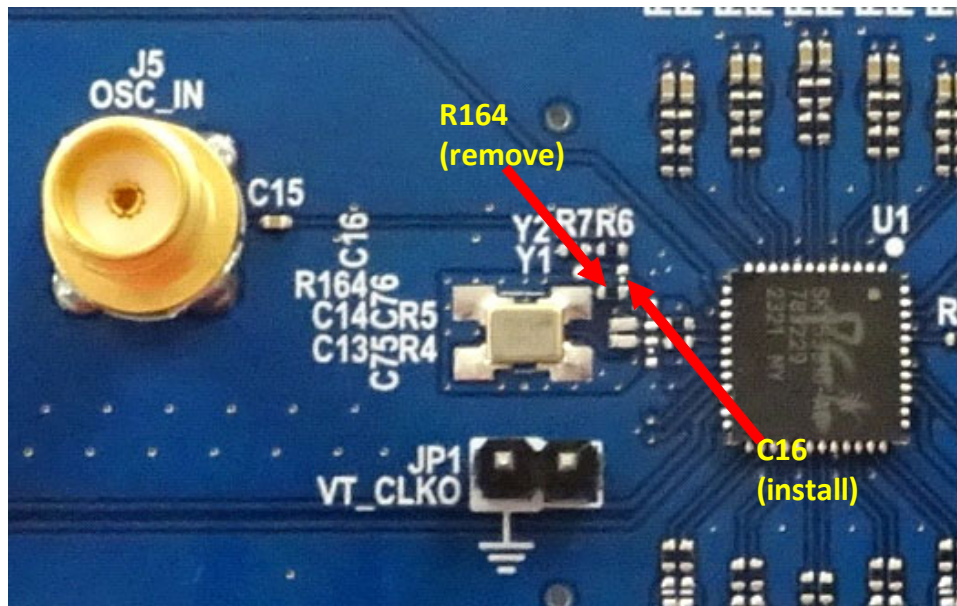


Figure 6. Component Location to Change from the Crystal to a Single-Ended External Clock (OSC_IN) on Input XA

7. Clock Outputs

By default, Bank A outputs are configured for ac-coupled 3.3 V LVPECL and source terminated with 130 Ω to Gnd. These outputs go to SMA connectors labeled Q0/0b:Q4/4b. Bank B outputs are configured for ac-coupled LVDS and therefore do not have the source pull-down resistor installed. These outputs go to SMA connectors labeled Q5/5b:Q9/9b. REFOUT is an LVCMOS output and is dc-coupled to its SMA connector

The CEVB is designed to accommodate most output formats, voltages, coupling, and terminations by installing the components shown in Table 6. Note that the components listed (R1:R7) are generic terms shown in red font on schematic pages 6 and 7. Note also that these termination configurations are intended for observing signal quality and making measurements with test equipment terminated with 50 Ω to ground. They are not necessarily the recommended part-to-part interconnect one would use when designing a board using the SKY53510. Refer to the data sheet for in-system termination recommendations.

Table 6. Output Termination Configuration for all Formats, Voltages, Coupling, and Terminations

Format	Measurement	R1	R2	R3	R4	R5	R6	R7
3.3V AC-LVPECL (default for Bank A)	Phase Noise Signal Integrity	130 Ω	0.1 μ F	NOPOP	NOPOP	0 Ω	NOPOP	0 Ω
2.5V AC-LVPECL	Phase Noise Signal Integrity	91 Ω	0.1 μ F	NOPOP	NOPOP	0 Ω	NOPOP	0 Ω
3.3V DC-LVPECL	Signal Integrity	NOPOP	0 Ω	127 Ω	82 Ω	953 Ω	0 Ω	0 Ω
2.5V DC-LVPECL	Signal Integrity	NOPOP	0 Ω	250 Ω	62 Ω	953 Ω	0 Ω	0 Ω
AC-LVDS (default for Bank B)	Phase Noise Signal Integrity	NOPOP	0.1 μ F	NOPOP	NOPOP	0 Ω	NOPOP	0 Ω
3.3 V AC-LVDS	Signal Integrity	NOPOP	0.1 μ F	137 Ω	78 Ω	953 Ω	0 Ω	0 Ω
2.5 V AC-LVDS	Signal Integrity	NOPOP	0.1 μ F	104 Ω	96 Ω	953 Ω	0 Ω	0 Ω
1.8 V AC-LVDS	Signal Integrity	NOPOP	0.1 μ F	75 Ω	150 Ω	953 Ω	0 Ω	0 Ω
DC-LVDS	Signal Integrity	NOPOP	0 Ω	NOPOP	50 Ω	953 Ω	NOPOP	0 Ω
AC-HCSL (END-TERM)	Phase Noise Signal Integrity	NOPOP	0.1 μ F	NOPOP	NOPOP	0 Ω	NOPOP	0 Ω
DC-HCSL (SRC-TERM)	Signal Integrity	50 Ω	0 Ω	NOPOP	NOPOP	0 Ω	NOPOP	33 Ω
DC-HCSL	Signal Integrity	NOPOP	0 Ω	NOPOP	NOPOP	0 Ω	NOPOP	0 Ω
Not Used	Signal Integrity	X	X	X	X	X	X	NOPOP

8. Making Measurements

There are many ways various measurements can be made, so this section is dedicated to offering recommendations on how to take advantage of some of the built-in features of the CEVB and how to configure the test setup for optimal measurements.

8.1. Supply Current

SKY53510 includes a $0.1\ \Omega$ precision in-line resistor on each voltage supply so measuring the supply current is simply a matter of measuring the voltage drop across this resistor for the given supply and applying the following equation to determine the current: $I_{DD(OX)} = V_{measured}/0.1\ \Omega$. Figure 7 and Figure 8 show the test points where each supply current can be measured.

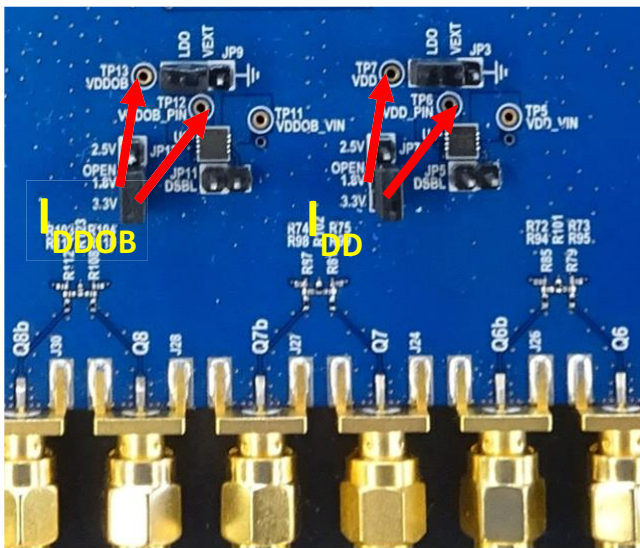


Figure 7. Test Points for Measuring I_{DD} and I_{DDOB}

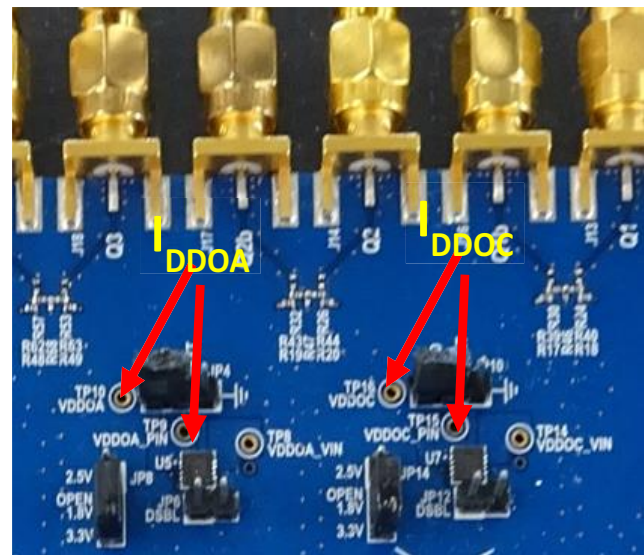


Figure 8. Test Points for Measuring I_{DDOA} and I_{DDOC}

8.2. Propagation Delay and Skew

Figure 9 shows a block diagram for measuring propagation delay and skew.

SKY53510 includes calibration traces (CAL_IN, CAL_OUT), which match the length and geometry of the SMA-to-DUT (input) and DUT-to-SMA (output) traces. The user can take advantage of these traces by simply measuring the propagation delay and output-to-output skew.

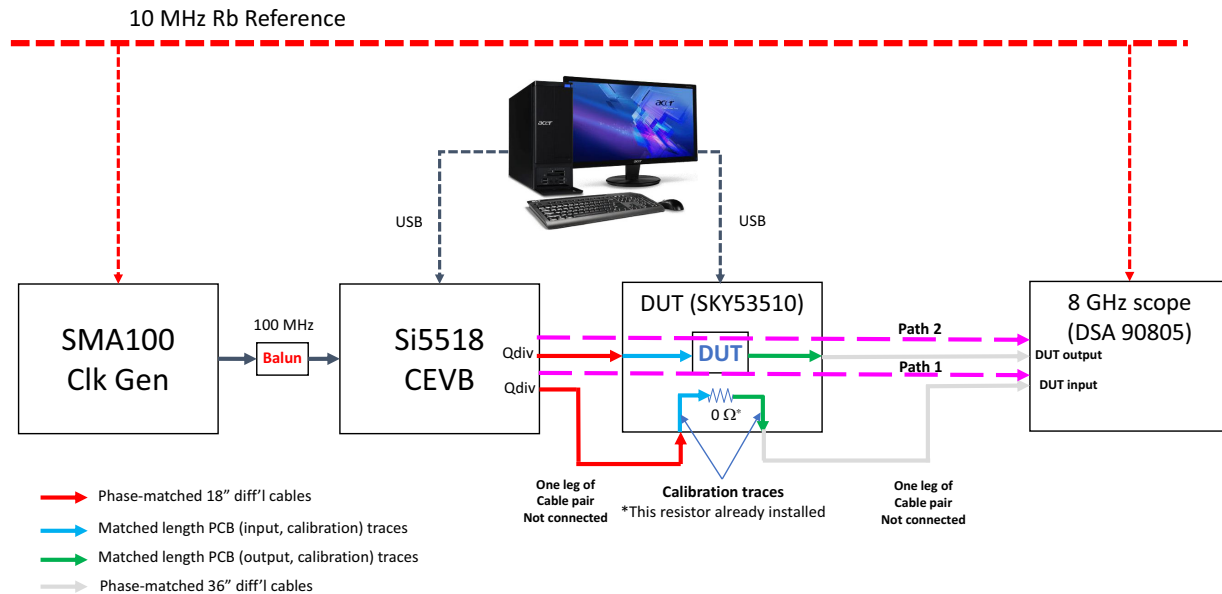


Figure 9. Block Diagram of Setup Used to Measure Propagation Delay and Skew

To make this measurement, the Si5518 CEVB is used, which provides a matched phase relationship on two Q divider LVDS outputs. Using two sets of phase/length matched differential coax cables, connect one pair to CLK0 and one to CAL_IN (this is a single-ended input, so one leg of the differential pair will not be connected). Terminate the unused LVDS output with $50\ \Omega$ to ground. Similarly, using two sets of phase/length matched differential coax cables, connect one pair from the Q output to one channel of the scope and the other from CAL_OUT to a second scope channel (again, one leg of the differential cable pair will be unconnected). Path 1 and Path 2 should now be equally matched in delay with the exception that Path 2 includes the input-to-output propagation delay of the SKY53510. Trigger the scope on the Path 1 input and measure the time delay between the two scope channels. The difference in delay is the propagation delay of the DUT plus any delay differential between the input cables, output cables, and the onboard traces, which should be quite small if the cables are equally phase matched. Figure 10 and Figure 11 show sample propagation delays for LVPECL and LVDS outputs, respectively.



Figure 10. Sample Propagation Delay for LVPECL Output

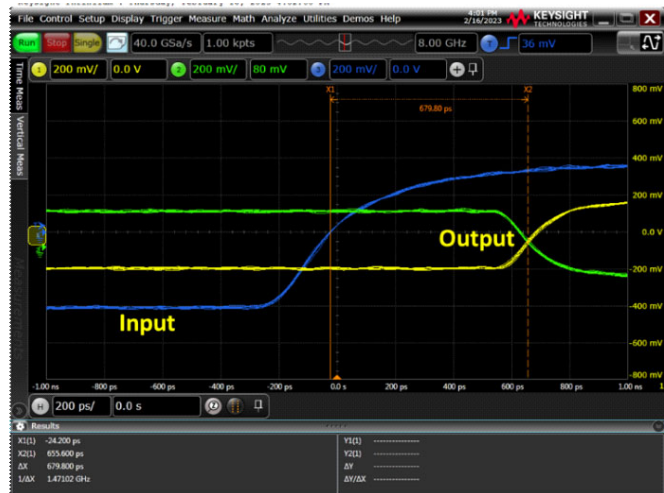


Figure 11. Sample Propagation Delay for LVDS Output

Now, to measure output-to-output skew, use a scope function which subtracts the two differential scope inputs on Path 2 and expand the vertical scale of the scope to around 5 mV/division to ensure a very sharp rising edge of this differential voltage and turn on averaging to minimize the jitter and using a scope cursor, place it on the rising edge of the Path 2 function channel. Next, move the differential cable to the next Qx/Qxb output and again place a cursor on the rising edge of the scope function channel. Continue in like fashion for all 10 outputs, keeping one cursor on the earliest rising edge and one on the latest rising edge (make sure that both banks use the same output termination configuration (as outlined in Table 6) and both use the same output format (SFOUTA[1:0] = SFOUTB[1:0])). The worst-case, output-to-output skew will then be the time delta between the earliest cursor placement and the latest cursor placement. Figure 12 and Figure 13 show sample output-to-output skews for LVPECL and LVDS outputs, respectively.

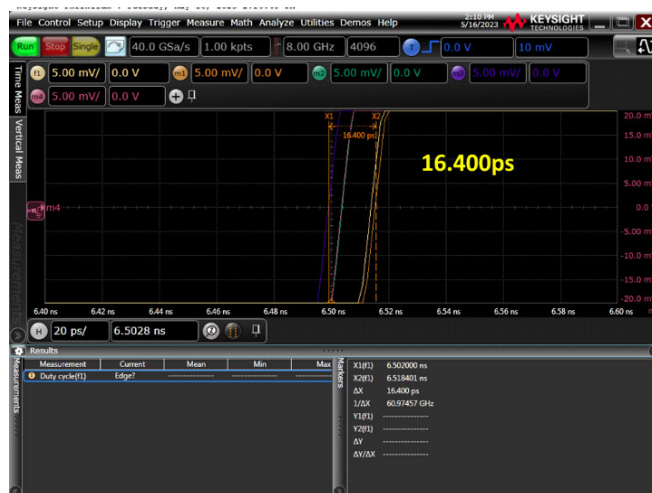


Figure 12. Sample Output-to-Output Skew for LVPECL Output



Figure 13. Sample Output-to-Output Skew for LVDS Output

8.3. Signal Integrity

There are many output formats, terminations, voltages, and coupling that SKY53510 CEVB accommodates by component modification as listed in Table 6. Signal integrity measurements that terminate $50\ \Omega$ to ground at the receiver (e.g., ac-coupled LVPECL, HCSL) can be measured full scale using the $50\ \Omega$ input setting of the scope. Measurements that terminate in $50\ \Omega$ to a voltage other than ground (e.g., dc-coupled LVPECL), or $100\ \Omega$ differentially (e.g., LVDS) can also be measured on the scope by creating a Thevenin-equivalent onboard termination followed by a series $953\ \Omega$ resistor near the SMA output that, combined with the scope's $50\ \Omega$ input creates a 20:1 probe. This effectively shows the signal integrity of the output at the point of termination (i.e., at the $953\ \Omega$ resistor). There will be some dielectric loss in the cable that will need to be calibrated for your setup. The following figures show examples of board modifications used for making signal integrity measurements for the three output formats: LVPECL, LVDS, and HCSL, along with example scope plots.

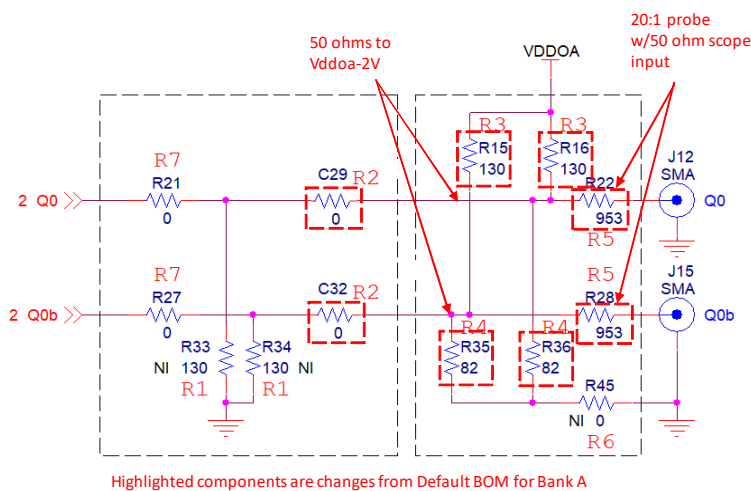


Figure 14. Board Modifications and Scope Plots for 3.3 V DC-Coupled LVPECL Output

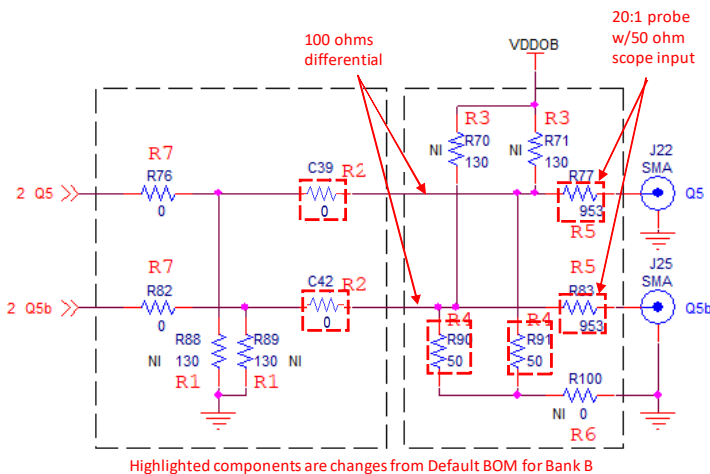
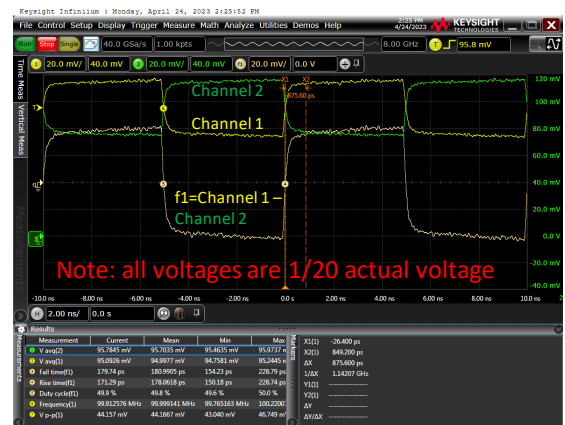
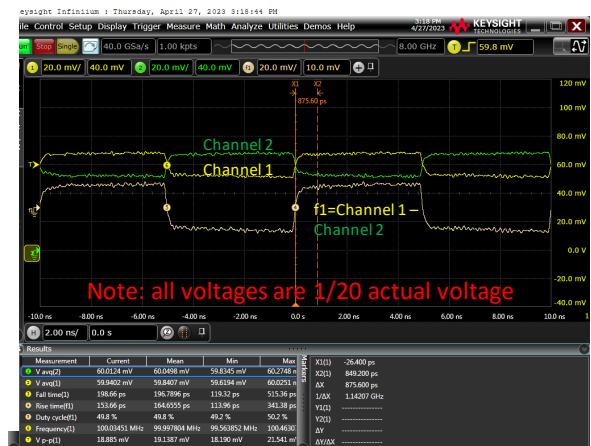


Figure 15. Board Modifications and Scope Plots for DC-Coupled LVDS Output



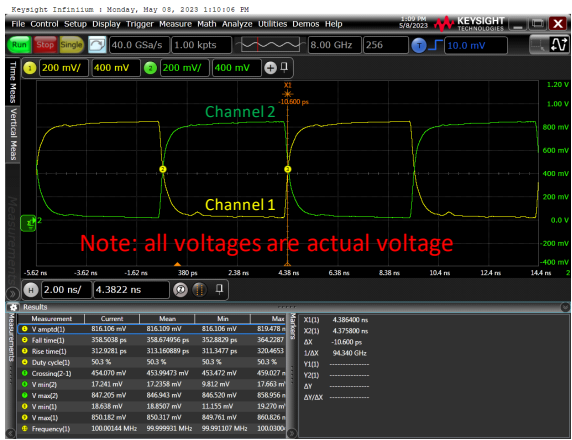
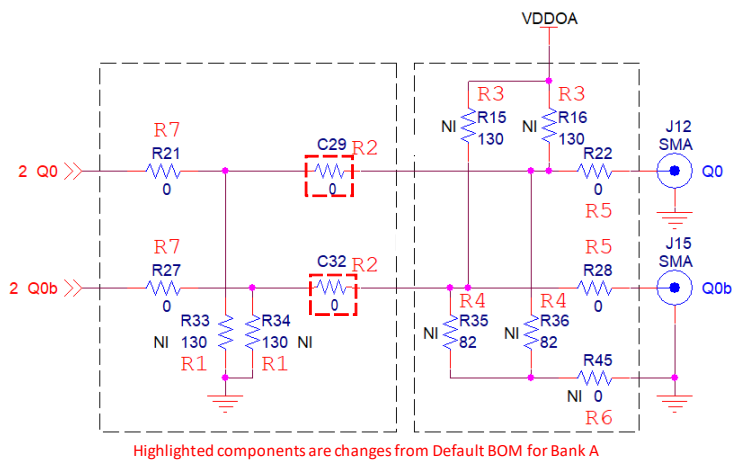


Figure 16. Board Modifications and Scope Plots for DC-Coupled End-Terminated HCSL Output

8.4. Additive Jitter

Additive jitter is dependent on several parameters of the input clock – (1) frequency, (2) slew rate, and (3) input rms jitter. To provide high slew rates with low input phase noise the input clock is driven by an Si5518 CEVB Q-divider output with 3.3 V LVPECL format at either 156.25 MHz or 625 MHz. The single-ended slew rate at 625 MHz was 2.2 V/ns and at 156.25 MHz it was 2 V/ns. One output per bank is connected to the PNA while all remaining outputs are terminated 50 Ω to Gnd at the SMA.

Figure 17 shows a block diagram of the setup used for measuring additive jitter. The board's default configuration (3.3 V ac-coupled LVPECL on Bank A and ac-coupled LVDS on Bank B) is the configuration needed for making phase noise measurements, so no alteration of the board is needed to perform these measurements. For HCSL PN measurements, modify a Bank B output to add 50 Ω resistors at the R1 position.

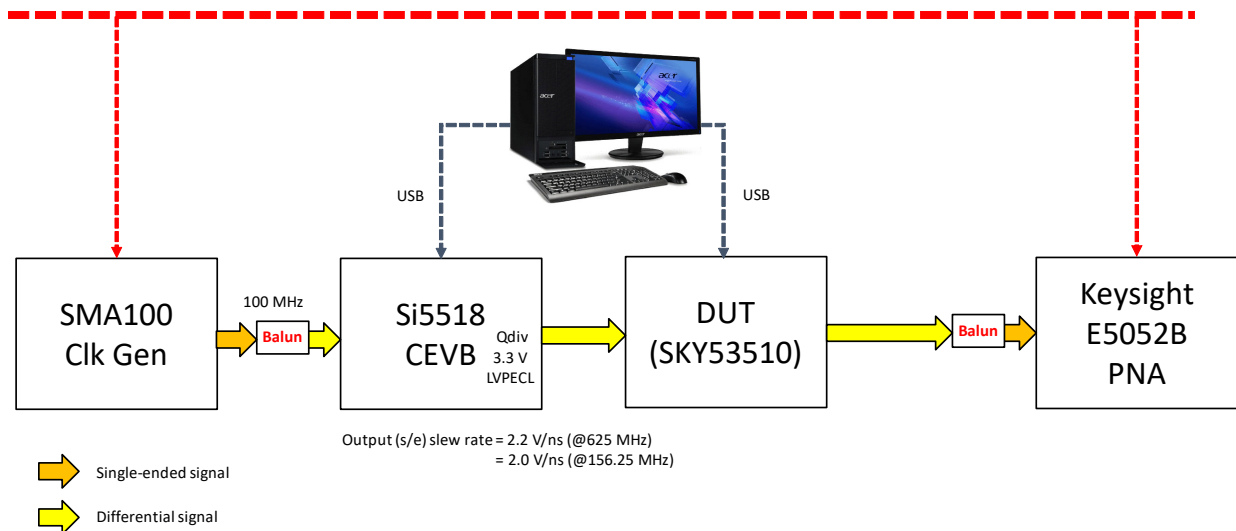


Figure 17. Block Diagram of Setup Used to Measure Additive Jitter

The following figures provide examples of additive jitter for LVPECL, LVDS, and HCSL at both 156.25 MHz and 625 MHz.

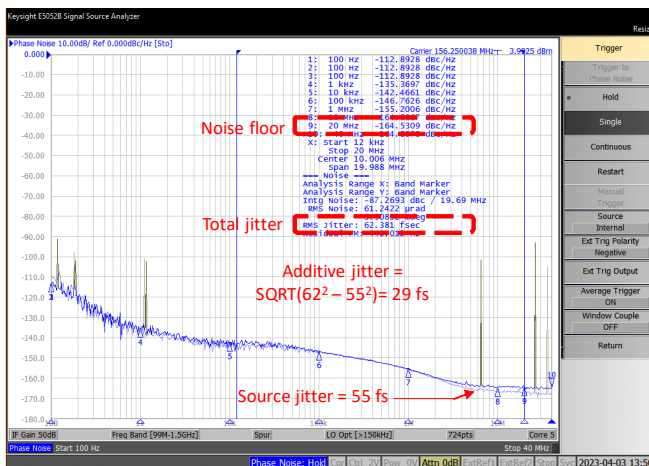


Figure 18. Sample PN Plot for 156.25 MHz LVPECL Output

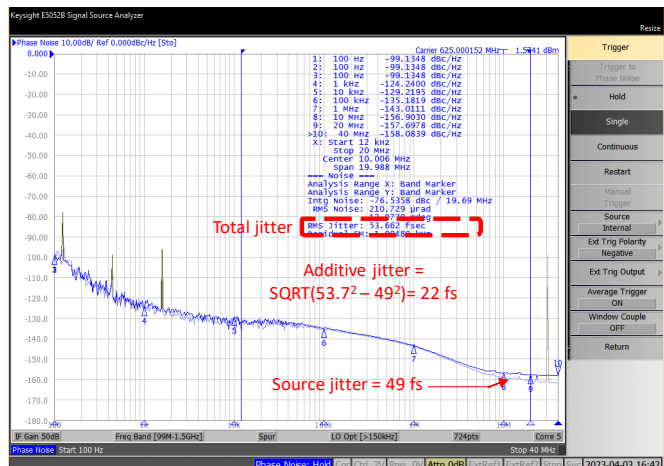


Figure 19. Sample PN Plot for 625 MHz LVPECL Output

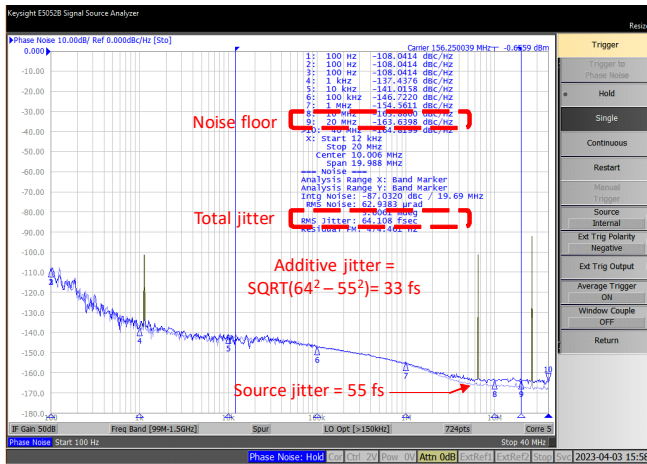


Figure 20. Sample PN Plot for 156.25 MHz LVDS Output

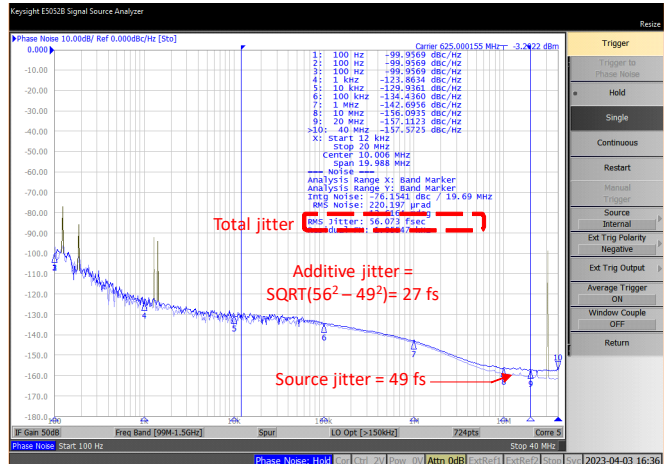


Figure 21. Sample PN Plot for 625 MHz LVDS Output

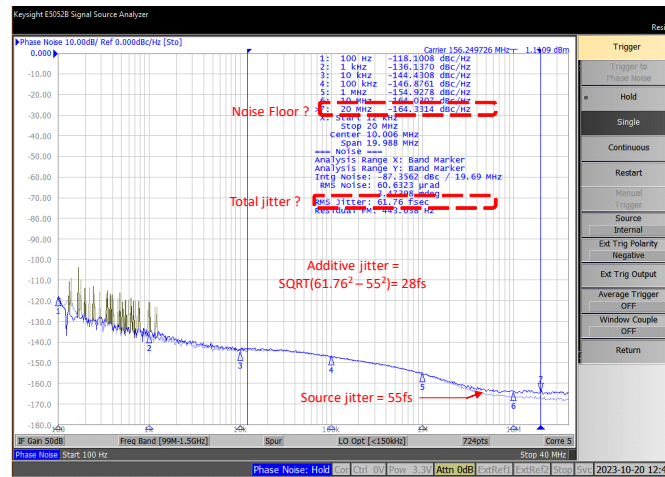


Figure 22. Sample PN Plot for 156.25 MHz HCSL Output

8.5. Input Mux Isolation

Figure 8.17 shows a block diagram of the setup used for measuring input mux isolation. A 156.25 MHz LVPECL carrier is applied to CLKIN0 by Q-divider output of Si5518 CEVB. An interfering tone at 156.25 MHz + offset freq (offsets of 10 kHz, 100 kHz, 500 kHz, and 10 MHz were used) is applied to CLKIN1 by N-divider LVPECL output of the Si5518 CEVB. The amplitude of the spur at the offset frequency applied to CLKIN1 was measured on the PNA.

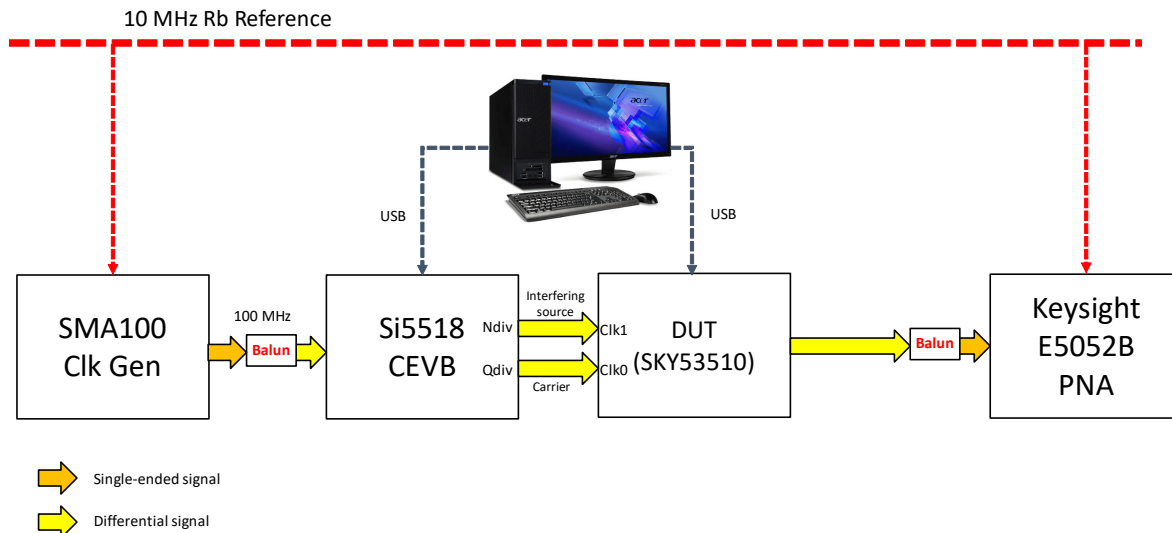


Figure 23. Block Diagram of Setup Used to Measure Input Mux Isolation

Figures 24 through 27 provide the PNA plots for the four offset noise frequencies mentioned above using the setup shown in Figure 23. Note that the interfering source could also be applied to CLK0 with the carrier applied to CLK1.

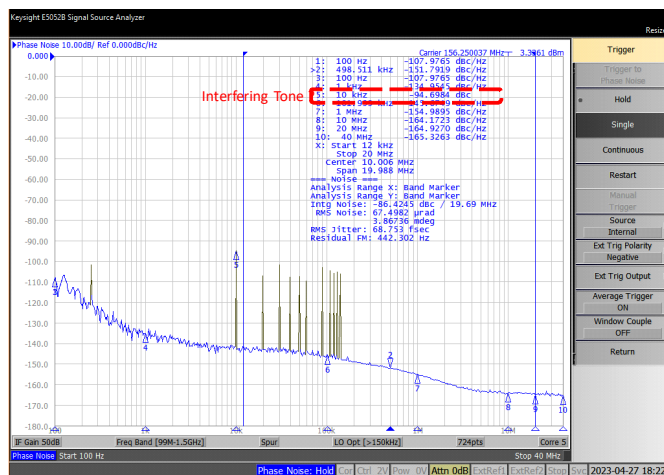


Figure 24. Sample PN Plot for Noise Source Offset = 10 kHz

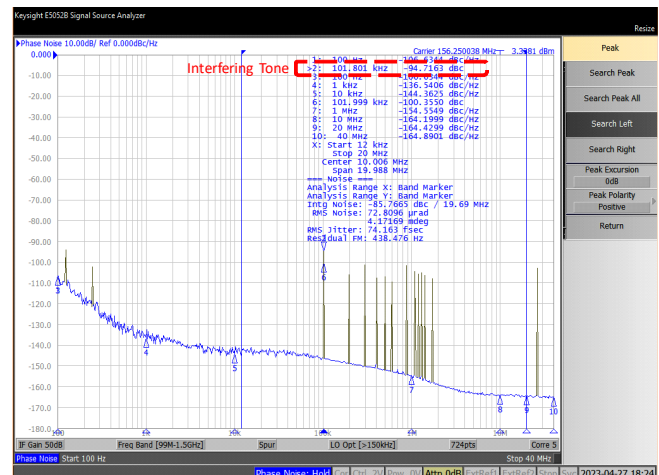


Figure 25. Sample PN Plot for Noise Source Offset = 100 kHz

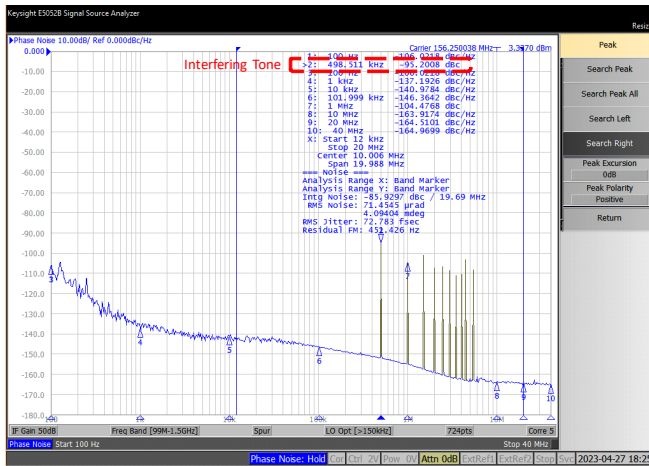


Figure 26. Sample PN Plot for
Noise Source Offset = 500 kHz

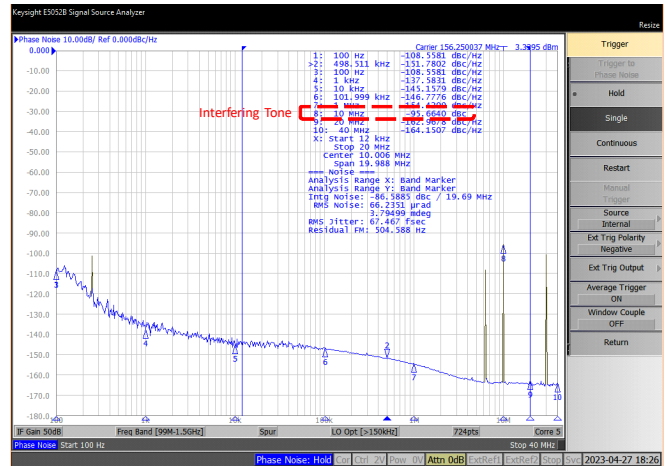


Figure 27. Sample PN Plot for
Noise Source Offset = 10 MHz

9. Schematics

The following pages include the complete schematics for SKY53510 CEVB.

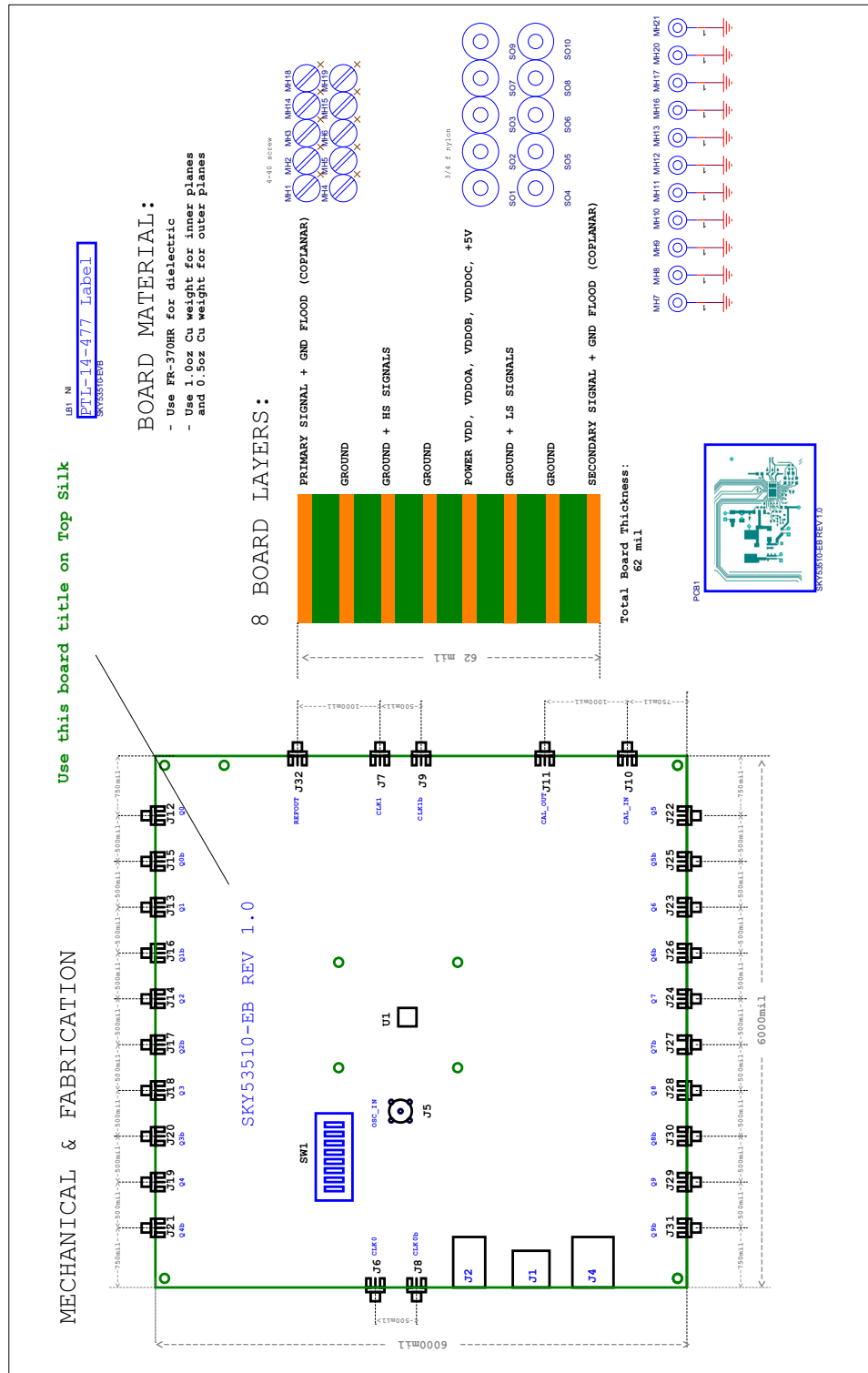
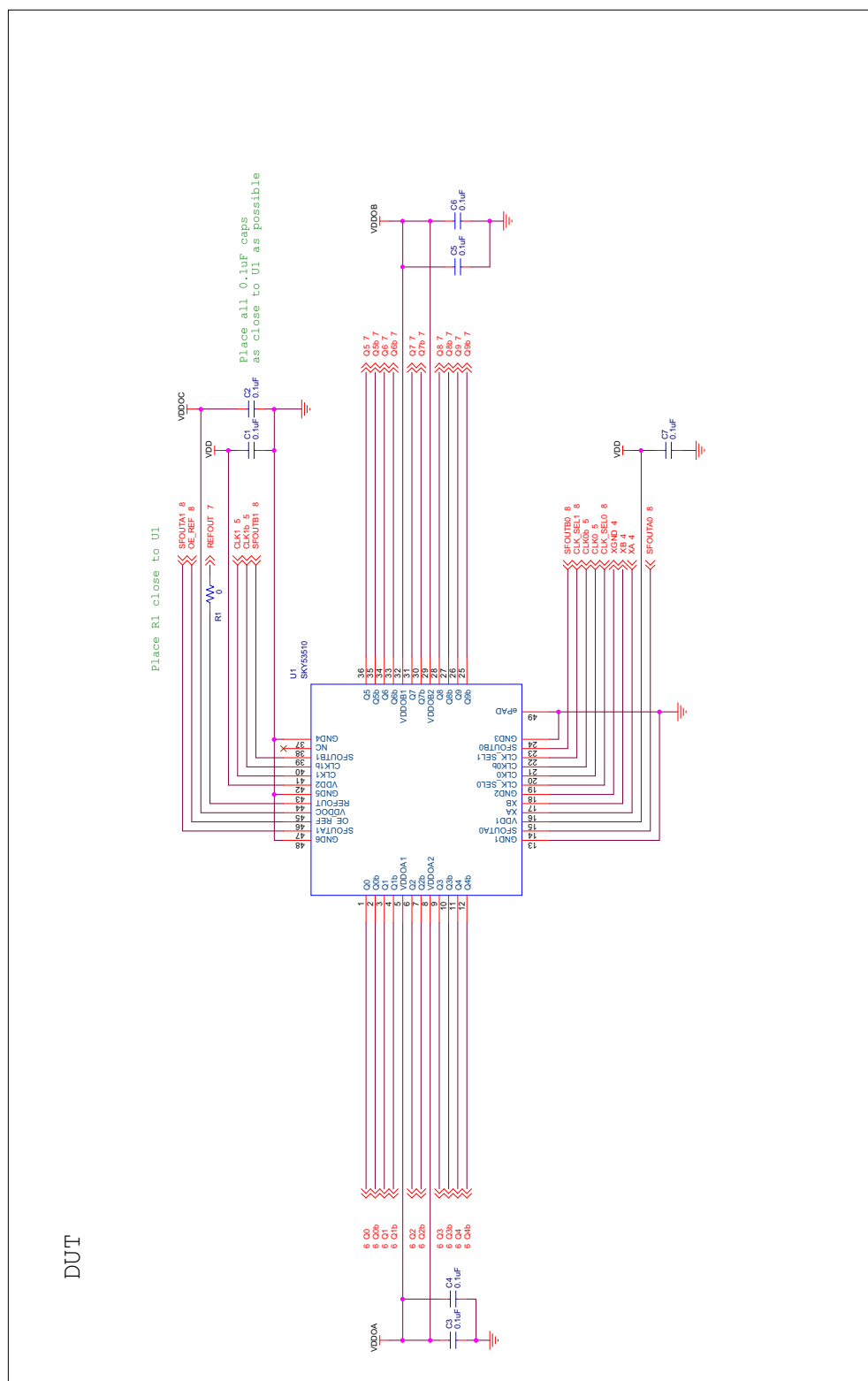


Figure 28. SKY53510 CEVB Schematic (1 of 9)



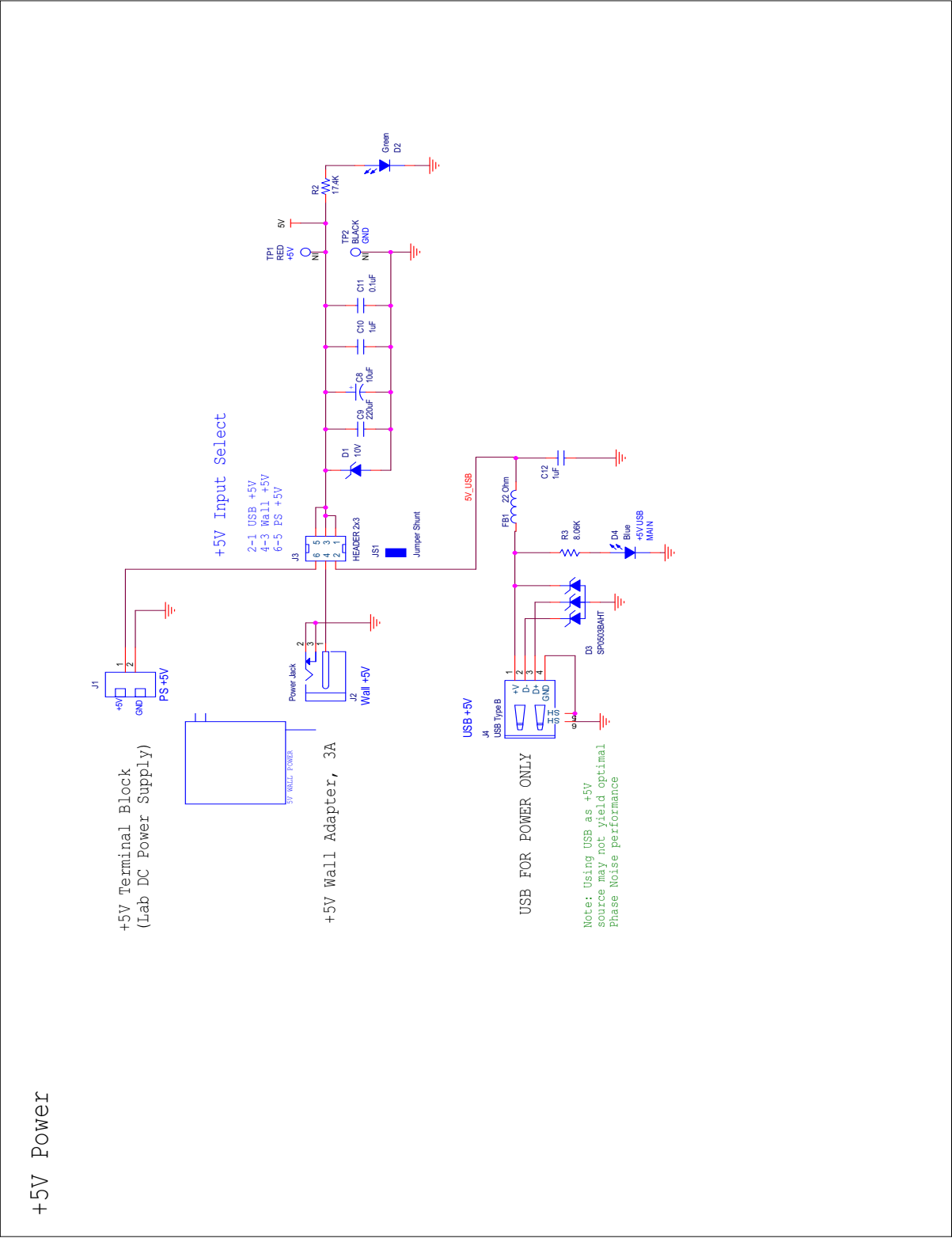


Figure 30. SKY53510 CEVB Schematic (3 of 9)

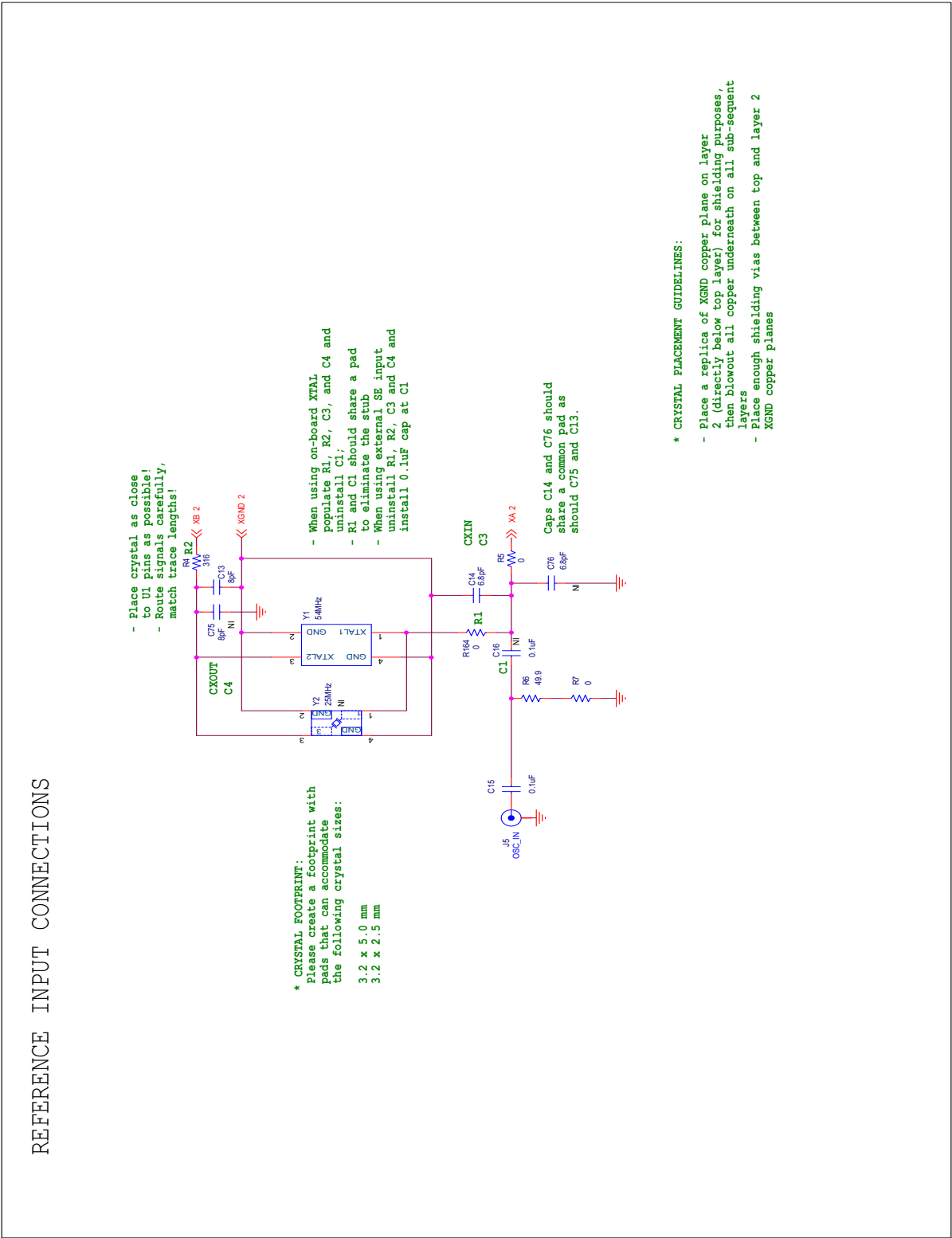


Figure 31. SKY53510 CEVB Schematic (4 of 9)

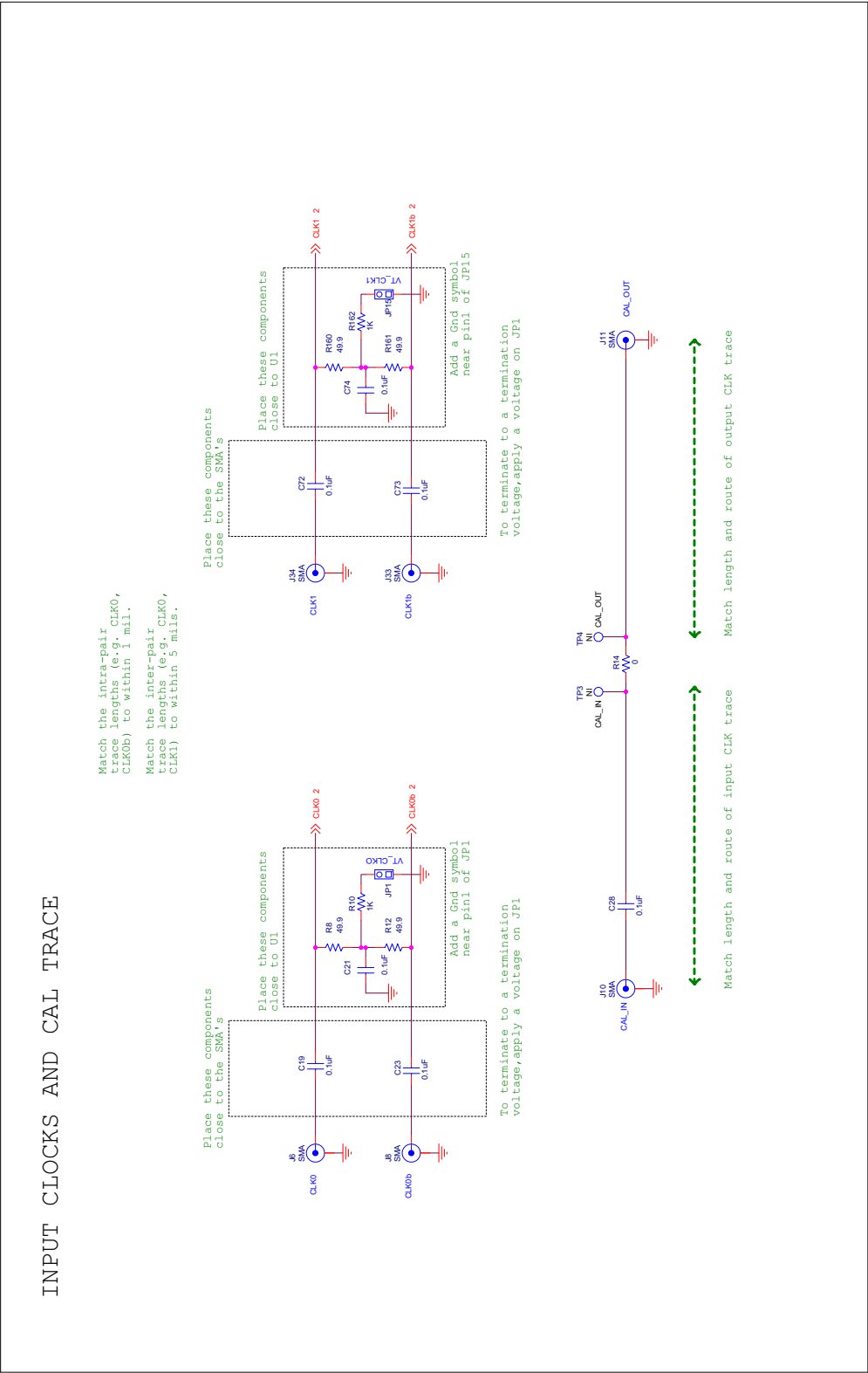


Figure 32. SKY53510 CEVB Schematic (5 of 9)

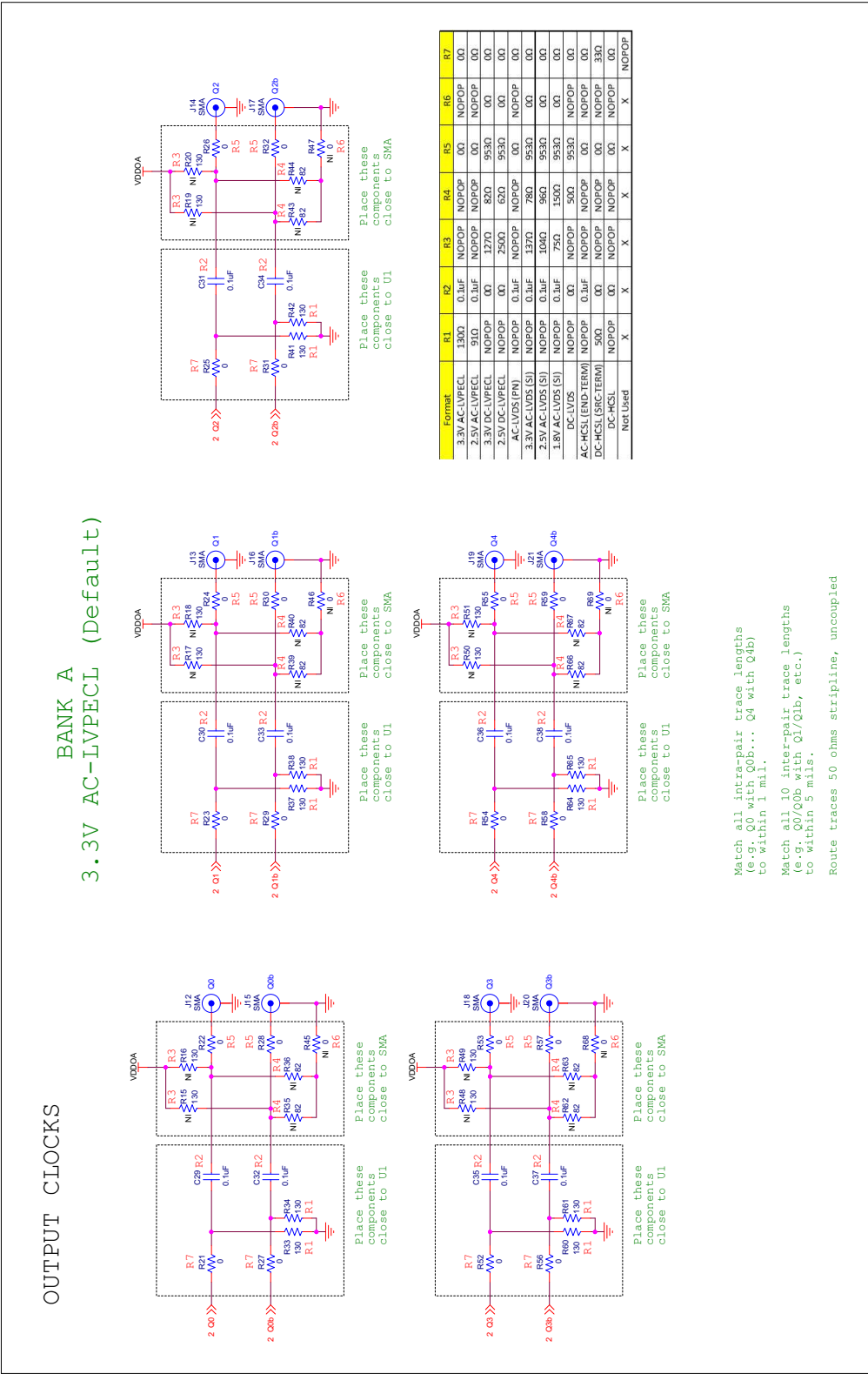


Figure 33. KY53510 CEVB Schematic (6 of 9)

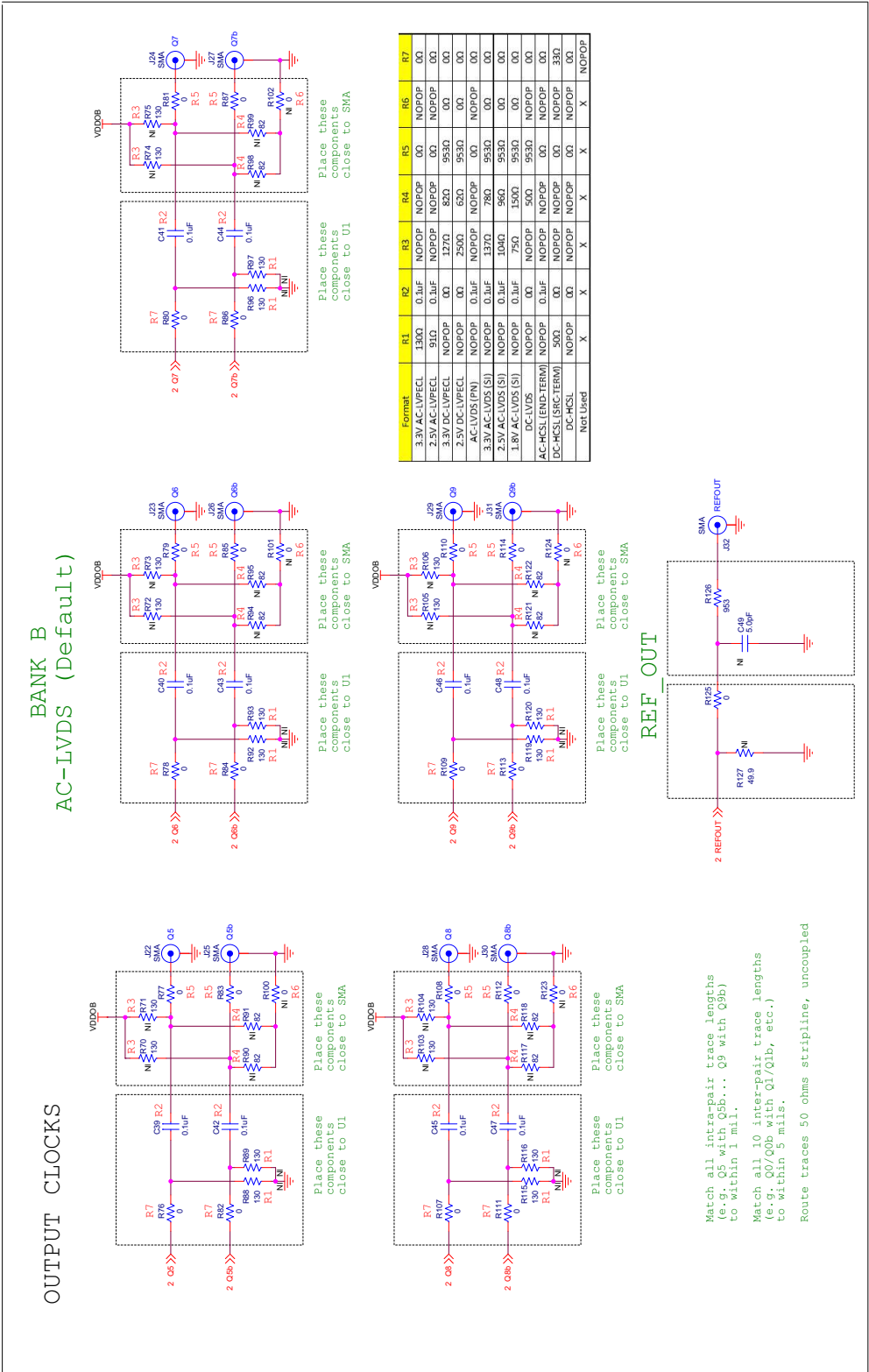


Figure 34. SKY53510 CEVB Schematic (7 of 9)

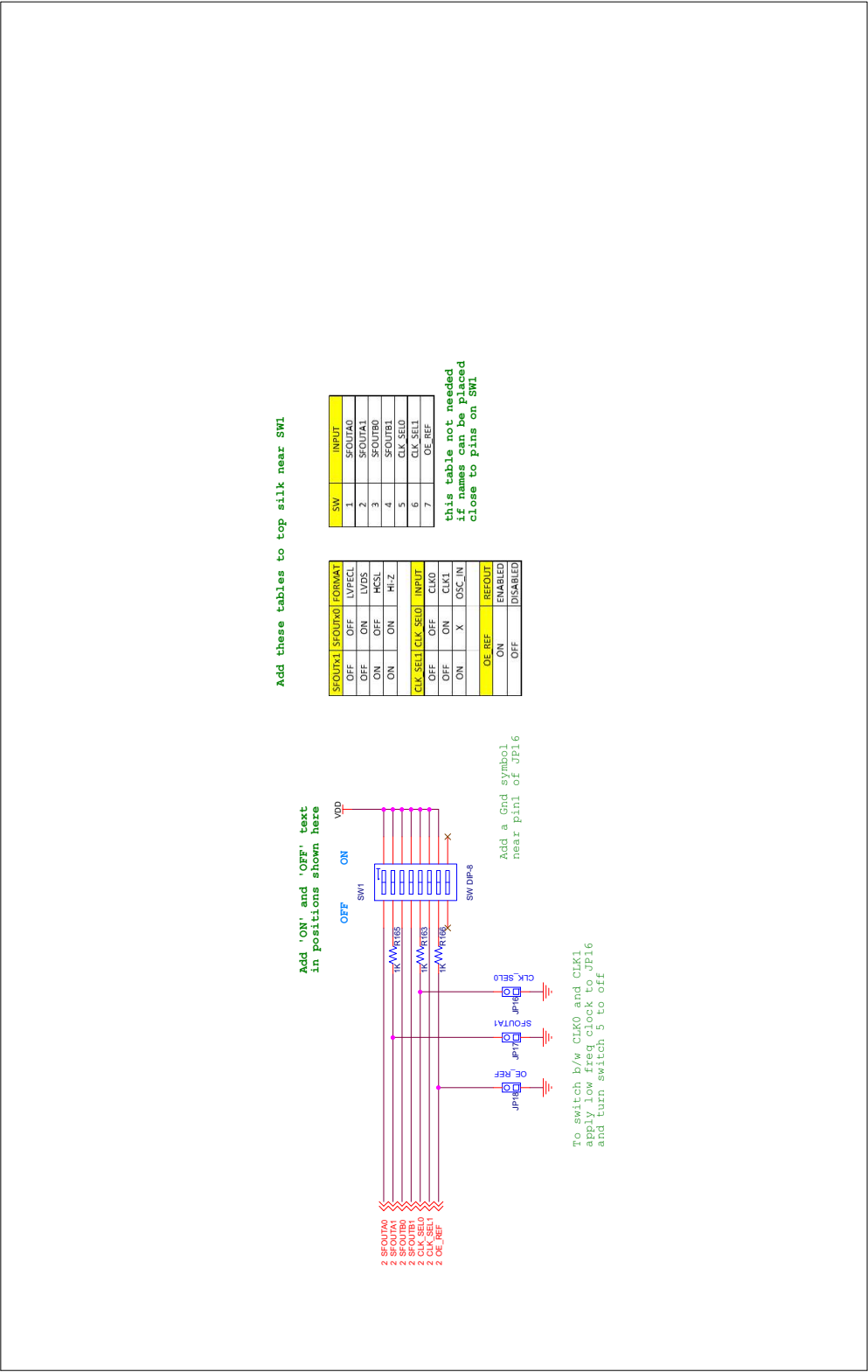


Figure 35. SKY53510 CEVB Schematic (8 of 9)

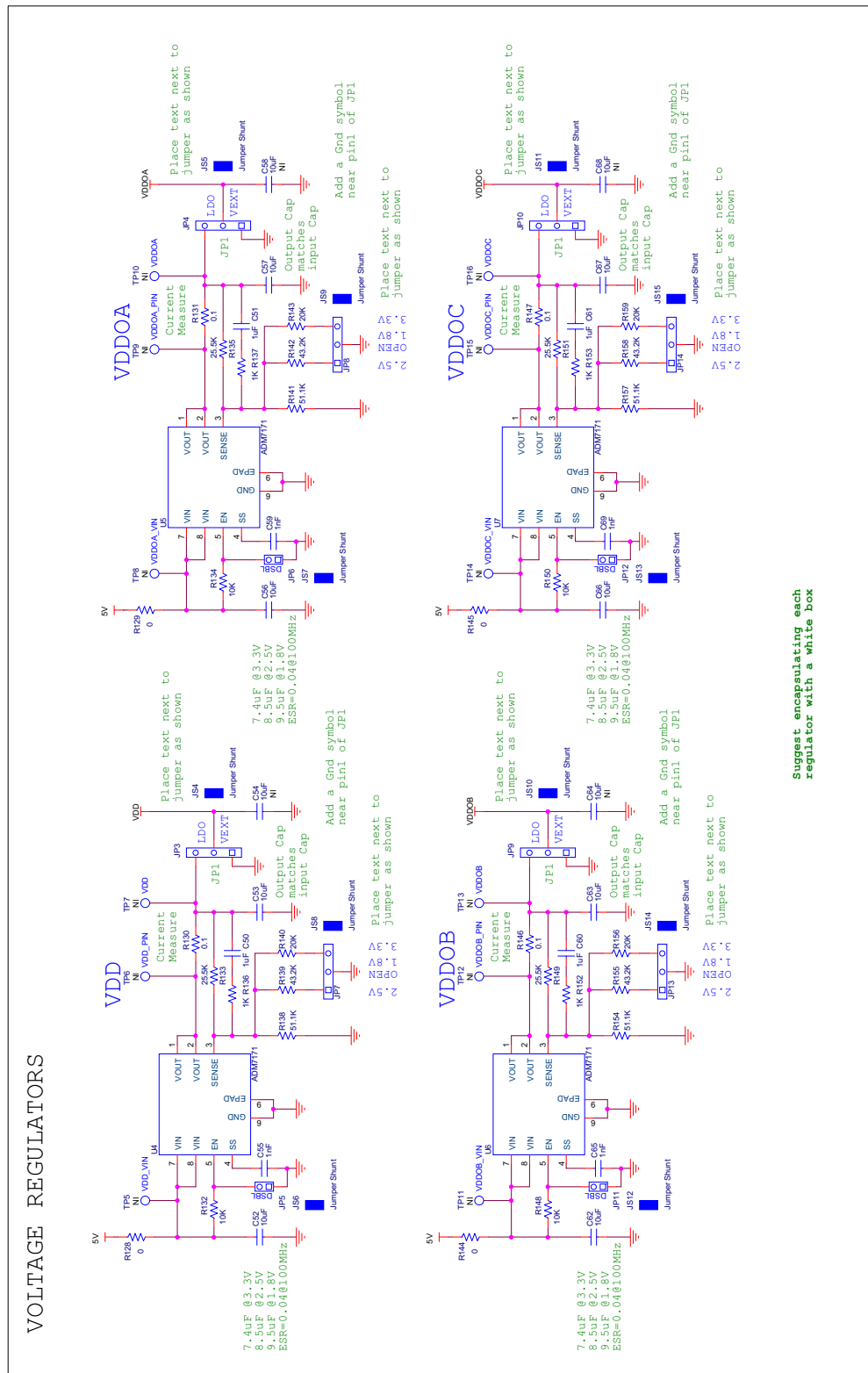


Figure 36. SKY53510 CEVB Schematic (9 of 9)

10. Bill of Materials

Table 7. SKY53510-CEVB Bill of Materials

Qty	Ref	Value	Rating	Voltage	Tol	Type	PCB Footprint	Mfr PN	Mfr
7	C1, C2, C3, C4, C5, C6, C7	0.1 μ F		16 V	$\pm 10\%$	X7R	C0402	530L104KT16T	ATC
2	C10, C12	1 μ F		16 V	$\pm 20\%$	X7R	C0805	C0805X7R160-105M	Venkel
1	C11	0.1 μ F		16 V	$\pm 10\%$	X7R	C0805	C0805X7R160-104K	Venkel
1	C13	8 pF		25 V	± 0.25 pF	C0G	C0402	C0402C0G250-8ROCNE	Venkel
1	C14	6.8 pF		25 V	± 0.5 pF	C0G	C0402 C0402L	C0402C0G2506R8D	Venkel
1	C15	0.1 μ F		10 V	$\pm 20\%$	X7R	C0402	C0402X7R100-104M	Venkel
27	C19, C21, C23, C28, C29, C30, C31, C32, C33, C34, C35, C36, C37, C38, C39, C40, C41, C42, C43, C44, C45, C46, C47, C48, C72, C73, C74	0.1 μ F		10 V	$\pm 10\%$	X7R	C0402 C0402L	C0402X7R100-104K	Venkel
4	C50, C51, C60, C61	1 μ F		10 V	$\pm 10\%$	X5R	C0603	C0603X5R100-105K	Venkel
8	C52, C53, C56, C57, C62, C63, C66, C67	10 μ F		10 V	$\pm 10\%$	X7R	C0805	C0805X7R100-106K	Venkel
4	C55, C59, C65, C69	1 nF		25 V	$\pm 10\%$	X5R	C0603	C0603X5R250-102K	Venkel
1	C8	10 μ F		25 V	$\pm 20\%$	TANT	C6032	T491C106M025ZT	Kemet
1	C9	220 μ F		6.3 V	$\pm 20\%$	X5R	C1210	C1210X5R6R3-227MNE	Venkel
1	D1	10 V	500 mW	10 V	5%	Zener	SOD-123	MMSZ4697T1G	On Semi
1	D2	Green	20 mA	3.4 V		SMT, Chip LED	LED-HSMX-C170	HSMQ-C170	Avago Technologies
1	D3	SP0503BAHT	300 mW	20 V		TVS	SOT143-AKKK	SP0503BAHTG	Littelfuse
1	D4	Blue	20 mA	3.4 V		SMT, Chip LED	LED-HSMX-C170	HSMR-C170	Avago Technologies
1	FB1	22 Ω	6000 mA			SMT	L0805	BLM21PG220SN1	Murata
1	J1	CONN TRBLK 2	24 A			Term BLK	CONN-TB-1711026	1711026	Phoenix Contact
1	J2	Power Jack	2.5 A			Barrel	CONN-3-PWR PJ-002A	PJ-002A	CUI
1	J3	HEADER 2x3				Header	CONN2X3 CONN2X3_4PIN	TSW-103-07-T-D	Samtec
1	J4	USB Type B				USB	CONN-USB-B	61729-0010BLF	FCI
1	J5	SMA				SMA	CONN-SMA-ST	142-0701-201	Johnson Components

Table 7. SKY53510-CEVB Bill of Materials (Continued)

Qty	Ref	Value	Rating	Voltage	Tol	Type	PCB Footprint	Mfr PN	Mfr
27	J6, J8, J10, J11, J12, J13, J14, J15, J16, J17, J18, J19, J20, J21, J22, J23, J24, J25, J26, J27, J28, J29, J30, J31, J32, J33, J34	SMA				SMA	SMA-SMT-50_OHM SMA-EDGE-3 SMA-SMT-50_OHM_10MIL	142-0701-851	Johnson Components
9	JP1, JP5, JP6, JP11, JP12, JP15, JP16, JP17, JP18	Header 1x2				Header	CONN1X2	TSW-102-07-T-S	Samtec
8	JP3, JP4, JP7, JP8, JP9, JP10, JP13, JP14	Header 1x3				Header	CONN-1X3	TSW-103-07-T-S	Samtec
13	JS1, JS4, JS5, JS6, JS7, JS8, JS9, JS10, JS11, JS12, JS13, JS14, JS15	Jumper Shunt				Shunt	Shunt	SNT-100-BK-T	Samtec
10	MH1, MH2, MH3, MH4, MH5, MH6, MH14, MH15, MH18, MH19	4 to 40				Screw	MH-125 MH-125NP	NSS-4-4-01	Richco Plastic Co.
1	PCB1	SKY53510-EB REV 1.0				Bare PCB	N/A	SKY53510-EB REV 1.0	Skyworks
46	R1, R5, R7, R14, R21, R22, R23, R24, R25, R26, R27, R28, R29, R30, R31, R32, R52, R53, R54, R55, R56, R57, R58, R59, R76, R77, R78, R79, R80, R81, R82, R83, R84, R85, R86, R87, R107, R108, R109, R110, R111, R112, R113, R114, R125, R164	0	1 A			Thick Film	R0402 R0402L	CR0402-16W-000	Venkel
5	R10, R162, R163, R165, R166	1 k Ω	1/16 W		$\pm 1\%$	Thick Film	R0402 R0402L	CR0402-16W-1001F	Venkel
1	R126	953 Ω	1/16 W		$\pm 1\%$	Thick Film	R0402 R0402L	CR0402-16W-9530F	Venkel
4	R128, R129, R144, R145	0 Ω	1 A			Thick Film	R0603 R0603L	CR0603-16W-000	Venkel
4	R130, R131, R146, R147	0.1 Ω	0.4 W		$\pm 0.5\%$	± 75 PPM	R0603	WSP0603R1000DEA	Vishay
4	R132, R134, R148, R150	10 k Ω	1/10 W		$\pm 5\%$	Thick Film	R0603	CR0603-10W-103J	Venkel
4	R133, R135, R149, R151	25.5 k Ω	1/16 W		$\pm 1\%$	Thick Film	R0603	CR0603-16W-2552F	Venkel
4	R136, R137, R152, R153	1 k Ω	1/16 W		$\pm 1\%$	Thick Film	R0603	CR0603-16W-1001F	Venkel

Table 7. SKY53510-CEVB Bill of Materials (Continued)

Qty	Ref	Value	Rating	Voltage	Tol	Type	PCB Footprint	Mfr PN	Mfr
4	R138, R141, R154, R157	51.1 k Ω	1/16 W		$\pm 1\%$	Thick Film	R0603	CR0603-16W-5112F	Venkel
4	R139, R142, R155, R158	43.2 k Ω	1/10 W		$\pm 1\%$	Thick Film	R0603	RC0603FR-0743K2L	Yageo
4	R140, R143, R156, R159	20 k Ω	1/10 W		$\pm 1\%$	Thick Film	R0603	CR0603-10W-2002F	Venkel
1	R2	17.4 k Ω	1/16 W		$\pm 1\%$	Thick Film	R0603	CR0603-16W-1742F	Venkel
1	R3	8.06 k Ω	1/16 W		$\pm 1\%$	Thick Film	R0603	CR0603-16W-8061F	Venkel
10	R33, R34, R37, R38, R41, R42, R60, R61, R64, R65	130 Ω	1/16 W		$\pm 1\%$	Thick Film	R0402 R0402L	CR0402-16W-131F	Venkel
1	R4	316 Ω	1/16 W		$\pm 1\%$	Thick Film	R0402 R0402L	RC0402FR-07316RL	Yageo
5	R6, R8, R12, R160, R161	49.9 Ω	1/16 W		$\pm 1\%$	Thick Film	R0402 R0402L	CR0402-16W-49R9F	Venkel
10	SO1, SO2, SO3, SO4, SO5, SO6, SO7, SO8, SO9, SO10	STANDOFF				Standoff		1902D	Keystone Electronics
1	SW1	SW DIP-8	0.1 A	50 V		DIP	SW16N9.91P2.54	219-8MST	CTS
1	U1	SKY53510				QFN	QFN48N7X7P0.5E4.7	SKY53510-A-GM	Skyworks
1	U2	WSU050-3000	15 W	5 V		MISC		WSU050-3000	Triad
4	U4, U5, U6, U7	ADM7171	1 A	1.2 V to 6.365 V		LDO	DFN8M3X3P0.5E1.65X2.38	ADM7171ACPZ-R7	Analog Devices
1	Y1	54 MHz				Quartz	XTAL4N3.2X2.5-CX3225SB	7M54072001	TXC
Not Installed Components									
1	C16	0.1 μ F		10 V	$\pm 20\%$	X7R	C0402	C0402X7R100-104M	Venkel
1	C49	5.0 pF		25 V	± 0.1 pF	C0G	C0402 C0402L	C0402C0G250-5R0BNP	Venkel
4	C54, C58, C64, C68	10 μ F		6.3 V	$\pm 20\%$	X5R	C0603 C0603L	C0603X5R6R3-106M	Venkel
1	C75	8 pF		25 V	± 0.25 pF	C0G	C0402	C0402C0G250-8ROCNE	Venkel
1	C76	6.8 pF		25 V	± 0.5 pF	C0G	C0402 C0402L	C0402C0G2506R8D	Venkel
1	LB1	SKY53510-EVB				Polyimide, White	PTL-14-717	LABEL-SKY53510-EVB	Skyworks
1	R127	49.9 Ω	1/16 W		$\pm 1\%$	Thick Film	R0402 R0402L	CR0402-16W-49R9F	Venkel
30	R15, R16, R17, R18, R19, R20, R48, R49, R50, R51, R70, R71, R72, R73, R74, R75, R88, R89, R92, R93, R96, R97, R103, R104, R105, R106, R115, R116, R119, R120	130 Ω	1/16 W		$\pm 1\%$	Thick Film	R0402 R0402L	CR0402-16W-131F	Venkel

Table 7. SKY53510-CEVB Bill of Materials (Continued)

Qty	Ref	Value	Rating	Voltage	Tol	Type	PCB Footprint	Mfr PN	Mfr
20	R35, R36, R39, R40, R43, R44, R62, R63, R66, R67, R90, R91, R94, R95, R98, R99, R117, R118, R121, R122	82 Ω	1/16 W		$\pm 1\%$	Thick Film	R0402	CR0402-16W-820FT	Venkel
10	R45, R46, R47, R68, R69, R100, R101, R102, R123, R124	0 Ω	1 A			Thick Film	R0402 R0402L	CR0402-16W-000	Venkel
15	TP1, TP3, TP4, TP5, TP6, TP7, TP8, TP9, TP10, TP11, TP12, TP13, TP14, TP15, TP16	Red				Loop	TESTPOINT	151-207-RC	Kobiconn
1	TP2	Black				Loop	TESTPOINT	151-203-RC	Kobiconn
1	Y2	25 MHz	25 $^{\circ}\text{C}$		± 30 PPM	7B SERIES	OSC4N5X3.2-FOX924	7B-25.000MAAJ-T	TXC

11. Revision History

Rev	Change Description	Date
A	Initial release	September, 2023

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