PRODUCT SUMMARY

Si469xx/xxC: High-Performance Automotive Digital Radio Coprocessor for HD Radio™, DAB/DAB+, DRM, and CDR

The Si469xx/xxC is a high-performance, multistandard, and multichannel digital radio coprocessor. Supporting up to four channels, the Si469xx/xxC enables reception, decode, and playback of HD Radio, DAB/DAB+/DMB, DRM, or CDR digital radio broadcasts by demodulating RF signals, decoding encoded audio, and seamlessly linking multiple audio streams to minimize the effects of switching between digital and analog AM/FM streams from multiple antennas. The Si469xx/xxC supports HD Radio, DAB, DRM+, or CDR Maximal Ratio Combining (MRC) data services and background scan. When combined with Skyworks Si479xx Hybrid SDR tuners, system designers benefit from unparalleled scalability and configurability allowing a single PCB design to support all global regions and a full range of performance segments. A customer-programmable MCU, Digital Data Stream Interface (DDSI), Demod/Tuner Manager, two SPI/I^2C interfaces, and automatic power-on-reset and self-boot simplify hardware and software design and reduce system cost.

Applications

- OEM automotive infotainment systems
- Remote tuner modules/smart antennas
- Aftermarket car radio systems

HD Radio Features

- 2-, 3-, and 4-channel HD Radio™ coprocessor
  - Si469x1/x1C only
  - High Definition Coding (HDC) audio source decoder
  - FM HD1, HD2, HD3 multicast support
  - Station Information Service (SIS) Support
  - Program Service Data (PSD)
  - Advanced Application Services (AAS) payload for data applications
  - Automatic Audio Alignment (AAA) and IBOC Blend mode allow seamless transition between digital and analog content

DAB/DAB+ Features

- 2-/3-/4-channel coprocessor for DAB/DAB+/DMB
  - Si469x2/x2C only
  - Integrated seamless linking of up to four audio streams: FM/DAB/DAB/IP
  - FIC decoder
  - Full support for data services

DRM Features

- 2-, 3-, and 4-channel DRM coprocessor
  - Si469x4/x4C only
  - MPEG xHE-AAC and AAC audio source decoders
  - Integrated seamless linking of up to three audio streams (includes linking, time/level alignment and/or blending audio): FM/DRM+/DRM+ or AM/DRM30/DRM30 (DRM30/DRM+ linking is not supported.)
  - FAC and SDC decoder
  - Full support for data services

CDR Features

- 2-, 3-, and 4-channel CDR coprocessor
  - Si469x3/x3C only
  - Audio decoder with Dynamic Resolution Adaptation (DRA), DRA+
  - Data services

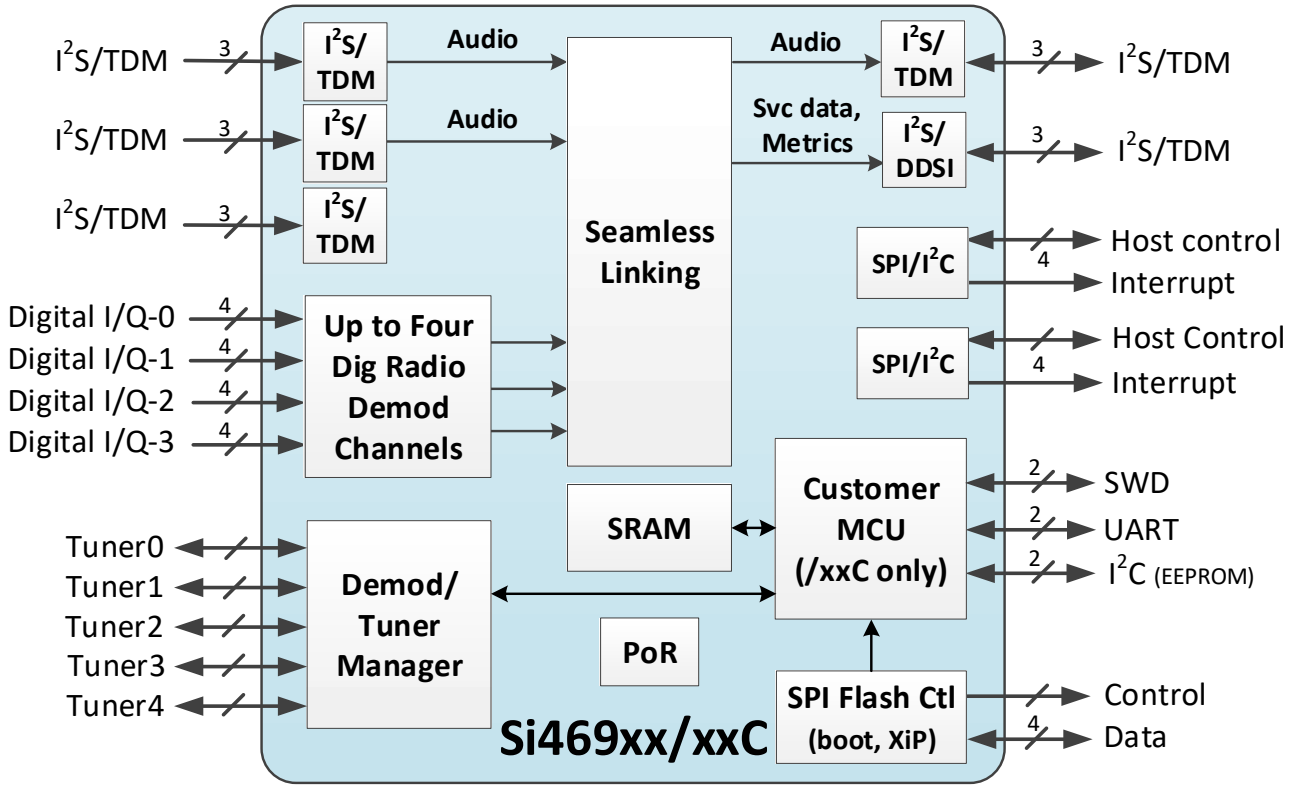
Multistandard Features

- 2-,3-, and 4-channel multistandard digital radio coprocessor
  - Si46999/99C only
  - Supports multiple standards, selectable through software packages
  - Digital radio demodulation
  - Audio decoding
  - Seamless linking

General Features

- Integrated Demod/Tuner Manager controls tuner and channel processing
- Audio Interface
  - Digital Data Stream Interface (DDSI) optimally packetizes high-payload, non-audio data (e.g., LOT/MOT) to interface to A2B™ or to a DSP over I^2S.
  - Three I^2S/TDM Audio inputs
  - Two I^2S/TDM Audio outputs
- Integrated, customer-programmable ARM® Cortex®-M3 MCU (“C” parts only)
- HD Radio, DAB, DRM+, or CDR Maximal Ratio Combining (MRC) for antenna diversity available via software package
- No external RAM needed
- Serial Flash Memory interface for application program load with support for Quad SPI flash and OTA updates
- Autonomous self-boot from flash for accelerated time-to-audio
- Support for 744.1875 kS/s (x1/x1C), 2.048 MS/s (x2/x2C), and 192 kS/s (x4/x4C)
- Two SPI/I^2C interfaces available to host MCU/SoC/A2B
- UART interface allows control of XM/SDARS
- Reference clock input
- 88-pin, 12 x 12 x 0.85 mm QFN with 0.5 mm pad pitch
- AEC-Q100 qualified
- For RoHS and other product compliance information, see the Skyworks Certificate of Conformance.

1. Functional Block Diagram



2. Pin Descriptions

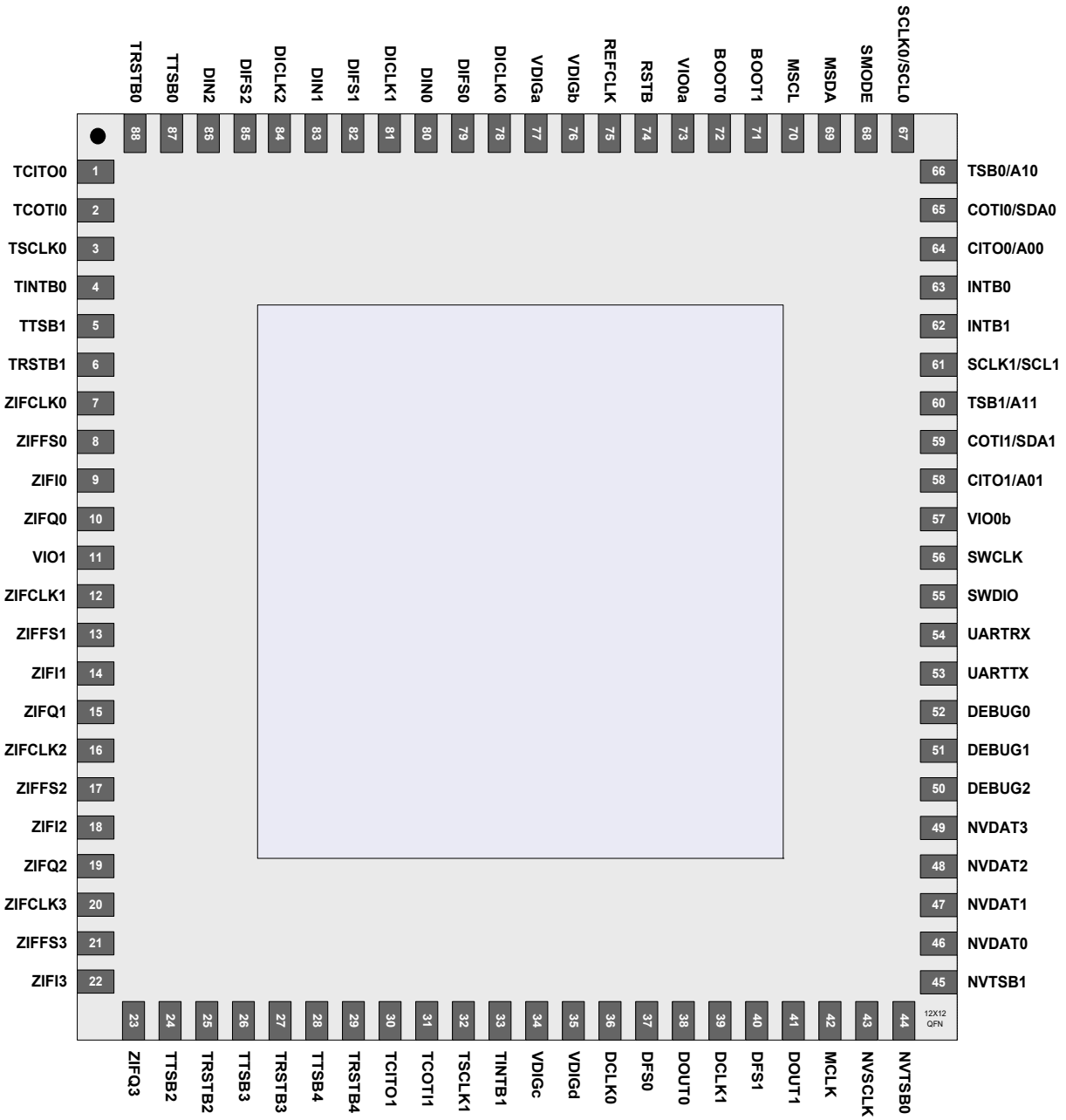


Figure 1. Si469xx/xxC Pins

Table 1. Si469xx/xxC Pin Descriptions

Pin Number	Pin Name	I/O	Power Domain	Description
1	TCITO0	I	VIO1	Tuner SPI 0 data, controller-in / target-out
2	TCOTI0	O	VIO1	Tuner SPI 0 data, controller-out/target-in
3	TSCLK0	O	VIO1	Tuner SPI 0 clock
4	TINTB0	I	VIO1	Tuner SPI 0 Interrupt, active low
5	TTSB1	O	VIO1	Tuner 1 SPI target select, active low
6	TRSTB1	O	VIO1	Tuner 1 reset, active low
7	ZIFCLK0	I	VIO1	ZIF clock input for coprocessor channel 0
8	ZIFFS0	I	VIO1	ZIF frame input for coprocessor channel 0
9	ZIFI0	I	VIO1	ZIF I-data input for coprocessor channel 0
10	ZIFQ0	I	VIO1	ZIF Q-data input for coprocessor channel 0
11	VIO1	Supply	VIO1	I/O supply for tuner interfaces
12	ZIFCLK1	I	VIO1	ZIF clock input for coprocessor channel 1
13	ZIFFS1	I	VIO1	ZIF frame input for coprocessor channel 1
14	ZIFI1	I	VIO1	ZIF I-data input for coprocessor channel 1
15	ZIFQ1	I	VIO1	ZIF Q-data input for coprocessor channel 1
16	ZIFCLK2	I	VIO1	ZIF clock input for coprocessor channel 2
17	ZIFFS2	I	VIO1	ZIF frame input for coprocessor channel 2
18	ZIFI2	I	VIO1	ZIF I-data input for coprocessor channel 2
19	ZIFQ2	I	VIO1	ZIF Q-data input for coprocessor channel 2
20	ZIFCLK3	I	VIO1	ZIF clock input for coprocessor channel 3
21	ZIFFS3	I	VIO1	ZIF frame input for coprocessor channel 3
22	ZIFI3	I	VIO1	ZIF I-data input for coprocessor channel 3
23	ZIFQ3	I	VIO1	ZIF Q-data input for coprocessor channel 3
24	TTSB2	O	VIO1	Tuner 2 SPI target select, active low
25	TRSTB2	O	VIO1	Tuner 2 reset, active low
26	TTSB3	O	VIO1	Tuner 3 SPI target select, active low
27	TRSTB3	O	VIO1	Tuner 3 reset, active low
28	TTSB4	O	VIO1	Tuner 4 SPI target select, active low
29	TRSTB4	O	VIO1	Tuner 4 reset, active low
30	TCITO1	I	VIO1	Tuner SPI 1 data, controller-in/target-out
31	TCOTI1	O	VIO1	Tuner SPI 1 data, controller-out/target-in
32	TSCLK1	O	VIO1	Tuner SPI 1 clock
33	TINTB1	I	VIO1	Tuner SPI 1 interrupt, active low
34	VDIGc	Supply	VDIG	Core/digital supply
35	VDIGd	Supply	VDIG	Core/digital supply

Table 1. Si469xx/xxC Pin Descriptions

Pin Number	Pin Name	I/O	Power Domain	Description
36	DCLK0	IO	VIO0	Host I^2S 0 clock
37	DFS0	IO	VIO0	Host I^2S 0 frame sync
38	DOUT0	O	VIO0	Host I^2S 0 data output
39	DCLK1	IO	VIO0	Host I^2S 1 clock
40	DFS1	IO	VIO0	Host I^2S 1 frame sync
41	DOUT1	O	VIO0	Host I^2S 1 data output
42	MCLK	O	VIO0	System clock for external I^2S DAC
43	NVSCLK	O	VIO0	Serial flash SPI clock
44	NVTSB0	O	VIO0	Serial flash SPI target select 0, active low
45	NVTSB1	O	VIO0	Serial flash SPI target select 1, active low
46	NVDAT0	IO	VIO0	Serial flash SPI data 0
47	NVDAT1	IO	VIO0	Serial flash SPI data 1
48	NVDAT2	IO	VIO0	Serial flash SPI data 2
49	NVDAT3	IO	VIO0	Serial flash SPI data 3
50	DEBUG2	IO	VIO0	Debug port 2
51	DEBUG1	IO	VIO0	Debug port 1
52	DEBUG0	IO	VIO0	Debug port 0
53	UARTTX	O	VIO0	UART transmit
54	UARTRX	I	VIO0	UART receive
55	SWDIO	I/IO	VIO0	Serial wire debug I/O
56	SWCLK	I	VIO0	Serial wire debug clock
57	VIO0b	Supply	VIO0	I/O supply for host interfaces
58	CITO1/A01	O/I	VIO0	Secondary host control SPI (1) data, controller-in / target-out / I^2C 1 A0 address select
59	COTI1/SDA1	I/IO	VIO0	Secondary host control SPI (1) data, controller-out / target-in / I^2C 1 data input/output
60	TSB1/A11	I	VIO0	Secondary host control SPI (1) target select / I^2C 1 A1 address select
61	SCLK1/SCL1	I	VIO0	Secondary host control SPI (1) clock input / I^2C 1 clock input
62	INTB1	O	VIO0	Host interrupt 1, active low
63	INTB0	O	VIO0	Host interrupt 0, active low
64	CITO0/A00	O/I	VIO0	Primary host control SPI (0) control in target out / I^2C 0 A0 address select
65	COTI0/SDA0	I/IO	VIO0	Primary host control SPI (0) data, controller-out / target-in / I^2C 0 data input/output
66	TSB0/A10	I	VIO0	Primary host control SPI (0) target select (active low) / I^2C 0 A1 address select
67	SCLK0/SCL0	I	VIO0	Primary host control SPI (0) clock input / I^2C 0 clock input
68	SMODE	I	VIO0	Set mode of primary host control serial port (0 = SPI, 1 = I^2C)

Table 1. Si469xx/xxC Pin Descriptions

Pin Number	Pin Name	I/O	Power Domain	Description
69	MSDA	IO	VIO0	Memory data for I^2C EEPROM
70	MSCL	O	VIO0	Memory clock for I^2C EEPROM
71	BOOT1	I	VIO0	Boot control 1
72	BOOT0	I	VIO0	Boot control 0
73	VIO0a	Supply	VIO0	I/O supply for host interfaces
74	RSTB	I	VIO0	Host controlled reset, active low
75	REFCLK	I	VIO0	Reference clock
76	VDIGb	Supply	VDIG	Core / digital supply
77	VDIGa	Supply	VDIG	Core / digital supply
78	DICLK0	I	VIO1	Tuner audio I^2S 0 clock
79	DIFS0	I	VIO1	Tuner audio I^2S 0 frame sync
80	DIN0	I	VIO1	Tuner audio I^2S 0 data input
81	DICLK1	I	VIO1	Tuner audio I^2S 1 clock
82	DIFS1	I	VIO1	Tuner audio I^2S 1 frame sync
83	DIN1	I	VIO1	Tuner audio I^2S, 1 data input
84	DICLK2	I	VIO1	Tuner audio I^2S, 2 clock
85	DIFS2	I	VIO1	Tuner audio I^2S, 2 frame sync
86	DIN2	I	VIO1	Tuner audio I^2S, 2 data input
87	TTSB0	O	VIO1	Tuner 0 SPI target select, active low
88	TRSTB0	O	VIO1	Tuner 0 reset, active low

3. Package Outline

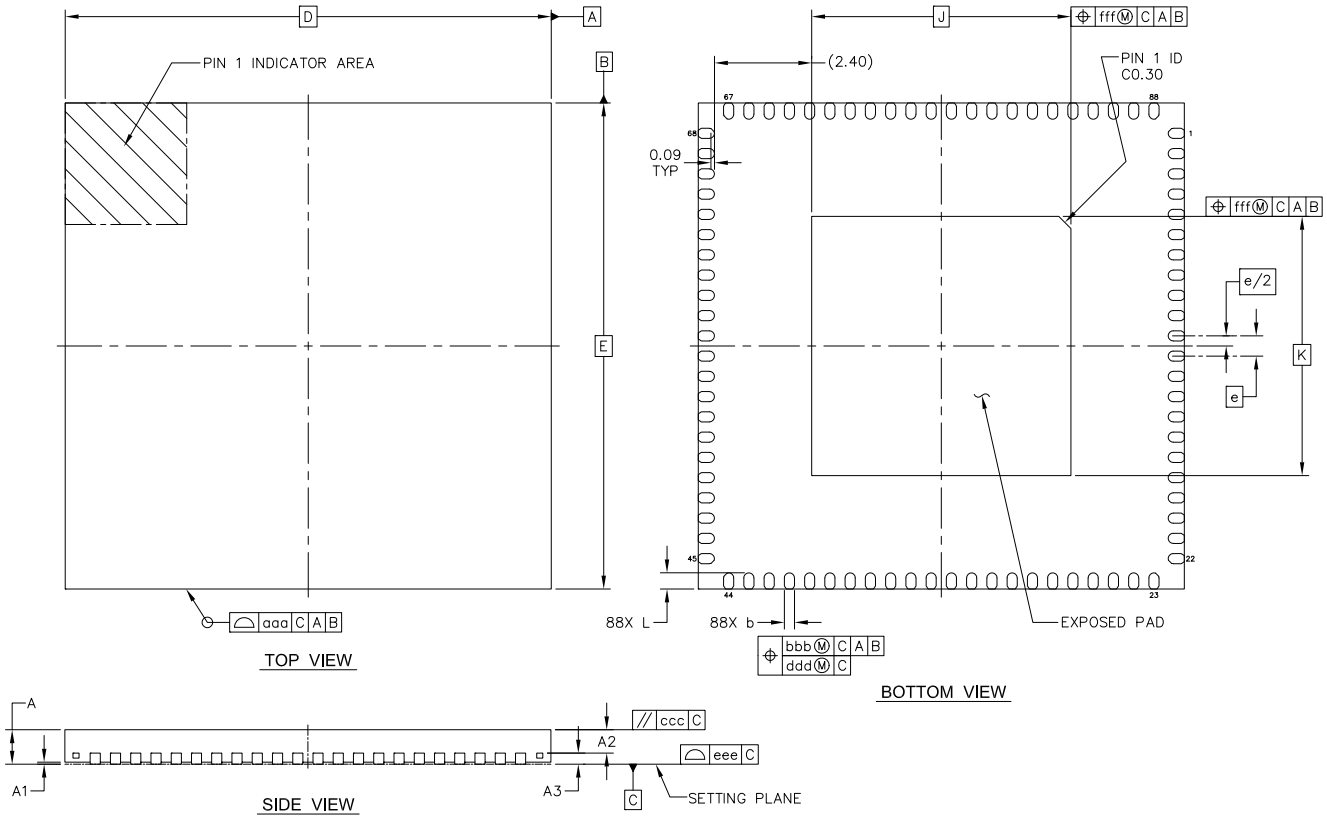


Figure 2. Package Drawing

Table 2. Package Drawing Dimensions

Dimension	Min	Nom	Max
A	0.80 mm	0.85 mm	0.90 mm
A1	0.00 mm	—	0.05 mm
A2	—	0.65 mm	—
A3	0.203 REF		
b	0.20 mm	0.25 mm	0.30 mm
D	12.00 BSC		
E	12.00 BSC		
e	0.5 BSC		
J	6.30 mm	6.40 mm	6.50 mm
K	6.30 mm	6.40 mm	6.50 mm
L	0.35 mm	0.40 mm	0.45 mm

Table 2. Package Drawing Dimensions (Continued)

Dimension	Min	Nom	Max
aaa		0.10 mm	
bbb		0.10 mm	
ccc		0.10 mm	
ddd		0.05 mm	
eee		0.08 mm	
fff		0.10 mm	

4. PCB Land Pattern

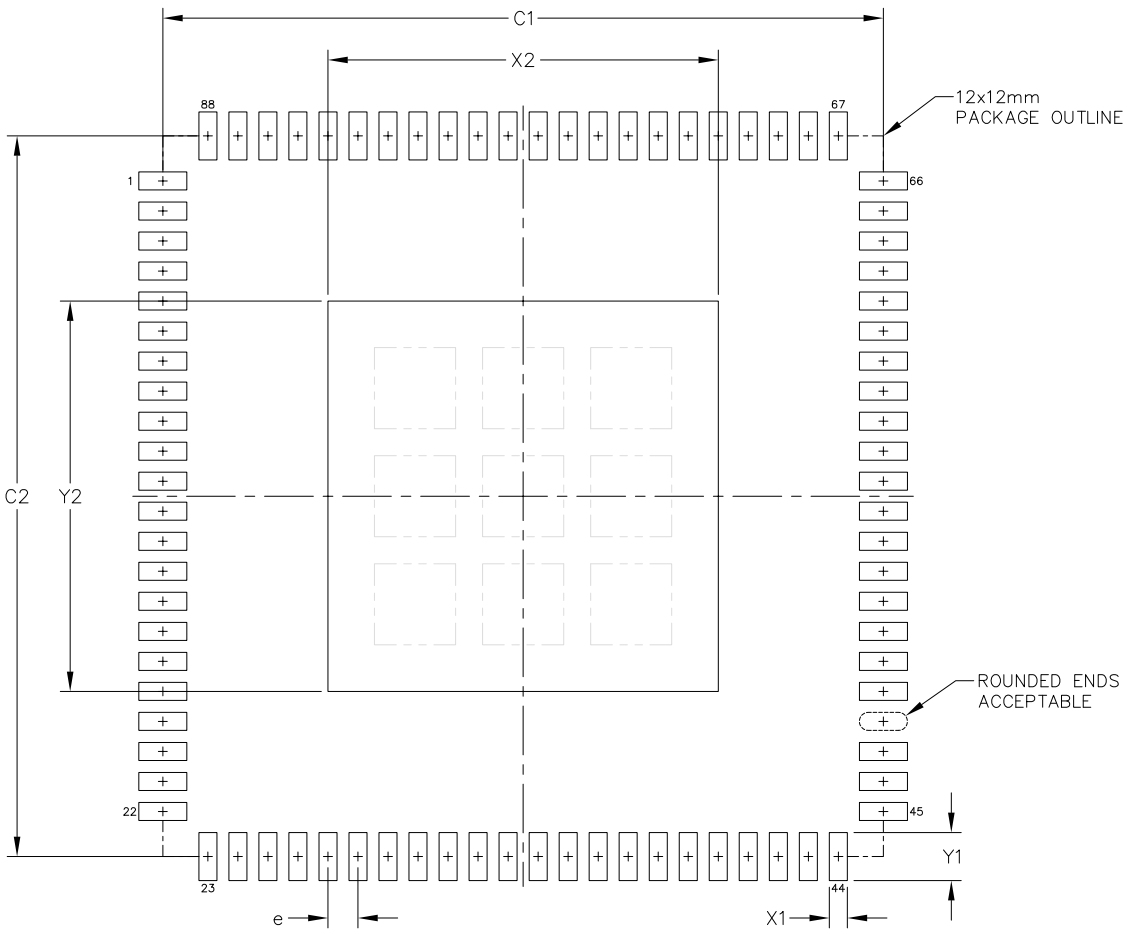


Figure 3. 88-QFN 12x12 mm PCB Land Pattern

Table 3. 88-QFN 12x12 mm PCB Land Pattern Dimensions

Dimension	Feature	mm	Notes
C1	Pad column spacing	12.00	**General** 1. All dimensions shown are in millimeters (mm) unless otherwise noted. 2. Dimensioning and Tolerancing per ASME Y14.5M. 3. This Land Pattern is based on IPC-7351 guidelines. 4. All dimensions shown are at Maximum Material Condition (MMC). Least Material Condition (LMC) is calculated based on a Fabrication Allowance of 0.05 mm. **Solder Mask Design** 1. All metal pads are to be non-solder mask defined (NSMD). Clearance between the solder mask and the metal pad is to be 0.060 mm minimum, all the way around the pad. **Stencil Design** 1. A stainless steel, laser-cut and electro-polished stencil with trapezoidal walls should be used to assure good solder paste release. 2. The stencil thickness should be 0.125 mm (5.0 mils). 3. The ratio of stencil aperture to land pad size should be 1:1 for all perimeter pads. 4. A 3x3 array of 1.35 mm square openings on a 1.80 mm pitch should be used for the center ground pad (shown in light lines above). **Card Assembly** 1. A No-Clean, Type-3 solder paste is recommended. 2. The recommended card reflow profile is per the JEDEC/IPC J-STD-020 specification for Small Body Components.
C2	Pad column spacing	12.00	
e	Pad row pitch	0.50 BSC	
X1	Pad width	0.30	
Y1	Pad length	0.80	
X2	Ground pad size	6.50	
Y2	Ground pad size	6.50	

5. Ordering Guide

5.1. Ordering Part Number Explanation

Si469abccdddAMe

- a = Number of channels supported
  - 2 = two channels
  - 3 = three channels
  - 4 = four channels
  - 9 = software defined: 2-, 3- or 4-channel
- b = Digital broadcast standard
  - 1 = HD Radio
  - 2 = DAB/DAB+
  - 3 = CDR
  - 4 = DRM (DRM for AM, DRM for FM)
  - 9 = software defined: HD Radio, DAB/DAB+, CDR, and/or DRM
- cc = Revision
  - A1 = current revision
- ddd = Device designator
  - GE1 = general market device, no customer-programmable MCU
  - GC1 = general market device, with customer-programmable MCU
- e = Outer packaging
  - R = Tape and reel
  - Blank = Tray

Table 4. Ordering Guide

Part Number[1,2]	Description	Package Type	Ambient Operating Temperature
Si469x1 Part Numbers			
Si46921A1GE1AM	High-Performance, Two-Channel HD Radio Coprocessor with Seamless Blending 12 x 12 x 0.85 mm, 88-pin QFN	QFN Pb-Free	–40 to 105 °C
Si46921A1GC1AM	High-Performance, Two-Channel HD Radio Coprocessor with Seamless Blending and Customer-Programmable MCU 12 x 12 x 0.85 mm, 88-pin QFN	QFN Pb-Free	–40 to 105 °C
Si46931A1GE1AM	High-Performance, Three-Channel HD Radio Coprocessor with Seamless Blending 12 x 12 x 0.85 mm, 88-pin QFN	QFN Pb-Free	–40 to 105 °C
Si46931A1GC1AM	High-Performance, Three-Channel HD Radio Coprocessor with Seamless Blending and Customer-Programmable MCU 12 x 12 x 0.85 mm, 88-pin QFN	QFN Pb-Free	–40 to 105 °C
Si46941A1GE1AM	High-Performance, Four-Channel HD Radio Coprocessor with Seamless Blending 12 x 12 x 0.85 mm, 88-pin QFN	QFN Pb-Free	–40 to 105 °C
Si46941A1GC1AM	High-Performance, Four-Channel HD Radio Coprocessor with Seamless Blending and Customer-Programmable MCU 12 x 12 x 0.85 mm, 88-pin QFN	QFN Pb-Free	–40 to 105 °C

Table 4. Ordering Guide (Continued)

Part Number[1,2]	Description	Package Type	Ambient Operating Temperature
Si469x2 Part Numbers			
Si46922A1GE1AM	High-Performance, Two-Channel DAB/DAB+ Coprocessor with Seamless Blending 12 x 12 x 0.85 mm, 88-pin QFN	QFN Pb-Free	–40 to 105 °C
Si46922A1GC1AM	High-Performance, Two-Channel DAB/DAB+ Coprocessor with Seamless Blending and Customer-Programmable MCU 12 x 12 x 0.85 mm, 88-pin QFN	QFN Pb-Free	–40 to 105 °C
Si46932A1GE1AM	High-Performance, Three-Channel DAB/DAB+ Coprocessor with Seamless Blending 12 x 12 x 0.85 mm, 88-pin QFN	QFN Pb-Free	–40 to 105 °C
Si46932A1GC1AM	High-Performance, Three-Channel DAB/DAB+ Coprocessor with Seamless Blending and Customer-Programmable MCU 12 x 12 x 0.85 mm, 88-pin QFN	QFN Pb-Free	–40 to 105 °C
Si46942A1GE1AM	High-Performance, Four-Channel DAB/DAB+ Coprocessor with Seamless Blending 12 x 12 x 0.85 mm, 88-pin QFN	QFN Pb-Free	–40 to 105 °C
Si46942A1GC1AM	High-Performance, Four-Channel DAB/DAB+ Coprocessor with Seamless Blending and Customer-Programmable MCU 12 x 12 x 0.85 mm, 88-pin QFN	QFN Pb-Free	–40 to 105 °C
Si469x3 Part Numbers			
Si46923A1GE1AM	High-Performance, Two-Channel CDR Coprocessor with Seamless Blending 12 x 12 x 0.85 mm, 88-pin QFN	QFN Pb-Free	–40 to 105 °C
Si46923A1GC1AM	High-Performance, Two-Channel CDR Coprocessor with Seamless Blending and Customer-Programmable MCU 12 x 12 x 0.85 mm, 88-pin QFN	QFN Pb-Free	–40 to 105 °C
Si46933A1GE1AM	High-Performance, Three-Channel CDR Coprocessor with Seamless Blending 12 x 12 x 0.85 mm, 88-pin QFN	QFN Pb-Free	–40 to 105 °C
Si46933A1GC1AM	High-Performance, Three-Channel CDR Coprocessor with Seamless Blending and Customer-Programmable MCU 12 x 12 x 0.85 mm, 88-pin QFN	QFN Pb-Free	–40 to 105 °C
Si46943A1GE1AM	High-Performance, Four-Channel CDR Coprocessor with Seamless Blending 12 x 12 x 0.85 mm, 88-pin QFN	QFN Pb-Free	–40 to 105 °C
Si46943A1GC1AM	High-Performance, Four-Channel CDR Coprocessor with Seamless Blending and Customer-Programmable MCU 12 x 12 x 0.85 mm, 88-pin QFN	QFN Pb-Free	–40 to 105 °C

Table 4. Ordering Guide (Continued)

Part Number[1,2]	Description	Package Type	Ambient Operating Temperature
Si469x4 Part Numbers			
Si46924A1GE1AM	High-Performance, Two-Channel DRM Coprocessor with Seamless Blending 12 x 12 x 0.85 mm, 88-pin QFN	QFN Pb-Free	–40 to 105 °C
Si46924A1GC1AM	High-Performance, Two-Channel DRM Coprocessor with Seamless Blending and Customer-Programmable MCU 12 x 12 x 0.85 mm, 88-pin QFN	QFN Pb-Free	–40 to 105 °C
Si46934A1GE1AM	High-Performance, Three-Channel DRM Coprocessor with Seamless Blending 12 x 12 x 0.85 mm, 88-pin QFN	QFN Pb-Free	–40 to 105 °C
Si46934A1GC1AM	High-Performance, Three-Channel DRM Coprocessor with Seamless Blending and Customer-Programmable MCU 12 x 12 x 0.85 mm, 88-pin QFN	QFN Pb-Free	–40 to 105 °C
Si46944A1GE1AM	High-Performance, Four-Channel DRM Coprocessor with Seamless Blending 12 x 12 x 0.85 mm, 88-pin QFN	QFN Pb-Free	–40 to 105 °C
Si46944A1GC1AM	High-Performance, Four-Channel DRM Coprocessor with Seamless Blending and Customer-Programmable MCU 12 x 12 x 0.85 mm, 88-pin QFN	QFN Pb-Free	–40 to 105 °C
Si46999/99C Part Numbers			
Si46999A1GE1AM	High-Performance, License-Defined Coprocessor 12 x 12 x 0.85 mm, 88-pin QFN	QFN Pb-Free	–40 to 105 °C
Si46999A1GC1AM	High-Performance, License-Defined Coprocessor with Customer-Programmable MCU 12 x 12 x 0.85 mm, 88-pin QFN	QFN Pb-Free	–40 to 105 °C
Si46999A1AC1AM	High-Performance, AM/FM-only Coprocessor with Customer-Programmable MCU 12 x 12 x 0.85 mm, 88-pin QFN	QFN Pb-Free	–40 to 105 °C

1. Add an “(R)” at the end of the device part number to denote tape and reel option.
2. AM numbered devices receive full automotive quality production status, including AEC-Q100 qualification, registration with International Material Data System (IMDS), and Part Production Approval Process (PPAP) documentation. PPAP documentation is available at www.skyworksinc.com with a registered and NDA approved user account.