PRELIMINARY DATA SHEET

Si82Cx Single-Channel Isolated Gate Driver with SelVCD™ and Miller Clamp

The Si82Cx is a family of single-channel isolated gate drivers for high-power applications. These drivers can operate with a 3 V to 20 V input supply and a maximum gate driver supply voltage of 30 V. The inputs are CMOS, which provides robust noise margin.

The Si82Cx is ideal for driving power silicon MOSFETs, IGBTs, SiC FETs, and GaN FETs used in various switched power and motor control applications. These drivers utilize Skyworks' proprietary silicon isolation technology, supporting up to 6 kV_{RMS} for one minute isolation voltage. This technology enables high CMTI (200 kV/µs), lower propagation delays, little variation with temperature and age, and tight part-to-part matching. The Si82Cx family offers longer service life and higher reliability than optocoupled gate drivers.

The output stage features Selectable Variable Current Drive (SelVCD™) technology that adjusts output current between eight selectable levels, eliminating the need for gate resistors and clamping any Miller effect currents. SelVCD operates as a current source that maintains current output within a tight tolerance of the target across all operating conditions. The driver family also offers features such as Undervoltage Lockout (UVLO) and defined output states in all operating conditions.

Automotive grade is available. These products are built using automotive-specific flows at all steps in the manufacturing process to ensure the robustness and low defectivity required for automotive applications.

Applications

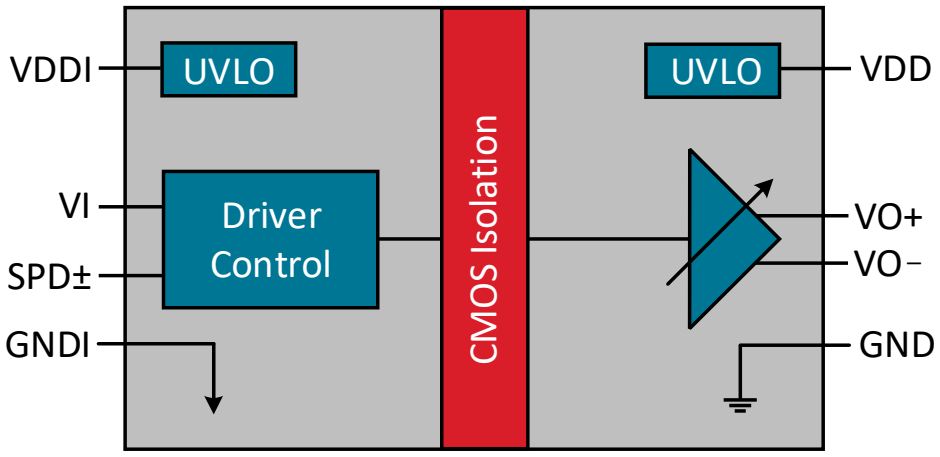
- Isolated switched-mode supplies
- Motor drives
- Power inverters
- Uninterruptable power supplies
- Onboard chargers
- DC-DC converters

Safety Regulator Approvals (Pending)

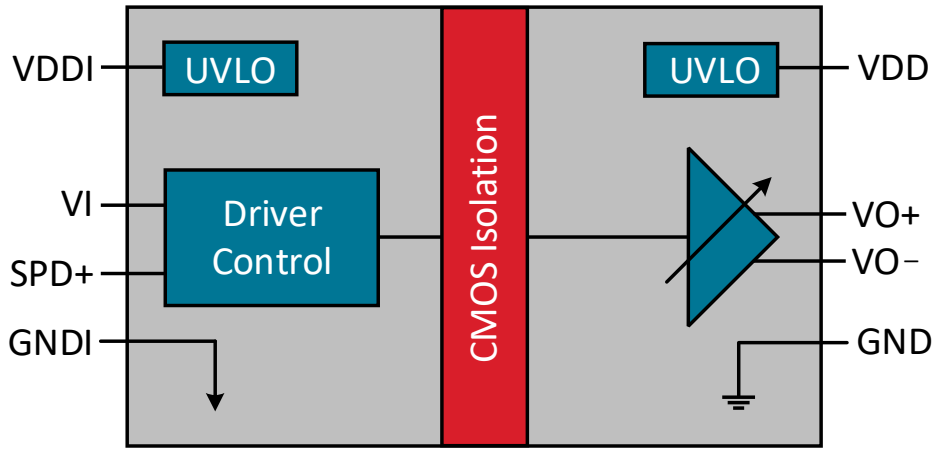
- UL 1577 recognized
  - Up to 6000 V_{RMS} for one minute
- CSA certification conformity
  - 62368-1 (reinforced insulation)
  - 60601-1 (2 MOPP)
- VDE certification conformity
  - 60747-17 (reinforced insulation)
- CQC certification approval
  - GB4943.1 (reinforced insulation)

Key Features

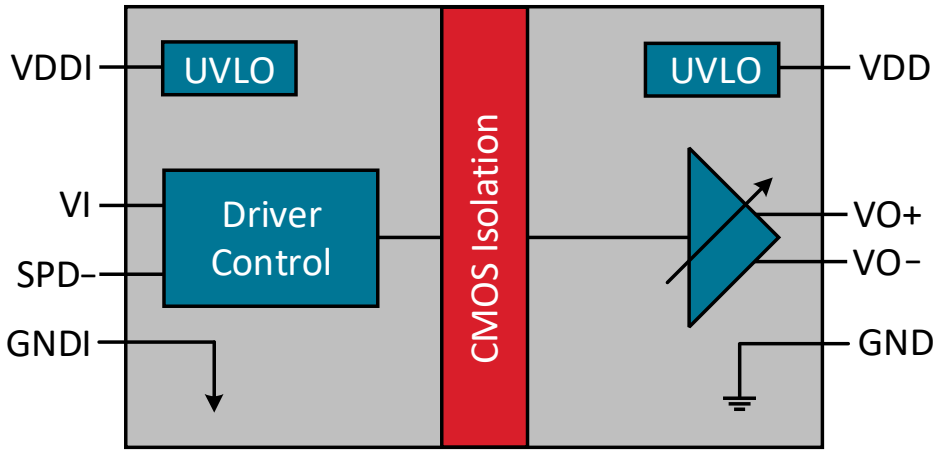
- Wide input range of 3 to 20 V.
- Wide gate supply voltage of 5 to 30 V.
- CMOS input with a selectable deglitch filter.
- Selectable Variable Current Drive (SelVCD).
- Integrated Miller clamp.
- High precision current source output.
- CMTI > 200 kV/µs.
- 1500 V_{RMS} working voltage.
- Optimized UVLO of 4 V, 8 V, 12 V, and 15 V.
- 4 kV HBM ESD rating.
- No unknown output states.
- <44 ns propagation delay with 5 ns part-to-part skew.
- 6 kV_{RMS} safety rated isolation.
- 10 kV bipolar surge.
- Wide temperature range: –40 to 125 °C.
- Narrow-body 8-pin SOIC and Stretched Small Outline (SSO) 8-pin packages.
- AEC-Q100 qualification.
- Automotive-grade OPNs available.
- For RoHS and other product compliance information, see the Skyworks Certificate of Conformance.



Si82C50x



Si82C60x



Si82C70x

1. Pin Descriptions

1.1. Device Pinouts

The Si82Cx consists of multiple die in packages with different bond-outs for different customer needs. Each bond-out corresponds to a pinout below. See “10. Ordering Guide” on page 48 for the part numbers and features of these products.

1.1.1. NB SOIC-8 Pinouts

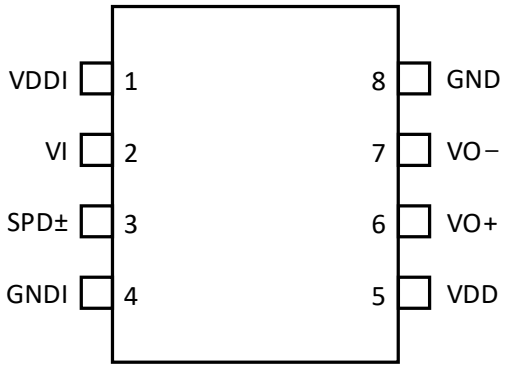


Figure 1. Si82C50x Pinout

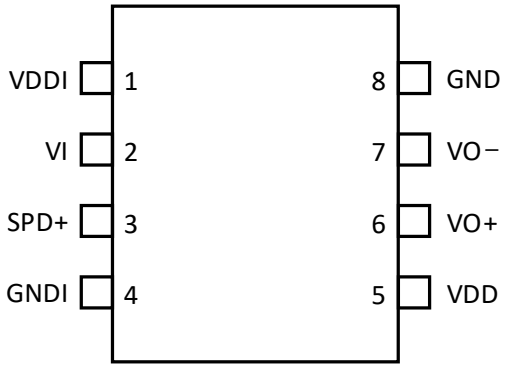


Figure 2. Si82C60x Pinout

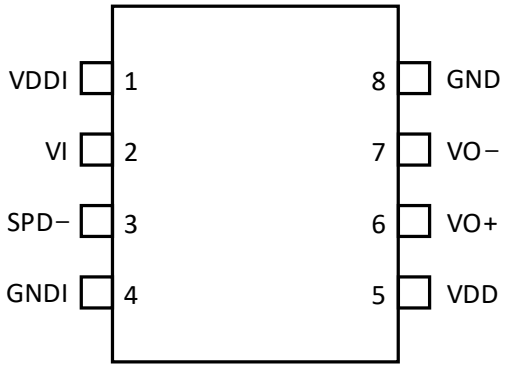


Figure 3. Si82C70x Pinout

1.1.2. SSO-8 Pinouts

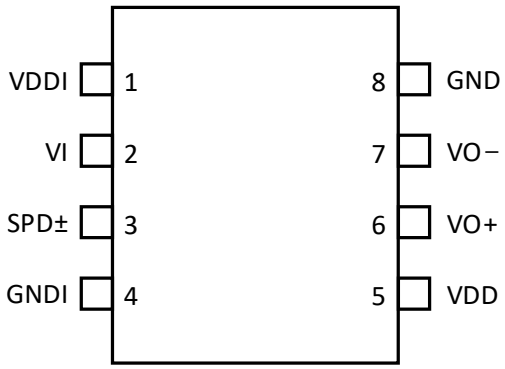


Figure 4. Si82C50x Pinout

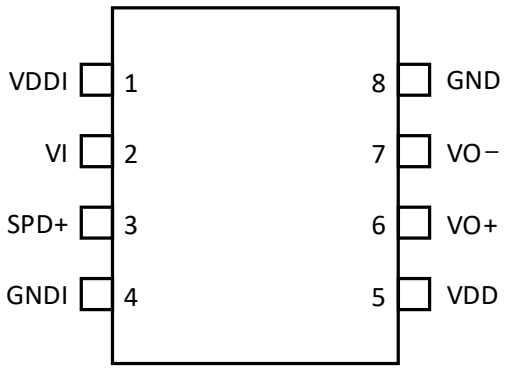


Figure 5. Si82C60x Pinout

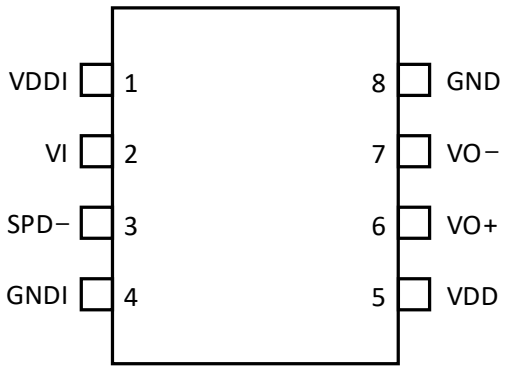


Figure 6. Si82C70x Pinout

1.2. Pin Details

Table 1. Si82Cx Pin Details

Pin Name	Pin Description
VDDI	Logic input power supply.
GNDI	Logic input ground terminal.
VI	Non-inverting logic input terminal for the gate driver.
SPD±	Driver strength programming input for the sourcing and sinking current of the gate driver. The value of the resistor connected from SPD± to GNDI sets the controlled current of the driver. Connect SPD± to GNDI to minimize the controlled current of the driver. Connect SPD± to VDDI to disable the driver and unconditionally drive output VO– to logic low output VO+ to High-Z.
SPD+	Driver strength programming input for the controlled sourcing current of the driver. The value of the resistor connected from SPD+ to GNDI sets the controlled sourcing current of the driver. Connect SPD+ to GNDI to minimize the controlled sourcing current of the driver. Connect SPD+ to VDDI to disable the driver and unconditionally drive output VO– to logic low and output VO+ to High-Z.
SPD–	Driver strength programming input for the controlled sinking current of the driver. The value of the resistor connected from SPD– to GNDI sets the controlled sinking current of the driver. Connect SPD– to GNDI to minimize the controlled sinking current of the driver. Connect SPD– to VDDI to disable the driver and unconditionally drive output VO– to logic low and output VO+ to High-Z.
VDD	Gate driver power supply.
GND	Gate driver ground terminal.
VO+	Split pull-up (sourcing) output for the gate driver.
VO–	Split pull-down (sinking) output for the gate driver.

2. Device Overview

The Si82Cx is an isolated, single-channel gate driver offered in a split output configuration. Each variant can be customized with additional features, including adjustable undervoltage lockout (UVLO) levels and configurable deglitch filter times. Refer to “10. Ordering Guide” on page 48 for more details. Safety-rated isolation is provided from logic input to gate driver output by a pair of high-voltage silicon dioxide (SiO_2) capacitors. These capacitors are duplicated to form a differential path for signals modulated with an RF carrier and using an on-off keying (OOK) modulation scheme. This optimizes for fault tolerance and timing performance between input and output.

The digital logic inputs are high-voltage capable, CMOS-compatible, Schmitt triggered, and deglitched for high noise immunity and a wide range of compatibility. See “4.4. Logic Input Signals” on page 10 for more details. The analog speed control inputs (SPD±/SPD+/SPD–) are also high-voltage tolerant and include a high-voltage clamp to protect the device’s internal low-voltage circuits. The gate driver output operates as a current source. Output current is selectable between eight different levels, eliminating the need for gate resistors and enabling a built-in Miller clamp to operate directly on the gate driver output (VO–). See 4.9. "Selectable Variable Current Drive (SelVCD)" for more information.

3. Functional Block Diagrams

Note that, in the following figures, SPD8 is equal to VDDI.

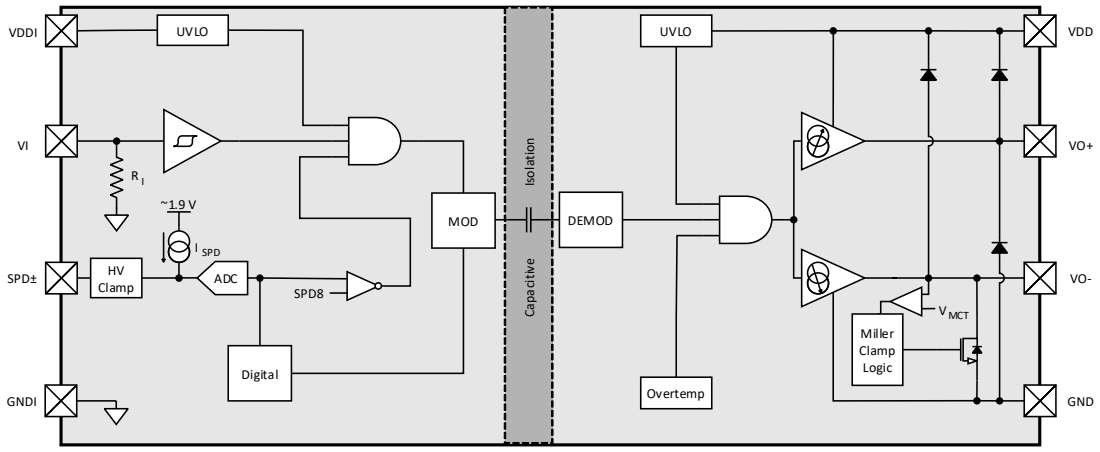


Figure 7. Si82C50x Device with Split Output and SPD± Input

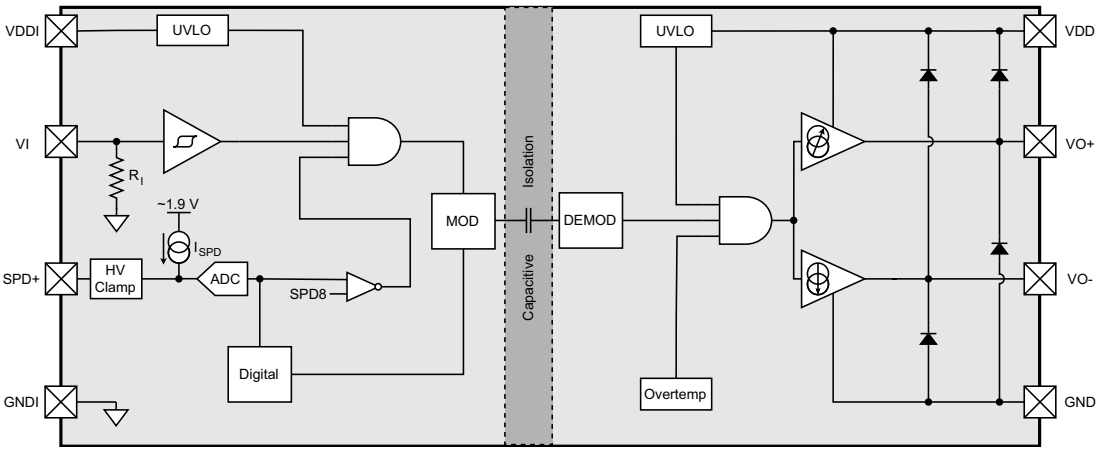


Figure 8. Si82C60x with Split Output and SPD+ Input

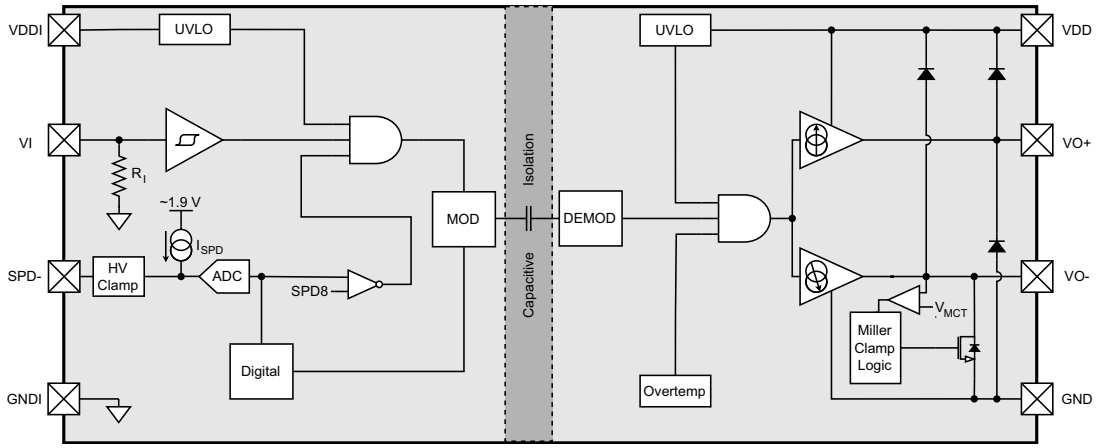


Figure 9. Si82C70x with Split Output and SPD– Input

4. Device Operation

This section describes the capabilities of the device and how it should be used to achieve different goals within a design. Refer to "5.1. Recommended Application Circuits" on page 15 and "10. Ordering Guide" on page 48 for information on how to best utilize each device for different applications.

4.1. Truth Table

The following tables describe the logical behavior of the Si82Cx Isolated Gate Driver devices.

Table 2. Si82Cx Truth Table

Inputs[1]		Power Supply State[2]		Outputs[3]	
VI	SPD[1]	VDDI[4]	VDD[5]	VO+	VO–
H	E	P	P	H	High-Z
L	X	—	—	High-Z	L
X	D	—	—	High-Z	L
X	X	—	NP	High-Z	L

1. "X" is any logic value, "H" is a logic high (true) value, and "L" is a logic low (false) value. SPD indicates the SPD±, SPD+, or SPD– pin depending on the device. "E" indicates the driver is enabled ($V_{SPD0} \leq V_{SPD} \leq V_{SPD7}$), "D" indicates the driver is disabled (V_{SPD} = VDDI). The VI pin should always be connected to either logic high or low. Logic values listed in this table are assumed to transition at the same time as the power supply state
2. "NP" is the "not powered" state; "P" is the "powered" state, and "—" is an irrelevant state.
3. "H" is a logic high (true) value, and "L" is a logic low (false). The logic low (L) value is enforced by the Shutdown Clamp (see "4.7. Shutdown Clamp" on page 11) if the gate driver's power supply (VDD) is not powered (NP).
4. "Not powered" (NP) state is defined as VDDI < $VDDI_{UV}$. "Powered" (P) state is defined as VDDI > $VDDI_{UV}$.
5. "Not powered" (NP) state is defined as VDD < VDD_{UV}. "Powered" (P) state is defined as VDD > VDD_{UV}.

4.2. Power Sequence and Timing Behavior

The device exhibits different timing behavior depending on the state of the power supplies, as well as the driver inputs. In the figure below, the analog power supply voltages are plotted against the digital input and output state of the device, with relevant device timings listed.

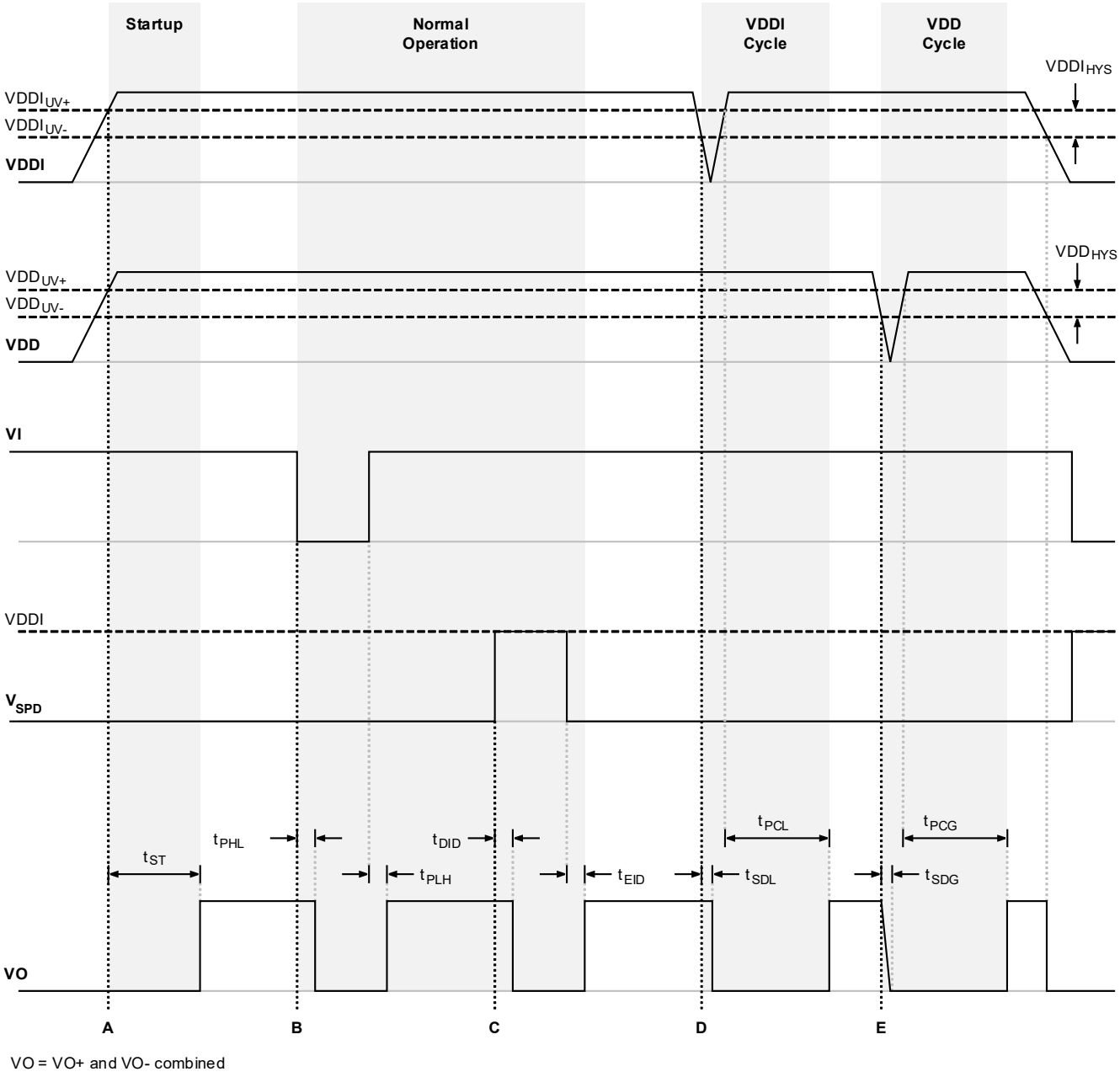


Figure 10. Gate Driver Timing Behavior

4.3. Undervoltage Lockout

Undervoltage Lockout (UVLO) is provided to prevent erroneous operation during device startup and shutdown or when VDDI or VDD is below its specified operating circuits range. The power supplies associated with the logic input and the gate driver each have undervoltage lockout monitors. The device's logic input enters UVLO when VDDI = $VDDI_{UV-}$, and exits UVLO when VDDI > $VDDI_{UV+}$. The gate driver outputs, VO/VO–, remain low and VO+ remains High-Z when the logic input supply of the device is in UVLO while its respective power supply (VDD) is within the specified range. The gate driver outputs, VO/VO–, remain low and VO+ remains High-Z when VDD falls below VDD_{UV-} and exit UVLO when VDD rises above $VDDI_{UV+}$. See "4.2. Power Sequence and Timing Behavior" on page 9 and "4.1. Truth Table" on page 8 for more details.

4.4. Logic Input Signals

4.4.1. Control Input

The VI input is a CMOS level-compatible, active-high input. When VDDI is in undervoltage lockout (UVLO), the input of this pin is ignored and the gate driver's output is pulled low. The device's output follows the VI input logic.

4.4.2. SPD±, SPD+, and SPD– Inputs

The device's SPD pin has a built-in disable function. When the SPD input is brought to VDDI, it unconditionally drives VO– low and VO+ High-Z regardless of the states of VI. Device operation terminates within t_{DID} after SPD rises to VDDI and resumes within t_{EID} after V_{SPD} falls below the maximum level of V_{SPD7}.
See "4.2. Power Sequence and Timing Behavior" on page 9 for more details. The SPD input has no effect if VDDI is below its UVLO level (i.e., VO– remains low and VO+ remains High-Z).

4.4.3. Deglitch Filter

A deglitch feature is provided on some devices. The deglitch feature ignores input noise with a duration shorter than the deglitch filter setting, but also introduces additional propagation delay. See "6.2.4. Timing Characteristics" on page 28 for the delays associated with this feature. The deglitch filter can be adjusted by selecting different product options. See "10. Ordering Guide" on page 48 for more details.

4.5. Short Circuit Clamp

The short circuit clamp is used to clamp voltages at the driver output (VO+) to slightly higher than the VDD voltage during short circuit conditions. The short circuit clamp helps protect the driven switch gate from overvoltage breakdown or degradation. The clamp is implemented by adding a diode connection between VO+ and the VDD pin inside the driver. See "6.2.3. Gate Driver Characteristics" on page 24 for detailed specifications of this clamping feature. External diodes between VO+ and VDD can increase current conduction capability as needed.

4.6. Thermal Protection

The device includes a temperature sensor in the gate driver. The sensor is monitored continuously. If the temperature exceeds the Trigger Temperature (T_{SD+}), a thermal shutdown fault will occur, and the driver will pull low. After 1 ms, if the driver temperature fails to fall below the Reset Temperature ($T_{SD–}$), the driver will pull weakly low. The driver will continuously pull weakly low until the temperature falls below $T_{SD–}$. Once the fault is removed, normal operation resumes.

4.7. Shutdown Clamp

The device includes a voltage clamp between the gate driver output (VO–) and ground (GND) when the gate driver is unpowered (VDD = High-Z). This clamp is sometimes referred to as an “active pull-down clamp”. It provides a path to ground for transient currents which could otherwise cause parasitic turn-on of a driven switch when the gate driver is unpowered. See “4.1. Truth Table” on page 8 and “6.2.3. Gate Driver Characteristics” on page 24 for details.

4.8. ESD Structure

The Si82Cx device’s I/O pin electrostatic discharge (ESD) diodes and associated supply pin ESD clamp diodes are illustrated in Figure 11, “Device ESD Structure” below. On the logic input side, a pair of ESD protection diodes are used on each input pin, and all upper diodes are connected to one shared clamp diode. This structure prevents the VDDI pin from being powered up through the input pin when the VDDI power supply is lost. The other clamp diode is present between the VDDI pin and the GNDI pin. The ESD structure of the gate driver output is similar to the logic input, except that the gate driver output’s upper ESD diode is connected to a clamp diode at the VDD pin.

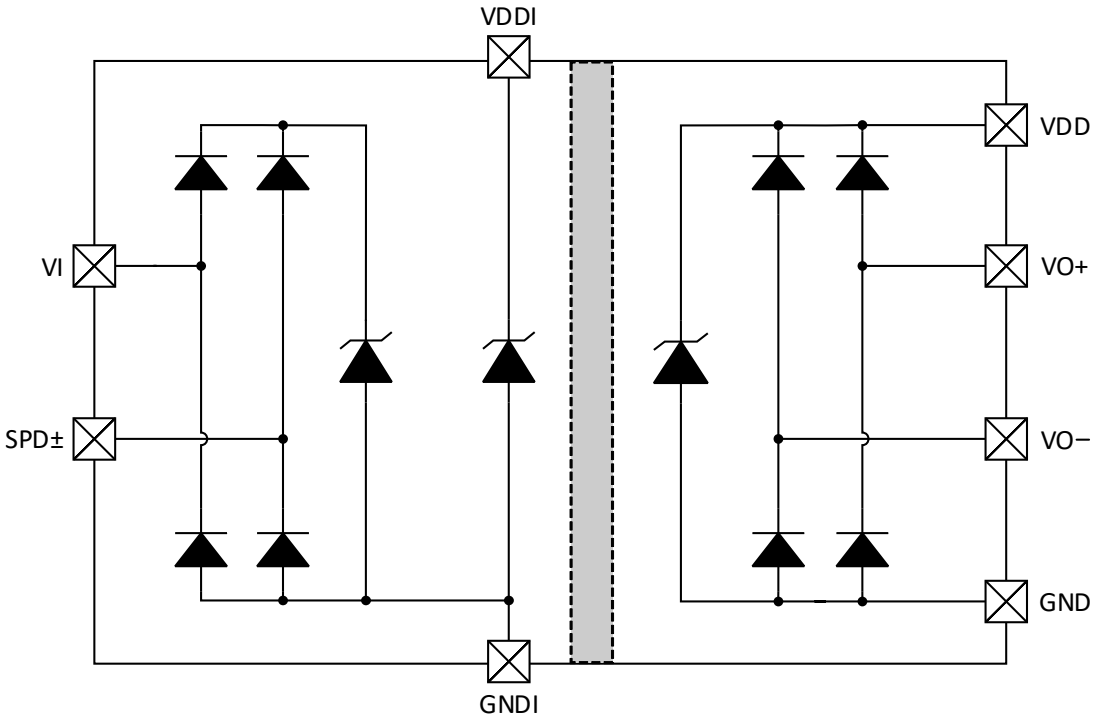


Figure 11. Device ESD Structure

4.9. Selectable Variable Current Drive (SelVCD)

The gate driver output of the device operates as a current source, maintaining the driver's output current within ±10% of the typical value over temperature and semiconductor process variation for devices with an undervoltage lockout (UVLO) level of 8 V, 12 V and 15 V. The UVLO 4 V devices maintain their output current within ±15% of the typical value over temperature and semiconductor process variation as well. As the gate driver output behaves as a current source, the output current remains well-regulated over the gate driver supply voltage range. The typical output current is dependent on the gate driver UVLO level as defined in "10. Ordering Guide" on page 48.
The driver output will operate as a current source until it runs out of voltage headroom. In other words, the MOSFETs which comprise the gate drive output transition from the saturated region into the linear operating region. Typical headroom knees for SPD± 7, 5, 3, and 1 are shown in Figure 12, "SPD+ Output Current vs. Output Voltage" and Figure 13, "SPD– Output Current vs. Output Voltage" below. Note that SPD± settings not shown do exhibit the same behavior. See "6.2.3. Gate Driver Characteristics" on page 24 for details.

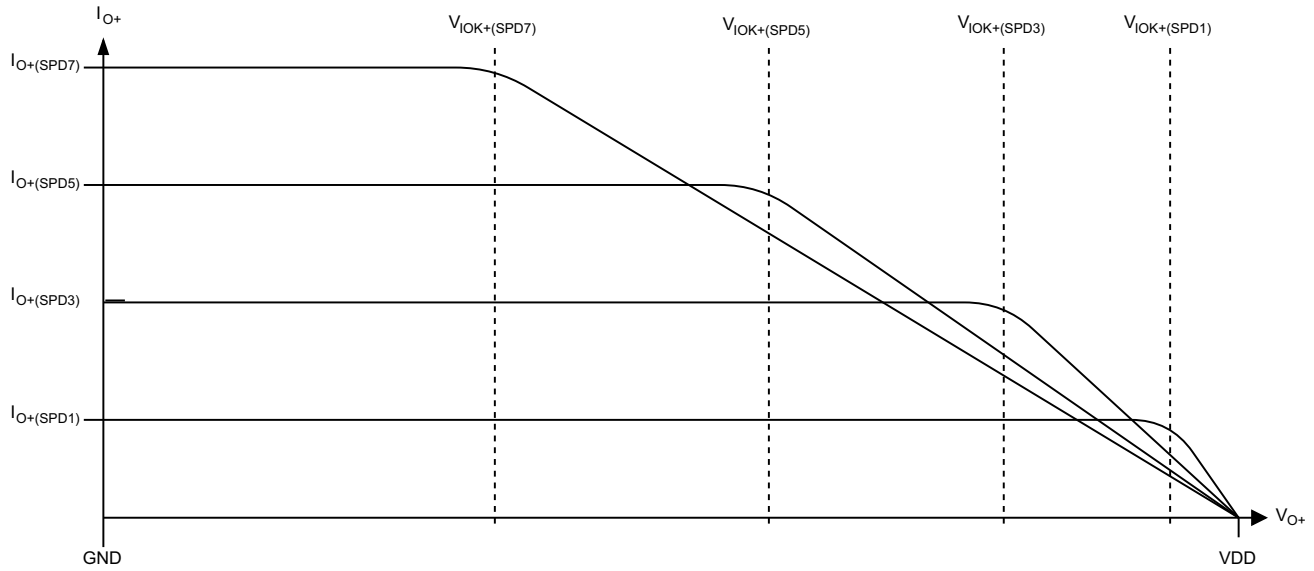


Figure 12. SPD+ Output Current vs. Output Voltage

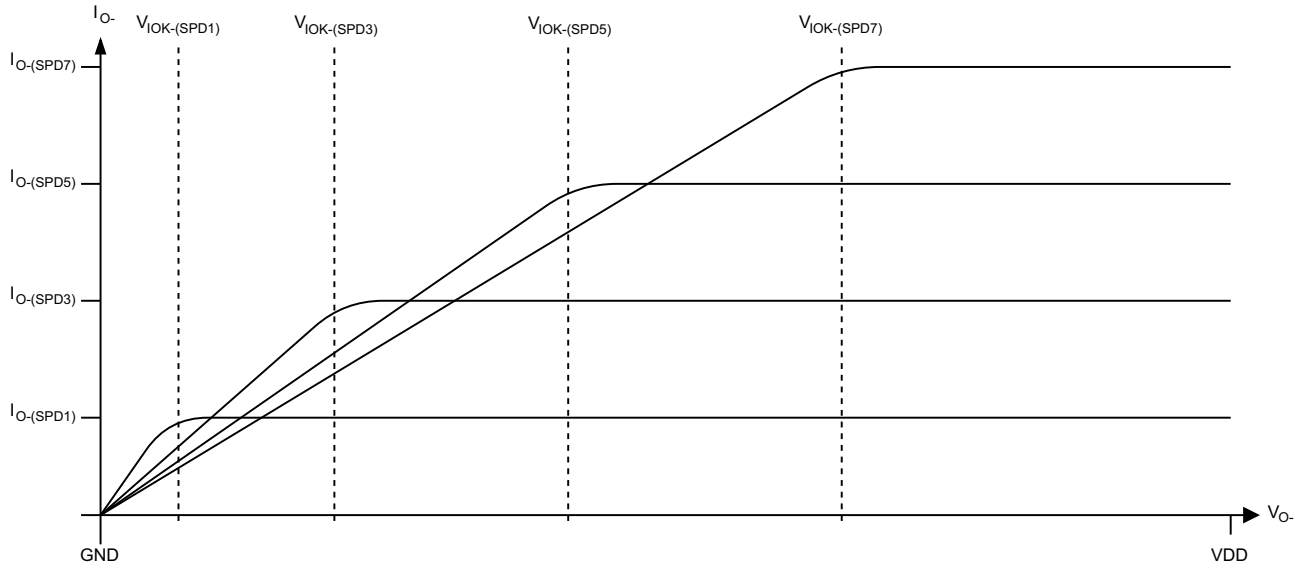


Figure 13. SPD– Output Current vs. Output Voltage

The device's output current levels are user selectable through the use of the SPD pins (SPD±, SPD+, and SPD–). The SPD+ pin controls the sourcing (turn-on) current, the SPD– pin controls the sinking (turn-off) current, and the SPD± pin controls both the sourcing and sinking currents simultaneously. There are eight selectable output current levels. For Si82C50x devices, the SPD± pin controls both sourcing and sinking current. For Si82C60x devices, the SPD+ pin only controls the sourcing current, and the sinking current is set to the maximum of SPD7–. For Si82C70x devices, the SPD– pin only controls the sinking current, and the sourcing current is set to the maximum of SPD7+.

For static control of the SPD± pin, use 1% resistors between the SPD pin and ground. See "5.1. Recommended Application Circuits" on page 15 and the SelVCD Resistor Settings in Table 5, "Logic Input Characteristics," on page 23 for more details. The SPD± pin operates by continuously sourcing $I_{SPD±}$ out of the pin and measuring the voltage at the pin. If dynamic speed control is utilized, the resistors can be removed and a voltage source can be placed on the SPD± pin. For any specific speed (SPD) setting, ensure that the voltage on the SPD± pin is within the minimum and maximum bounds for the associated SPD level. See the SelVCD Voltage Settings table in Table 5 for information on SPD voltage bounds. Note that the voltage source must be able to sink $I_{SPD±}$ from the SPD± pin. The sourcing and sinking current of VO± will change after Speed Update Delay (t_{SUD}). See Skyworks' AN1390: Methods for Dynamic Speed Control of the Si82Fx Performance Driver for more details on implementing dynamic speed control.

SelVCD eliminates the need for gate resistors and adds an integrated Miller clamp that operates through the gate driver output pin (VO–). The Miller clamp engages during the transition from V_{OH} to V_{OL}. When the output voltage, $V_{O–}$, falls below V_{MCT}, the output speed setting temporarily changes from the current speed setting to SPD7– to maximize the sinking current. An example of the Miller clamp engaging is shown in Figure 14, "Miller Clamp Engagement Behavior". Note that if the current speed setting is SPD7–, no change will occur. In the case of Si82C60x devices, the sinking output current is always set to SPD7–, so there will be no visible change.
The Miller clamp will stay engaged until the next V_{OL} to V_{OH} transition. If any voltage transients occur on VO– during the Off period, the Miller clamp will strongly clamp these to GND. For Si82C50x and Si82C70x devices, the user selected SPD– setting will be restored at the next V_{OH} to V_{OL} transition.

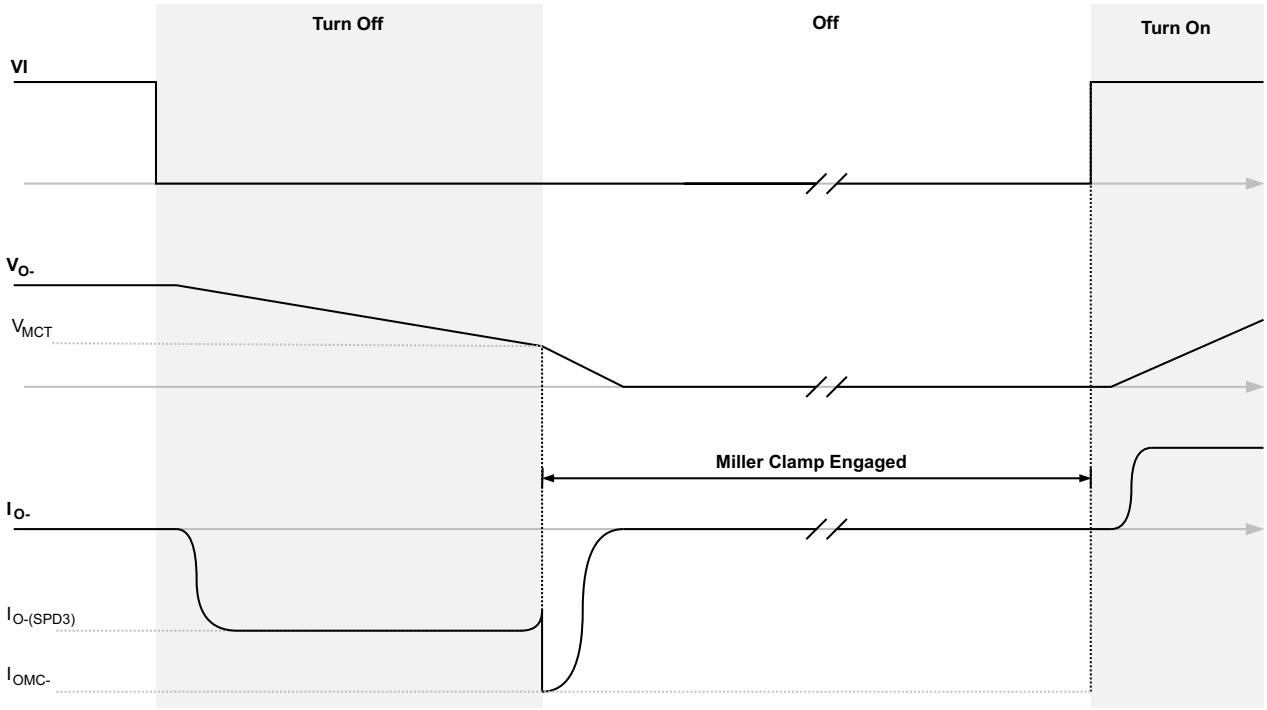


Figure 14. Miller Clamp Engagement Behavior

To achieve maximum Miller clamp performance, do not add any form of gate resistance between the gate driver output (VO–) and the power switch's gate or base. Use of gate resistors will cause a voltage drop across the resistor, which will slow down turn-on and turn-off transitions and reduce the effectiveness of the Miller clamp. In a traditional voltage-mode gate driver, external gate resistors dissipate a portion of the overall power required to charge and discharge the external power switch. As this power is dissipated internally in the Si82Cx, thermal protection will engage if power dissipation becomes excessive. See “4.6. Thermal Protection” on page 11 and “5.3. Power Dissipation Considerations” on page 19 for more details.

5. Application Information

The Si82Cx is designed to be both flexible and robust to meet a wide range of application requirements, safely survive overloads, and rapidly recover normal operation. To achieve these objectives, the appropriate Si82Cx device must be selected and its circuit carefully designed.

5.1. Recommended Application Circuits

Figure 15 illustrates a Si82Cx typical application circuit. The controller provides the Si82Cx input signal and can also provide disable functionality through pulling the SPD pin to VDDI.

The Si82Cx device's Selectable Variable Current Drive (SelVCD) feature eliminates the need for external high-power gate resistors at the gate driver's output. Resistor R26 is connected to the SPD pin and regulates the gate driver's output current strength, as detailed in “4.9. Selectable Variable Current Drive (SelVCD)” on page 12. Choose the R26 resistor value to meet the gate voltage rise-time/fall-time requirements based on the actual capacitive load of FET Q1.

In Figure 16. "Si82C60x Single Supply Configuration", the VO+ pin's output current is controlled by the SPD+ pin, while the VO– output current is fixed to SPD7. Conversely, in Figure 17. "Si82C70x Single Supply Configuration", the VO– pin's output current is controlled by the SPD– pin, and the VO+ output current is fixed to SPD7. For the pin with a fixed SPD7 setting, use a gate resistor attached to the output pin (VO+ or VO–) to control the current to the gate of FET Q1. Note that placing a gate resistor between VO– and the gate of FET Q1 will reduce the Miller clamp performance.

A high-voltage Y2-class capacitor (not shown in the diagrams) between the logic input reference (GNDI) and the gate driver reference (GND) is recommended if additional radiated emissions or electrostatic discharge (ESD) mitigation is desired. The typical value for the Y2 capacitor is between 47 pF and 100 pF. See Skyworks' “AN1131: Design Guide for Reducing Radiated and Conducted Emissions in Isolated Systems Using Skyworks’ Isolators” for additional techniques to mitigate radiated and conducted emissions. Note that the Si82Cx device provides excellent common-mode transient immunity (CMTI) without employing any additional components or techniques. However, if your application requires extremely high common-mode transient immunity (CMTI) performance, it is recommended to add a 10 nF capacitor between each of the logic input pins and the logic input ground (GNDI). This will help improve the CMTI performance.

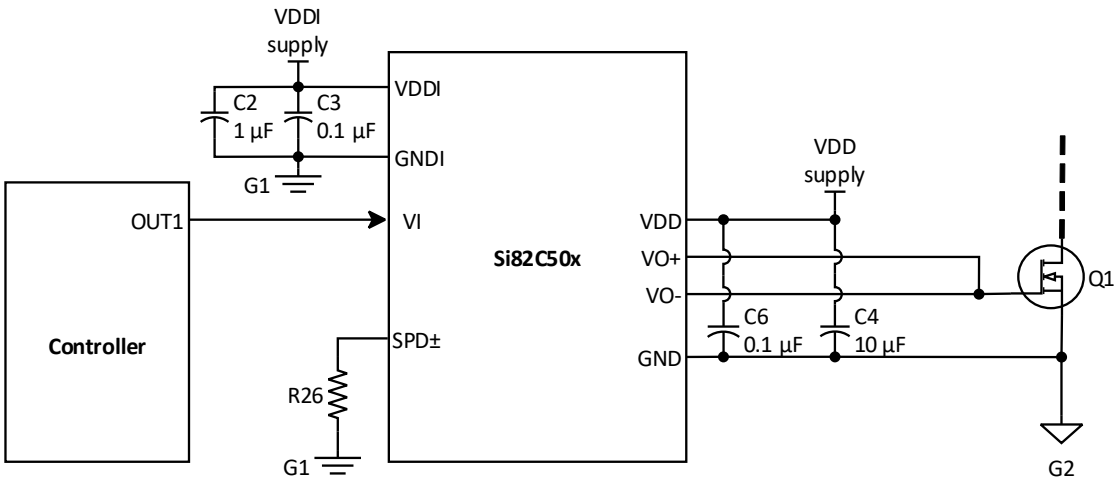


Figure 15. Si82C50x Single Supply Configuration

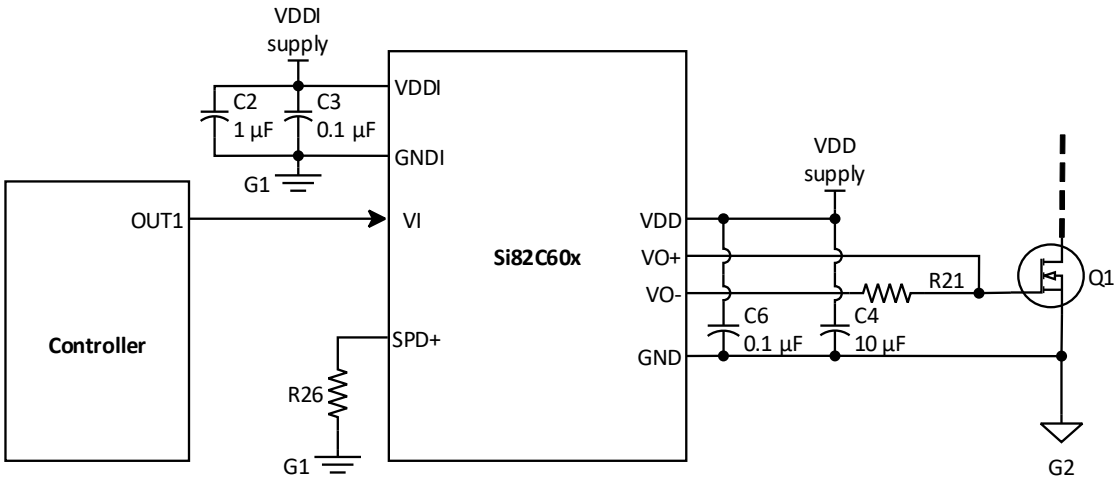


Figure 16. Si82C60x Single Supply Configuration

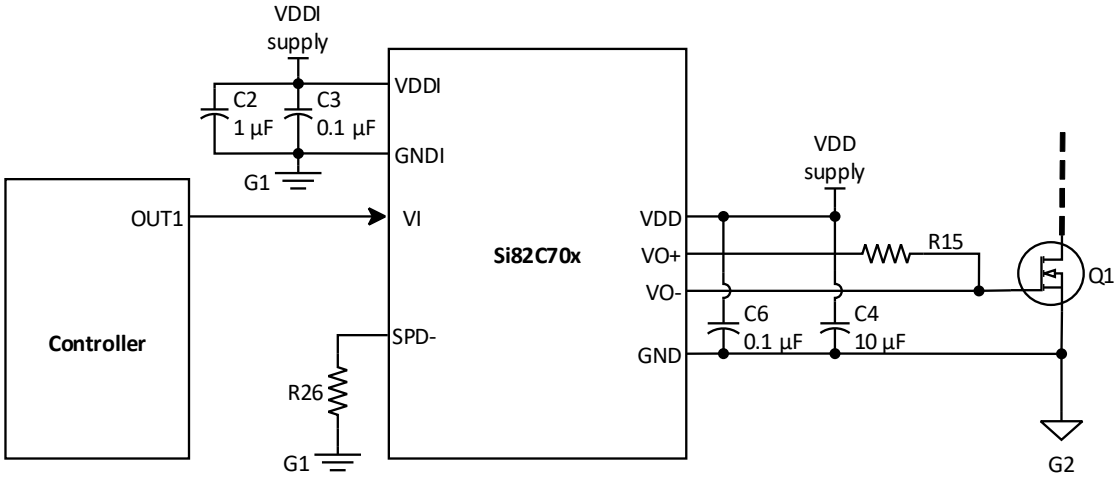


Figure 17. Si82C70x Single Supply Configuration

The diagram shown in Figure 18. "Si82Cx Bipolar Output Connection" is similar to the above circuit except that the drivers produce the bipolar V_{GS} output voltage. The bipolar V_{GS} output requires the system to provide positive and negative voltage sources. Note that the bootstrap circuit cannot be used to share the low-side voltage sources with the high-side gate driver for a bipolar V_{GS} output application. In this example, +15 V and –5 V sources are used. The voltage sources' reference G2 is electrically connected to FET Q1's source.

For the bipolar V_{GS} output application, the additional bypass capacitors form a capacitor divider in order to shorten the current flow loop. These capacitors should be placed close to the Si82Cx device's output power pins (VDD/GND). The ac component of the gate drive current flows from the VDDA net to the Si82Cx device's VDD pin, VO+ pin, Q1's gate, Q1's source, the midpoint of capacitors C16 and C17, and back to VDDA. Since the original bypass capacitors, C6 and C4, do not connect to reference G2 (which is connected to FET Q1's source), without capacitor C16, the return current needs to travel further to the system's +15 V source to complete the loop. This prolonged loop increases the chance of radiated emissions.

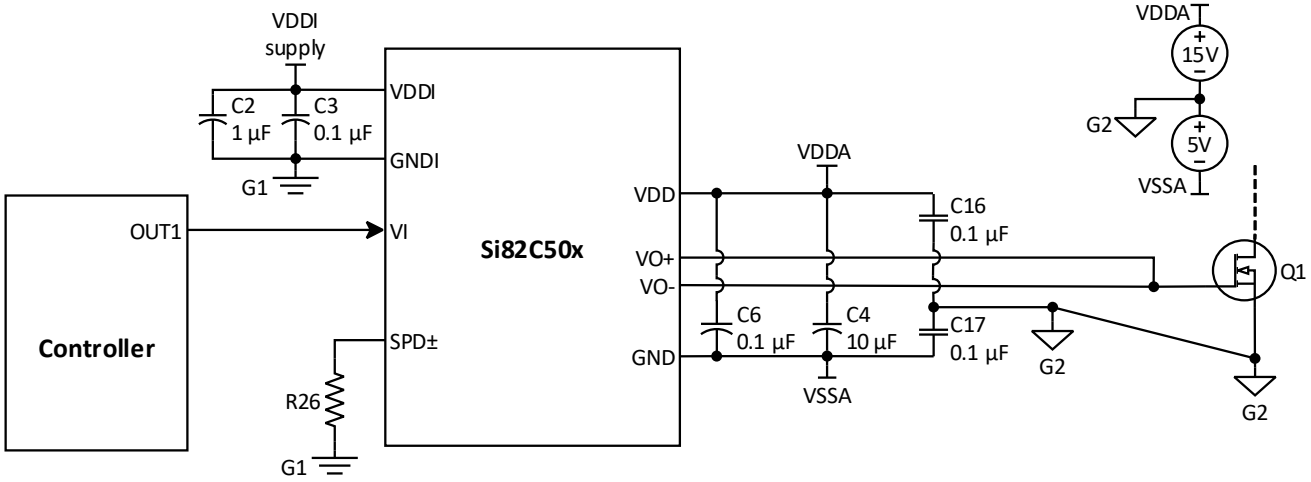


Figure 18. Si82Cx Bipolar Output Connection

5.2. Layout Considerations

The layout considerations are divided into general considerations for the entire device, the logic input side of the device, and the gate driver side. Refer to "5.1. Recommended Application Circuits" on page 15 for specific parts referenced.

5.2.1. General Considerations

- The bypass capacitors (usually 0.1 µF || 10 µF) should be placed close to the device's power supply pins and connected to the device with thick and short traces.
- The isolation barrier should have the required distance for the traces, power planes, ground planes, and copper areas on the device's logic input and gate drive sides.
- Safety isolation between two Si82Cx drivers is usually not required. If the system requires safety isolation between two drivers, the trace, power plane, ground plane, and the copper area between the two gate drivers should have the required distance. Even though safety isolation between two drivers is usually not required, to avoid arcing through the air, the traces operating at high voltage should have some distance (approximately 1 mm per 1 kV) from the low voltage signals.
- The Si82Cx device is often used in high-power systems with significant switching current and transient voltage. Attention should be paid to the proximity and orientation of the Si82Cx device and any high-current switching circuits. This should also apply to the traces and components surrounding the Si82Cx device to avoid unwanted noise coupling.

5.2.2. Logic Input Considerations

- Place resistor R26 close to the Si82Cx device's speed (SPD±) pin.
- If the application requires extremely high common-mode transient immunity (CMTI) performance, it is recommended to add a 10 nF capacitor between each of the logic input pins and the logic input ground (GNDI), including the no connect (NC) pins. This will help improve the CMTI performance.
- Using ≥6 mil trace width on all logic input pins is recommended. The interconnection between the controller and the Si82Cx device should be kept from any noisy signals in the system.

5.2.3. Gate Driver Considerations

- If the system is designed to provide a bipolar V_{GS} output, additional bypass capacitors (C16 and C17 in Figure 18, "Si82Cx Bipolar Output Connection," on page 17) are required to minimize the return path length of the gate drive signals.
- It is recommended to use ≥20 mil trace width for the VO± gate driver trace and its return path.
- For a unipolar V_{GS} output, the return path of the V_{GS} gate drive signal is from the power device's source/emitter to the Si82Cx device's gate driver ground pin (GND). Explicitly use ≥20 mil trace width for this return current path and route this trace close to the VO± gate driver trace to reduce the loop area of the whole V_{GS} gate drive signal. Moreover, it is a good practice to set the copper keep-out region along the return path trace so the system ground copper will not flood over this return trace.
- For a bipolar V_{GS} output, the return path of the V_{GS} gate drive signal is from the power device's source/emitter to the midpoint of capacitors C16 and C17. Therefore, these capacitors must be placed close to the Si82Cx device to minimize this current loop. Explicitly use ≥20 mil trace width for the return current path and route this return trace close to the VO± gate driver trace to reduce the loop area of the whole V_{GS} gate drive signal. Moreover, it is a good practice to set the copper keep-out region along the return path trace so the system ground copper will not flood over this return trace.

- For a multiple-layer PCB design, ground and power planes are recommended to create a power supply current path with the least inductance. If there is no dedicated power or ground plane on the gate driver side, use ≥20 mil trace width for the power supply connections.
- If the design utilizes a Y2 capacitor between the logic input and the gate driver, the Y2 capacitors across the isolation barrier should be placed as close as possible to the sides of the Si82Cx device without pins.

5.3. Power Dissipation Considerations

The device's average power dissipation is often required in order to estimate the silicon junction temperature and can be estimated using the equation provided in "AN1339: Driver Power Dissipation Considerations". To solve the equation, the intended supply voltages, the load characteristics, the gate resistor values, and the switching frequency need to be collected. Skyworks provides a Microsoft Excel® based calculator as part of AN1339 to easily estimate the device's power dissipation and its silicon junction temperature.

6. Specifications

6.1. Absolute Maximum Ratings

Table 3. Absolute Maximum Ratings[1]

Parameter	Symbol	Condition	Min	Max	Unit
Storage temperature	T_{STG}		–65	150	°C
Operating temperature	T_A		–40	125	°C
Junction temperature	T_J		—	150	°C
Logic input supply voltage	VDDI		–0.30	24.0	V
Gate driver supply voltage	VDD		–0.30	36.0	V
Input signal voltage	VI, SPD±, SPD+, SPD–		–0.30	VDDI + 0.30	V
	VI, SPD±, SPD+, SPD–	Transient for 100 ns[2]	–5.00	VDDI + 0.30	V
Output signal voltage	VO+, VO–		–0.30	VDD + V_{SCC}	V
		Transient for 200 ns[2]	–2.00	VDD + V_{SCC}	V
Lead solder temperature		Duration = 10 s	—	260	°C
ESD per AEC-Q100					
Human body model	HBM		–4	4	kV
Charged device model	CDM		–2	2	kV

1. Permanent device damage may occur if the absolute maximum ratings are exceeded. Functional operation should be restricted to the conditions specified in the operational sections of this data sheet. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.
2. This parameter is not subject to production test. It is guaranteed by characterization.

ESD Handling: Industry-standard ESD handling precautions must be adhered to at all times to avoid damage to this device.

6.2. Electrical Characteristics

The following tables provide electrical parametric data for this device.

6.2.1. Power Supply Characteristics

Table 4. Power Supply Characteristics

Operating range for the following specifications: VDDI = 3.0–20 V; VDD = 5.0–30 V; T_A = –40 to +125 °C; F_{IN} ≤ 1 MHz.

Typical specifications: VDDI = 5 V; VDD = 6 V for 4 V UVLO devices, 10 V for 8 V UVLO devices, 15 V for 12 V UVLO devices, 18 V for 15 V UVLO devices; T_A = 25 °C unless otherwise noted.

Parameter	Symbol	Test Condition	Min	Typ	Max	Unit
Supply Voltage						
Logic input supply	VDDI		3.00	—	20.0	V
Gate driver supply	VDD		5.00	—	30.0	V
Supply Current						
Logic Input Supply						
Quiescent current	$IDDI_Q$	VI = logic low and/or SPD±, SPD+, SPD– = logic high	—	1.15	1.70	mA
Active current	IDDI	VI = 1 MHz; 50% duty cycle	—	1.57	2.13	mA
Gate Driver Supply						
4 V Undervoltage Lockout (Si82CxxxGx) Devices						
Quiescent current	IDD_Q	VI = logic low and/or SPD±, SPD+, SPD– = logic high	—	2.93	4.02	mA
Active current	IDD	VO+/VO– = 1 MHz; 50% duty cycle; no load; Speed 7	—	5.99	13.2	mA
8 V Undervoltage Lockout (Si82CxxxBx) Devices						
Quiescent current	IDD_Q	VI = logic low and/or SPD±, SPD+, SPD– = logic high	—	2.95	4.02	mA
Active current	IDD	VO+/VO– = 1 MHz; 50% duty cycle; no load; Speed 7	—	7.14	13.2	mA
12 V Undervoltage Lockout (Si82CxxxCx) Devices						
Quiescent current	IDD_Q	VI = logic low and/or SPD±, SPD+, SPD– = logic high	—	3.00	4.02	mA
Active current	IDD	VO+/VO– = 1 MHz; 50% duty cycle; no load; Speed 7	—	8.51	13.2	mA
15 V Undervoltage Lockout (Si82CxxxEx) Devices						
Quiescent current	IDD_Q	VI = logic low and/or SPD±, SPD+, SPD– = logic high	—	3.06	4.02	mA
Active current	IDD	VO+/VO– = 1 MHz; 50% duty cycle; no load; Speed 7	—	9.33	13.2	mA

Table 4. Power Supply Characteristics (Continued)

Operating range for the following specifications: VDDI = 3.0–20 V; VDD = 5.0–30 V; T_A = –40 to +125 °C; F_{IN} ≤ 1 MHz.

Typical specifications: VDDI = 5 V; VDD = 6 V for 4 V UVLO devices, 10 V for 8 V UVLO devices, 15 V for 12 V UVLO devices, 18 V for 15 V UVLO devices; T_A = 25 °C unless otherwise noted.

Parameter	Symbol	Test Condition	Min	Typ	Max	Unit
Undervoltage Lockout						
Logic Input Supply						
Positive-going threshold	$VDDI_{UV+}$	VDDI rising	2.74	2.88	2.99	V
Negative-going threshold	$VDDI_{UV–}$	VDDI falling	2.67	2.79	2.91	V
VDDI undervoltage hysteresis	$VDDI_{HYS}$		—	90.0	—	mV
Gate Driver Supply						
4 V Undervoltage Lockout (Si82CxxxGx) Devices						
Positive-going threshold	VDD_{UV+}	VDD rising	4.09	4.30	4.54	V
Negative-going threshold	$VDD_{UV–}$	VDD falling	3.89	4.10	4.33	V
Threshold hysteresis	VDD_{HYS}		—	200	—	mV
8 V Undervoltage Lockout (Si82CxxxBx) Devices						
Positive-going threshold	VDD_{UV+}	VDD rising	7.58	8.07	8.55	V
Negative-going threshold	$VDD_{UV–}$	VDD falling	7.14	7.57	8.05	V
Threshold hysteresis	VDD_{HYS}		—	500	—	mV
12 V Undervoltage Lockout (Si82CxxxCx) Devices						
Positive-going threshold	VDD_{UV+}	VDD rising	11.21	11.90	12.61	V
Negative-going threshold	$VDD_{UV–}$	VDD falling	10.29	10.90	11.52	V
Threshold hysteresis	VDD_{HYS}		—	1.00	—	V
15 V Undervoltage Lockout (Si82CxxxEx) Devices						
Positive-going threshold	VDD_{UV+}	VDD rising	14.19	15.15	16.13	V
Negative-going threshold	$VDD_{UV–}$	VDD falling	13.81	14.70	15.66	V
Threshold hysteresis	VDD_{HYS}		—	450	—	mV

6.2.2. Logic Input Characteristics

Table 5. Logic Input Characteristics

Operating range for the following specifications: VDDI = 3.0–20 V; VDD = 5.0–30 V; T_A = –40 to +125 °C; F_{IN} ≤ 1 MHz.

Typical specifications: VDDI = 5 V; VDD = 6 V for 4 V UVLO devices, 10 V for 8 V UVLO devices, 15 V for 12 V UVLO devices, 18 V for 15 V UVLO devices; T_A = 25 °C unless otherwise noted.

Parameter	Symbol	Test Condition	Min	Typ	Max	Unit
Input Threshold						
High input	V_{IH}	VI rising	VDDI x 0.85	—	—	V
Low input	V_{IL}	VI falling	—	—	VDDI x 0.22	V
Hysteresis	V_{HYS}	VI	VDDI x 0.06	VDDI x 0.15	—	V
Input pull-down resistance	R_I	VI	152	200	279	kΩ
Input leakage current	$\lvert I_{LKG} \rvert$	VI	—	—	131	µA
SelVCD Resistor Settings[1]						
Speed 0	$R_{SPD0\pm}$, R_{SPD0+}, R_{SPD0-}	SPD±, SPD+, SPD–	—	0.00	—	kΩ
Speed 1	$R_{SPD1\pm}$, R_{SPD1+}, R_{SPD1-}	SPD±, SPD+, SPD–	—	2.67	—	kΩ
Speed 2	$R_{SPD2\pm}$, R_{SPD2+}, R_{SPD2-}	SPD±, SPD+, SPD–	—	4.12	—	kΩ
Speed 3	$R_{SPD3\pm}$, R_{SPD3+}, R_{SPD3-}	SPD±, SPD+, SPD–	—	5.62	—	kΩ
Speed 4	$R_{SPD4\pm}$, R_{SPD4+}, R_{SPD4-}	SPD±, SPD+, SPD–	—	7.32	—	kΩ
Speed 5	$R_{SPD5\pm}$, R_{SPD5+}, R_{SPD5-}	SPD±, SPD+, SPD–	—	9.53	—	kΩ
Speed 6	$R_{SPD6\pm}$, R_{SPD6+}, R_{SPD6-}	SPD±, SPD+, SPD–	—	12.4	—	kΩ
Speed 7	$R_{SPD7\pm}$, R_{SPD7+}, R_{SPD7-}	SPD±, SPD+, SPD–	—	15.8	—	kΩ
SelVCD Voltage Settings						
Speed 0	$V_{SPD0\pm}$, V_{SPD0+}, V_{SPD0-}	SPD±, SPD+, SPD–	0.00	—	85.0	mV
Speed 1	$V_{SPD1\pm}$, V_{SPD1+}, V_{SPD1-}	SPD±, SPD+, SPD–	127	—	145	mV
Speed 2	$V_{SPD2\pm}$, V_{SPD2+}, V_{SPD2-}	SPD±, SPD+, SPD–	197	—	224	mV
Speed 3	$V_{SPD3\pm}$, V_{SPD3+}, V_{SPD3-}	SPD±, SPD+, SPD–	268	—	306	mV
Speed 4	$V_{SPD4\pm}$, V_{SPD4+}, V_{SPD4-}	SPD±, SPD+, SPD–	350	—	398	mV
Speed 5	$V_{SPD5\pm}$, V_{SPD5+}, V_{SPD5-}	SPD±, SPD+, SPD–	455	—	518	mV
Speed 6	$V_{SPD6\pm}$, V_{SPD6+}, V_{SPD6-}	SPD±, SPD+, SPD–	593	—	674	mV
Speed 7	$V_{SPD7\pm}$, V_{SPD7+}, V_{SPD7-}	SPD±, SPD+, SPD–	755	—	858	mV
SelVCD resistor current	$I_{SPD\pm}$, I_{SPD+}, I_{SPD-}	SPD±, SPD+, SPD–	49.3	51.0	52.7	µA

1. Specified with E96 1% accuracy resistors. See "4.9. Selectable Variable Current Drive (SelVCD)" on page 12 for more information.

6.2.3. Gate Driver Characteristics

Table 6. Gate Driver Characteristics

Operating range for the following specifications: VDDI = 3.0–20 V; VDD = 5.0–30 V; T_A = –40 to +125 °C; $F_{IN} \leq 1$ MHz.

Typical specifications: VDDI = 5 V; VDD = 6 V for 4 V UVLO devices, 10 V for 8 V UVLO devices, 15 V for 12 V UVLO devices, 18 V for 15 V UVLO devices; T_A = 25 °C unless otherwise noted.

Parameter	Symbol	Test Condition	Min	Typ	Max	Unit
Output Voltage						
Logic high (sourcing)	V_{OH}	I_O = –20 mA	VDD x 0.98	—	—	V
Logic low (sinking)	V_{OL}	I_O = 20 mA	—	—	0.10	V
Output Resistance						
Logic high (sourcing)	R_{ON+}	15 V UVLO, SPD 7	—	1.00	—	Ω
Logic low (sinking)	$R_{ON–}$		—	0.70	—	Ω
Output Current						
4 V Undervoltage Lockout (Si82CxxxGx) Devices						
Logic high (sourcing)	I_{O+}	Speed 7, VDD = 6 V, VO = 1.5 V	1.27	1.50	1.73	A
Logic low (sinking)	$I_{O–}$	Speed 7, VDD = 6 V, VO = 4.5 V	1.27	1.50	1.73	A
8 V Undervoltage Lockout (Si82CxxxBx) Devices						
Logic high (sourcing)	I_{O+}	Speed 7, VDD = 10 V, VO = 3 V	2.25	2.50	2.75	A
Logic low (sinking)	$I_{O–}$	Speed 7, VDD = 10 V, VO = 7 V	2.25	2.50	2.75	A
12 V Undervoltage Lockout (Si82CxxxCx) Devices						
Logic high (sourcing)	I_{O+}	Speed 7, VDD = 15 V, VO = 5 V	3.15	3.50	3.85	A
Logic low (sinking)	$I_{O–}$	Speed 7, VDD = 15 V, VO = 10 V	3.15	3.50	3.85	A
15 V Undervoltage Lockout (Si82CxxxEx) Devices						
Logic high (sourcing)	I_{O+}	Speed 7, VDD = 18 V, VO = 6 V	3.60	4.00	4.40	A
Logic low (sinking)	$I_{O–}$	Speed 7, VDD = 18 V, VO = 12 V	3.60	4.00	4.40	A
Output Current Ratio						
Logic High (Sourcing)						
Speed 0	$\Delta_{IO+(0:7)}$	$I_{O(SPD0)} \div I_{O(SPD7)}$	5.08	8.75	12.6	%
Speed 1	$\Delta_{IO+(1:7)}$	$I_{O(SPD1)} \div I_{O(SPD7)}$	8.93	12.5	16.9	%
Speed 2	$\Delta_{IO+(2:7)}$	$I_{O(SPD2)} \div I_{O(SPD7)}$	14.1	17.5	23.3	%
Speed 3	$\Delta_{IO+(3:7)}$	$I_{O(SPD3)} \div I_{O(SPD7)}$	20.1	25.0	31.7	%
Speed 4	$\Delta_{IO+(4:7)}$	$I_{O(SPD4)} \div I_{O(SPD7)}$	30.9	35.0	42.8	%
Speed 5	$\Delta_{IO+(5:7)}$	$I_{O(SPD5)} \div I_{O(SPD7)}$	44.6	50.0	58.6	%
Speed 6	$\Delta_{IO+(6:7)}$	$I_{O(SPD6)} \div I_{O(SPD7)}$	62.9	70.0	79.2	%
Speed 7	$\Delta_{IO+(7:7)}$	$I_{O(SPD7)} \div I_{O(SPD7)}$	100	100	100	%

Table 6. Gate Driver Characteristics (Continued)

Operating range for the following specifications: VDDI = 3.0–20 V; VDD = 5.0–30 V; T_A = –40 to +125 °C; $F_{IN} \leq 1$ MHz.

Typical specifications: VDDI = 5 V; VDD = 6 V for 4 V UVLO devices, 10 V for 8 V UVLO devices, 15 V for 12 V UVLO devices, 18 V for 15 V UVLO devices; T_A = 25 °C unless otherwise noted.

Parameter	Symbol	Test Condition	Min	Typ	Max	Unit
Logic Low (Sinking)						
Speed 0	$\Delta_{IO-(0:7)}$	$I_{O(SPD0)} \div I_{O(SPD7)}$	5.67	8.75	14.5	%
Speed 1	$\Delta_{IO-(1:7)}$	$I_{O(SPD1)} \div I_{O(SPD7)}$	9.89	12.5	18.4	%
Speed 2	$\Delta_{IO-(2:7)}$	$I_{O(SPD2)} \div I_{O(SPD7)}$	15.6	17.5	24.4	%
Speed 3	$\Delta_{IO-(3:7)}$	$I_{O(SPD3)} \div I_{O(SPD7)}$	22.9	25.0	32.4	%
Speed 4	$\Delta_{IO-(4:7)}$	$I_{O(SPD4)} \div I_{O(SPD7)}$	33.0	35.0	45.6	%
Speed 5	$\Delta_{IO-(5:7)}$	$I_{O(SPD5)} \div I_{O(SPD7)}$	45.7	50.0	61.0	%
Speed 6	$\Delta_{IO-(6:7)}$	$I_{O(SPD6)} \div I_{O(SPD7)}$	65.9	70.0	81.5	%
Speed 7	$\Delta_{IO-(7:7)}$	$I_{O(SPD7)} \div I_{O(SPD7)}$	100	100	100	%
Output Current Knee						
4 V Undervoltage Lockout (Si82CxxxGx) Devices						
Logic High (Sourcing)						
Speed 1	$V_{IOK+(SPD1)}$	VDD = 6 V	—	4.05	—	V
Speed 3	$V_{IOK+(SPD3)}$		—	3.90	—	V
Speed 5	$V_{IOK+(SPD5)}$		—	3.60	—	V
Speed 7	$V_{IOK+(SPD7)}$		—	3.10	—	V
Logic Low (Sinking)[1]						
Speed 1	$V_{IOK-(SPD1)}$	VDD = 6 V	—	V_{MCT}	—	V
Speed 3	$V_{IOK-(SPD3)}$		—	V_{MCT}	—	V
Speed 5	$V_{IOK-(SPD5)}$		—	V_{MCT}	—	V
Speed 7	$V_{IOK-(SPD7)}$		—	V_{MCT}	—	V
8 V Undervoltage Lockout (Si82CxxxBx) Devices						
Logic High (Sourcing)						
Speed 1	$V_{IOK+(SPD1)}$	VDD = 10 V	—	6.75	—	V
Speed 3	$V_{IOK+(SPD3)}$		—	6.45	—	V
Speed 5	$V_{IOK+(SPD5)}$		—	6.10	—	V
Speed 7	$V_{IOK+(SPD7)}$		—	5.45	—	V
Logic Low (Sinking)[1]						
Speed 1	$V_{IOK-(SPD1)}$	VDD = 10 V	—	V_{MCT}	—	V
Speed 3	$V_{IOK-(SPD3)}$		—	V_{MCT}	—	V
Speed 5	$V_{IOK-(SPD5)}$		—	V_{MCT}	—	V
Speed 7	$V_{IOK-(SPD7)}$		—	3.40	—	V

Table 6. Gate Driver Characteristics (Continued)

Operating range for the following specifications: VDDI = 3.0–20 V; VDD = 5.0–30 V; T_A = –40 to +125 °C; $F_{IN} \leq 1$ MHz.

Typical specifications: VDDI = 5 V; VDD = 6 V for 4 V UVLO devices, 10 V for 8 V UVLO devices, 15 V for 12 V UVLO devices, 18 V for 15 V UVLO devices; T_A = 25 °C unless otherwise noted.

Parameter	Symbol	Test Condition	Min	Typ	Max	Unit
12 V Undervoltage Lockout (Si82CxxxCx) Devices						
Logic High (Sourcing)						
Speed 1	$V_{IOK+(SPD1)}$	VDD = 15 V	—	9.90	—	V
Speed 3	$V_{IOK+(SPD3)}$		—	9.65	—	V
Speed 5	$V_{IOK+(SPD5)}$		—	9.20	—	V
Speed 7	$V_{IOK+(SPD7)}$		—	8.40	—	V
Logic Low (Sinking)						
Speed 1	$V_{IOK-(SPD1)}$	VDD = 15 V	—	2.50	—	V
Speed 3	$V_{IOK-(SPD3)}$		—	2.95	—	V
Speed 5	$V_{IOK-(SPD5)}$		—	3.65	—	V
Speed 7	$V_{IOK-(SPD7)}$		—	4.60	—	V
15 V Undervoltage Lockout (Si82CxxxEx) Devices						
Logic High (Sourcing)						
Speed 1	$V_{IOK+(SPD1)}$	VDD = 18 V	—	11.75	—	V
Speed 3	$V_{IOK+(SPD3)}$		—	11.45	—	V
Speed 5	$V_{IOK+(SPD5)}$		—	10.95	—	V
Speed 7	$V_{IOK+(SPD7)}$		—	10.15	—	V
Logic Low (Sinking)						
Speed 1	$V_{IOK-(SPD1)}$	VDD = 18 V	—	2.95	—	V
Speed 3	$V_{IOK-(SPD3)}$		—	3.55	—	V
Speed 5	$V_{IOK-(SPD5)}$		—	4.30	—	V
Speed 7	$V_{IOK-(SPD7)}$		—	5.35	—	V

Table 6. Gate Driver Characteristics (Continued)

Operating range for the following specifications: VDDI = 3.0–20 V; VDD = 5.0–30 V; T_A = –40 to +125 °C; $F_{IN} \leq 1$ MHz.

Typical specifications: VDDI = 5 V; VDD = 6 V for 4 V UVLO devices, 10 V for 8 V UVLO devices, 15 V for 12 V UVLO devices, 18 V for 15 V UVLO devices; T_A = 25 °C unless otherwise noted.

Parameter	Symbol	Test Condition	Min	Typ	Max	Unit
Miller Clamp						
Threshold voltage	V_{MCT}		1.75	2.00	2.35	V
Output Current						
4 V undervoltage lockout (Si82CxxxGx) devices	I_{OMC}	VDD = 6 V, VO = V_{MCT}	—	1.50	—	A
		VDD = 6 V, VO = 4.5 V	—	1.50	—	A
8 V undervoltage lockout (Si82CxxxBx) devices		VDD = 10 V, VO = V_{MCT}	—	1.80	—	A
		VDD = 10 V, VO = 7 V	—	2.50	—	A
12 V undervoltage lockout (Si82CxxxCx) devices		VDD = 15 V, VO = V_{MCT}	—	1.90	—	A
		VDD = 15 V, VO = 10 V	—	3.50	—	A
15 V undervoltage lockout (Si82CxxxEx) devices		VDD = 18 V, VO = V_{MCT}	—	2.10	—	A
		VDD = 18 V, VO = 12 V	—	4.00	—	A
Output resistance	R_{ONMC}		—	0.70	—	Ω
Short Circuit Clamp						
Clamping voltage	V_{SCC}	VO – VDD or GND – VO, I_O = 70 mA	—	70.0	—	mV
		VO – VDD or GND – VO, I_O = 500 mA, t_{SCC} = 10 µs	—	530	—	mV
Thermal Shutdown						
Trigger temperature	T_{SD+}	T_J rising	—	163	—	°C
Release temperature	$T_{SD–}$	T_J falling	—	131	—	°C
Shutdown clamp output voltage	V_{SDC}	VDD = High-Z, I_O = 50 mA	—	1.55	2.00	V

1. A typical value referencing the Miller Clamp Threshold Voltage (V_{MCT}) indicates that the current does not fall below 85% of the stated output current before the Miller clamp engages.

6.2.4. Timing Characteristics

Table 7. Timing Characteristics

Operating range for the following specifications: VDDI = 3.0–20 V; VDD = 5.0–30 V; T_A = –40 to +125 °C; $F_{IN} \leq 1$ MHz.

Typical specifications: VDDI = 5 V; VDD = 6 V for 4 V UVLO devices, 10 V for 8 V UVLO devices, 15 V for 12 V UVLO devices, 18 V for 15 V UVLO devices; T_A = 25 °C unless otherwise noted.

Parameter	Symbol	Test Condition	Min	Typ	Max	Unit
Minimum Pulse Width						
Si82CxxAx devices	PW_{MIN}	No load	—	10.0	—	ns
Si82CxxBx devices			—	30.0	—	ns
Si82CxxEx devices			—	90.0	—	ns
Propagation Delay						
Positive-Going Control Input Delay[1]						
0 ns deglitch (Si82CxxAx) devices	t_{PLH}	VI rising; no load	22.0	30.0	43.4	ns
30 ns deglitch (Si82CxxBx) devices			46.8	56.0	72.6	ns
90 ns deglitch (Si82CxxEx) devices			110	127	144	ns
Negative-Going Control Input Delay[1]						
0 ns deglitch (Si82CxxAx) devices	t_{PHL}	VI falling; no load	22.0	30.0	43.4	ns
30 ns deglitch (Si82CxxBx) devices			46.8	56.0	72.6	ns
90 ns deglitch (Si82CxxEx) devices			110	127	144	ns
Enable input delay[2]	t_{EID}	SPD±, SPD+, SPD– falling, no load	—	20.0	—	µs
Disable input delay[2]	t_{DID}	SPD±, SPD+, SPD– rising, no load	—	20.0	—	µs
Speed update delay[3]	t_{SUD}	SPD±, SPD+, SPD–	—	65.0	—	µs
Pulse width distortion	PWD	$\lvert t_{PLH} - t_{PHL} \rvert$	—	5.00	10.0	ns

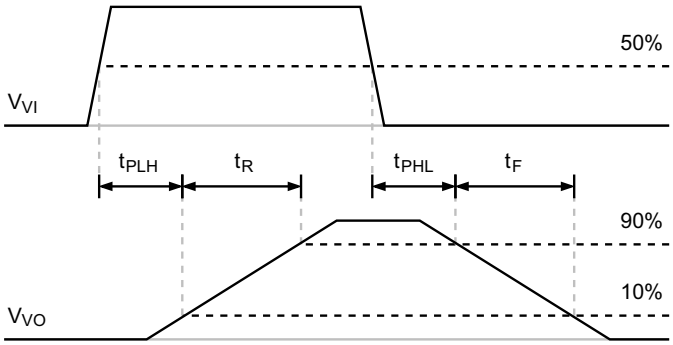
Table 7. Timing Characteristics (Continued)

Operating range for the following specifications: VDDI = 3.0–20 V; VDD = 5.0–30 V; T_A = –40 to +125 °C; $F_{IN} \leq 1$ MHz.

Typical specifications: VDDI = 5 V; VDD = 6 V for 4 V UVLO devices, 10 V for 8 V UVLO devices, 15 V for 12 V UVLO devices, 18 V for 15 V UVLO devices; T_A = 25 °C unless otherwise noted.

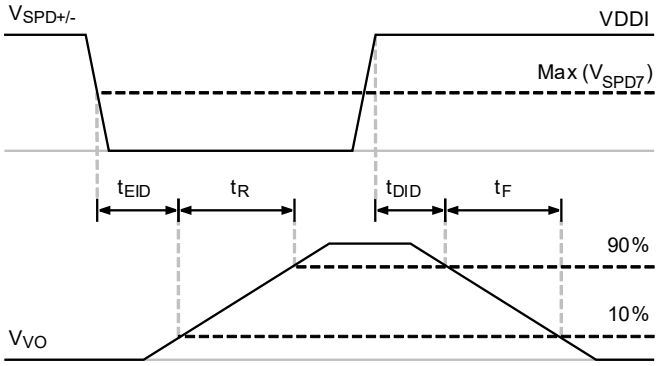
Parameter	Symbol	Test Condition	Min	Typ	Max	Unit
Propagation Delay Skew						
Part-to-Part[4]						
0 ns deglitch (Si82CxxAx) devices	$t_{PSK(PP)}$	MAX{ $\lvert t_{PLHx}-t_{PLHy} \rvert$, $\lvert t_{PHLx}-t_{PHLy} \rvert$ }	—	—	5.00	ns
30 ns deglitch (Si82CxxBx) devices			—	—	8.00	ns
90 ns deglitch (Si82CxxEx) devices			—	—	20.0	ns
Output Rise Time[1]						
4 V UVLO (Si82CxxxGx) devices	t_R	Speed 7, VDD = 6 V, C_L = 2.2 nF	—	16.0	—	ns
8 V UVLO (Si82CxxxBx) devices		Speed 7, VDD = 10 V, C_L = 2.2 nF	—	16.0	—	ns
12 V UVLO (Si82CxxxCx) devices		Speed 7, VDD= 15 V, C_L = 2.2 nF	—	17.0	—	ns
15 V UVLO (Si82CxxxEx) devices		Speed 7, VDD= 18 V, C_L = 2.2 nF	—	17.0	—	ns
Output Fall Time[1]						
4 V UVLO (Si82CxxxGx) devices	t_F	Speed 7, VDD = 6 V, C_L = 2.2 nF	—	22.0	—	ns
8 V UVLO (Si82CxxxBx) devices		Speed 7, VDD = 10 V, C_L = 2.2 nF	—	19.0	—	ns
12 V UVLO (Si82CxxxCx) devices		Speed 7, VDD = 15 V, C_L = 2.2 nF	—	18.0	—	ns
15 V UVLO (Si82CxxxEx) devices		Speed 7, VDD = 18 V, C_L = 2.2 nF	—	20.0	—	ns
Startup time[5]	t_{ST}		—	75.0	—	µs
VDDI logic input power cycle time[5]	t_{PCL}		—	40.0	—	µs
VDDI logic input shutdown time[5]	t_{SDL}		—	300	—	ns
VDD gate driver power cycle time[5]	t_{PCG}		—	75.0	—	µs
VDD gate driver shutdown time[5]	t_{SDG}		—	330	—	ns
Common-mode transient immunity	CMTI		200	—	—	kV/µs

1. See Figure 19, “Control Input Timing Measurements,” on page 30 for details.
2. See Figure 20, “Enable or Disable Input Timing Measurements,” on page 30 for details.
3. t_{SUD} is measured from the edge of a square wave applied to the input (SPD±, SPD+ or SPD–) to next change in output (VO+/VO–) voltage slope. See Figure 21, “Speed Update Delay Timing Measurement,” on page 30 for details.
4. $t_{PSK(PP)}$ is the largest absolute value difference in propagation delays measured between different units operating at the same supply voltages, load, and ambient temperature.
5. Startup, power cycle, and shutdown timing are detailed in “4.2. Power Sequence and Timing Behavior” on page 9.



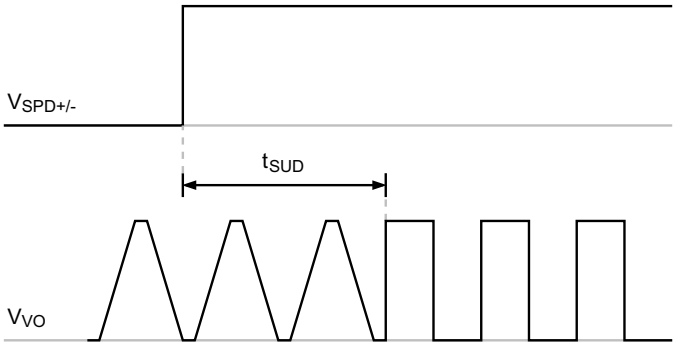
VO = VO+ and VO- tied together
$V_{SPD} \leq V_{SPD7}$

Figure 19. Control Input Timing Measurements



VO = VO+ and VO- tied together
VI = Logic High

Figure 20. Enable or Disable Input Timing Measurements



VI = Square wave
VO = VO+ and VO- tied together
$V_{SPD} \leq V_{SPD7}$

Figure 21. Speed Update Delay Timing Measurement

6.3. Typical Performance Characteristics

The typical performance characteristics depicted in the figures below are for information purposes only. Refer to the data tables in "6.2. Electrical Characteristics" on page 21 for actual specification limits.

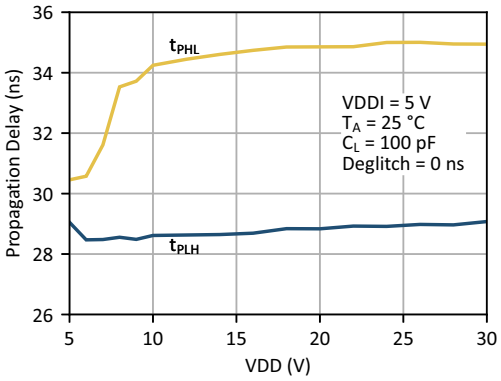


Figure 22. Propagation Delay vs. Gate Driver Supply Voltage

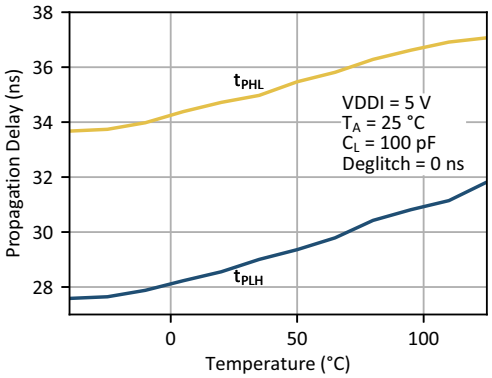


Figure 23. Propagation Delay vs. Ambient Temperature

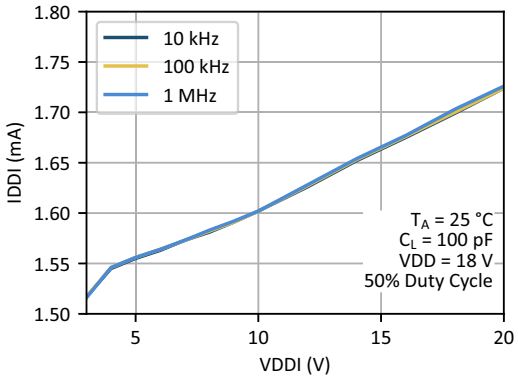


Figure 24. Logic Input Active Supply Current vs. Logic Input Supply Voltage

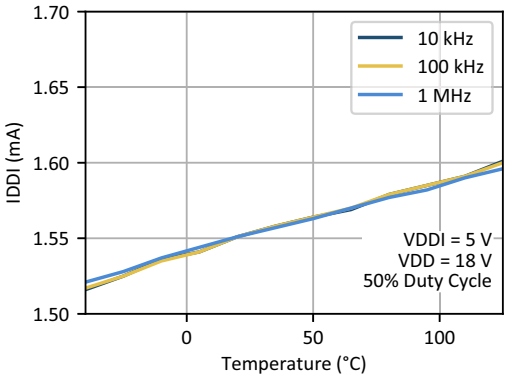


Figure 25. Logic Input Active Supply Current vs. Ambient Temperature

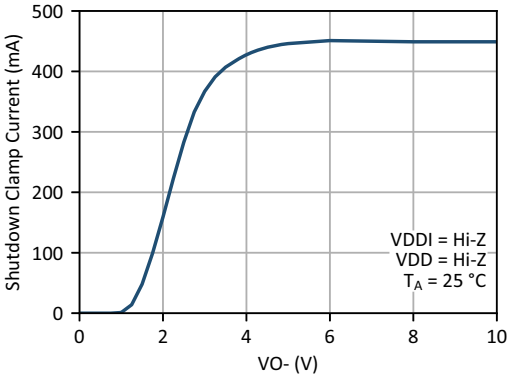


Figure 26. Shutdown Clamp Current vs. Shutdown Clamp Voltage

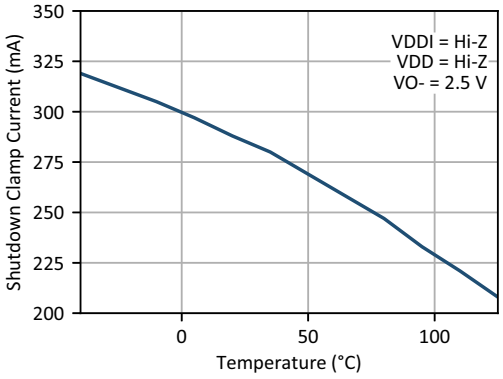


Figure 27. Shutdown Clamp Current vs. Ambient Temperature

6.3.1. 4 V UVLO (Si82CxxxGx) Devices

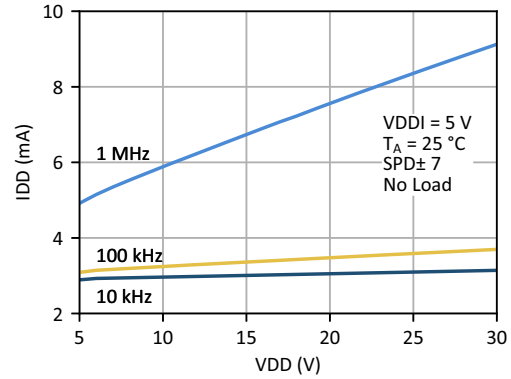


Figure 28. Gate Driver Active Supply Current vs. Gate Driver Supply Voltage

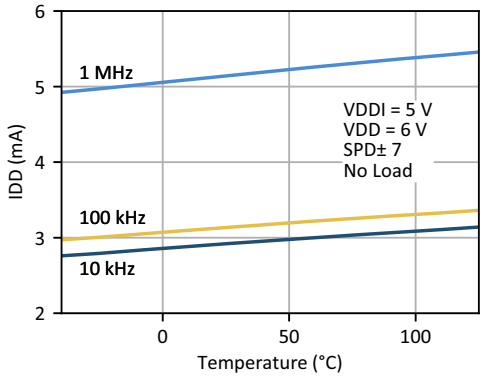


Figure 29. Gate Driver Active Supply Current vs. Ambient Temperature

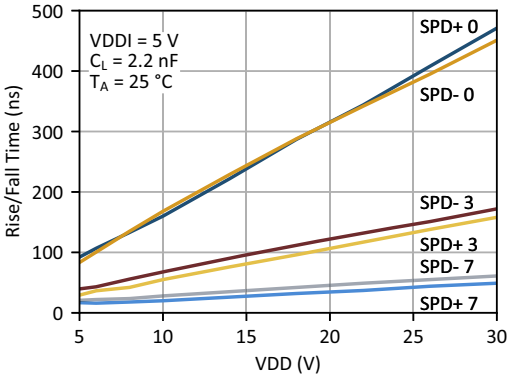


Figure 30. Output Rise/Fall Time vs. Gate Driver Supply Voltage

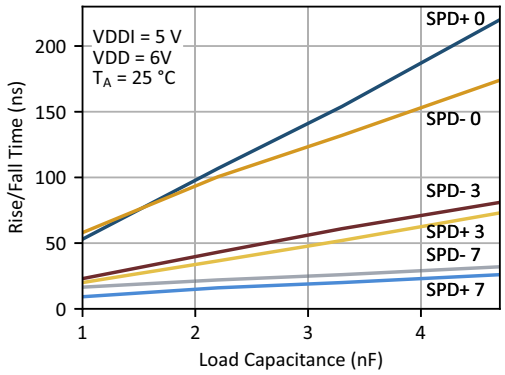


Figure 31. Output Rise/Fall Time vs. Output Load

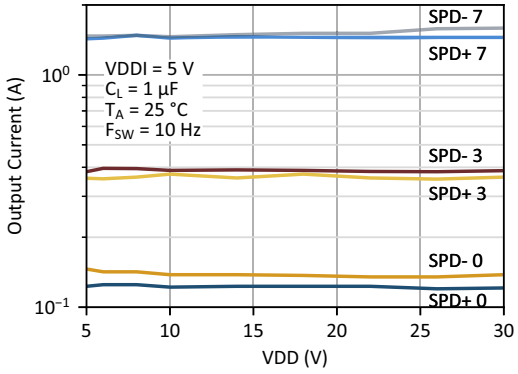


Figure 32. Output Current vs. Gate Driver Supply Voltage

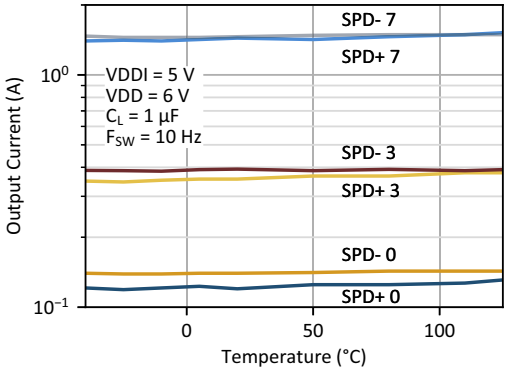


Figure 33. Output Current vs. Ambient Temperature

6.3.2. 8 V UVLO (Si82CxxxBx) Devices

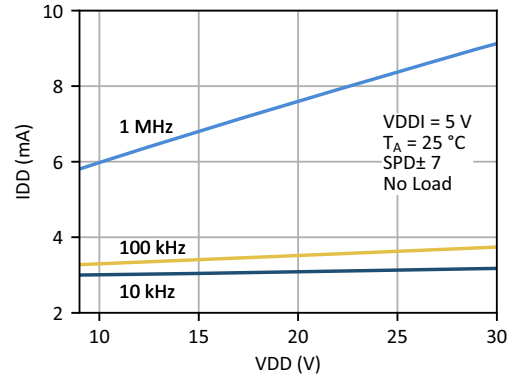


Figure 34. Gate Driver Active Supply Current vs. Gate Driver Supply Voltage

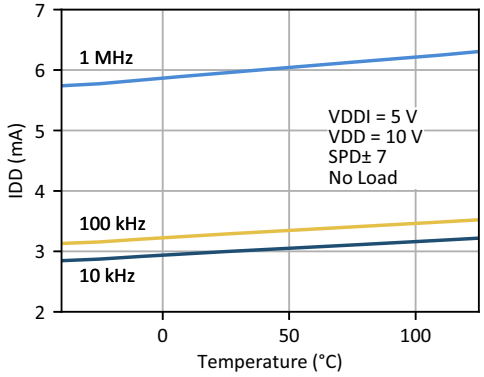


Figure 35. Gate Driver Active Supply Current vs. Ambient Temperature

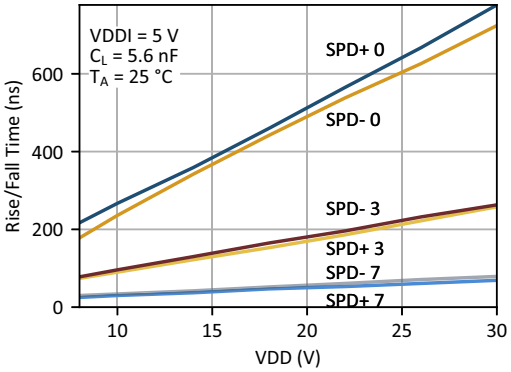


Figure 36. Output Rise/Fall Time vs. Gate Driver Supply Voltage

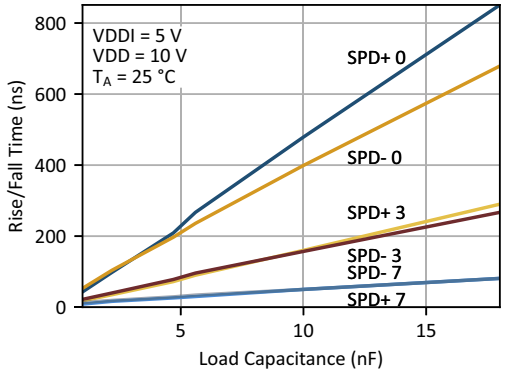


Figure 37. Output Rise/Fall Time vs. Output Load

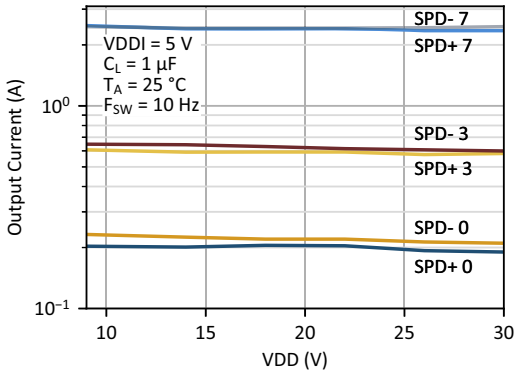


Figure 38. Output Current vs. Gate Driver Supply Voltage

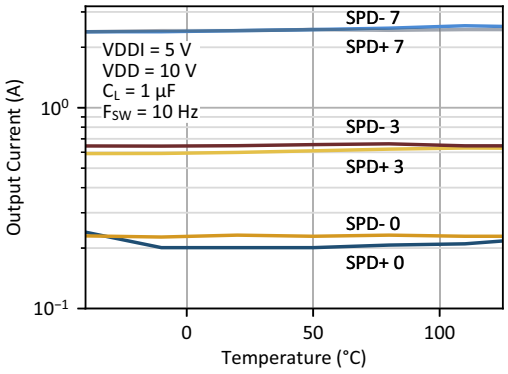


Figure 39. Output Current vs. Ambient Temperature

6.3.3. 12 V UVLO (Si82CxxxCx) Devices

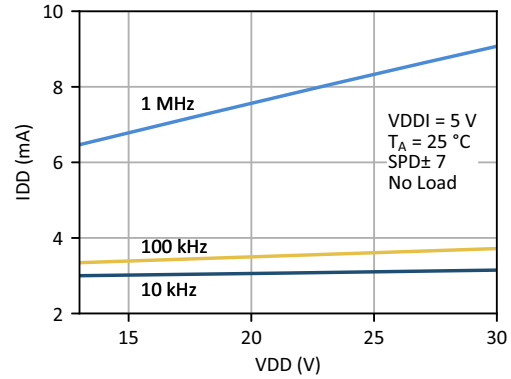


Figure 40. Gate Driver Active Supply Current vs. Gate Driver Supply Voltage

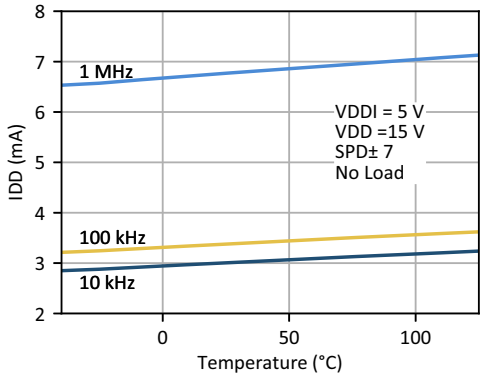


Figure 41. Gate Driver Active Supply Current vs. Ambient Temperature

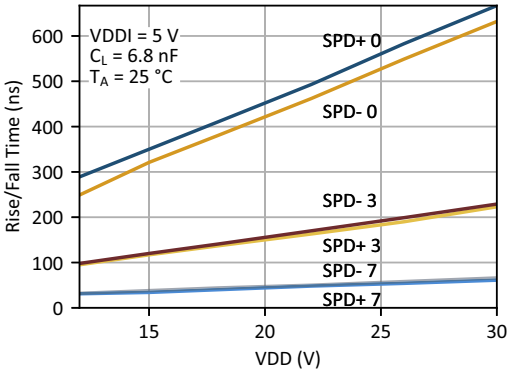


Figure 42. Output Rise/Fall Time vs. Gate Driver Supply Voltage

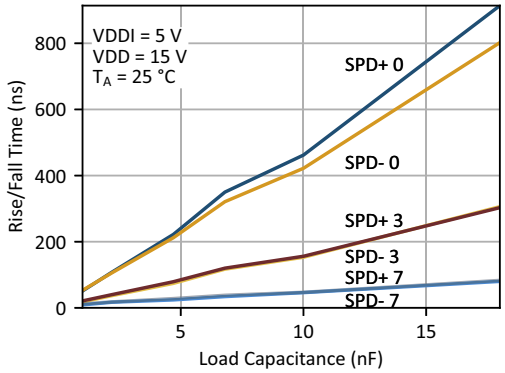


Figure 43. Output Rise/Fall Time vs. Output Load

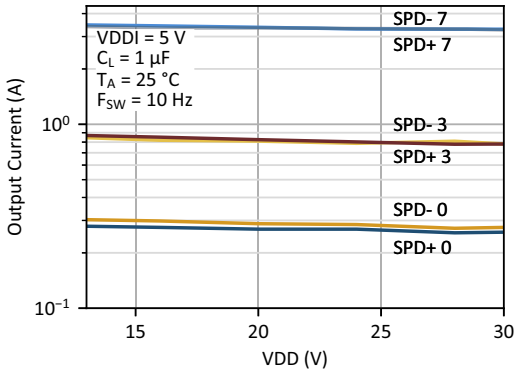


Figure 44. Output Current vs. Gate Driver Supply Voltage

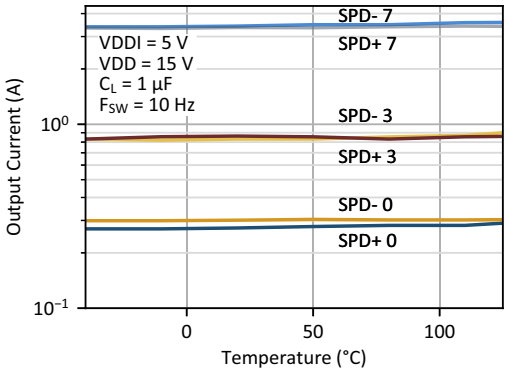


Figure 45. Output Current vs. Ambient Temperature

6.3.4. 15 V UVLO (Si82CxxxEx) Devices

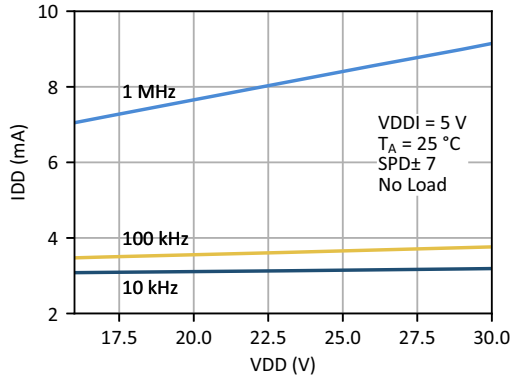


Figure 46. Gate Driver Active Supply Current vs. Gate Driver Supply Voltage

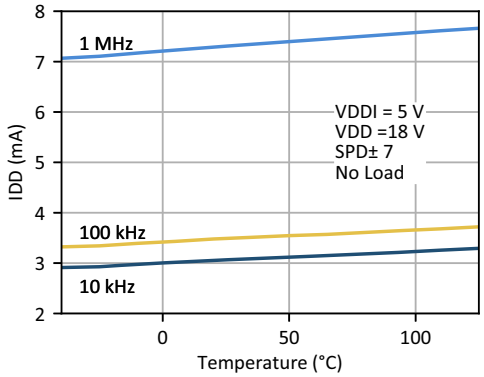


Figure 47. Gate Driver Active Supply Current vs. Ambient Temperature

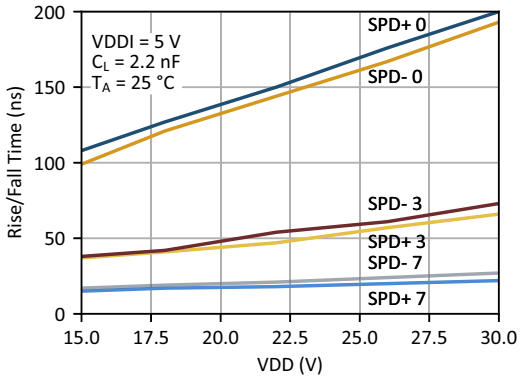


Figure 48. Output Rise/Fall Time vs. Gate Driver Supply Voltage

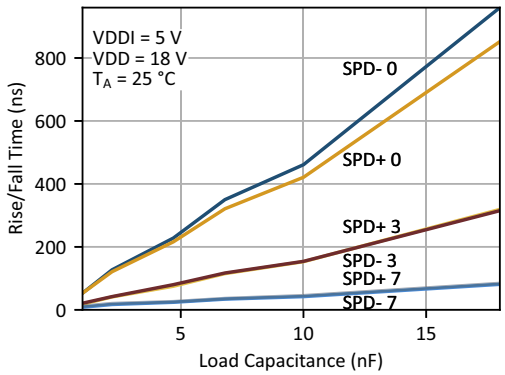


Figure 49. Output Rise/Fall Time vs. Output Load

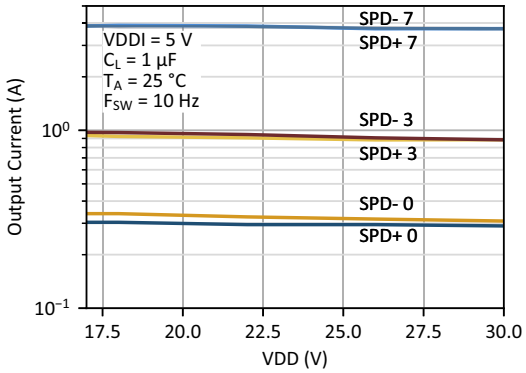


Figure 50. Output Current vs. Gate Driver Supply Voltage

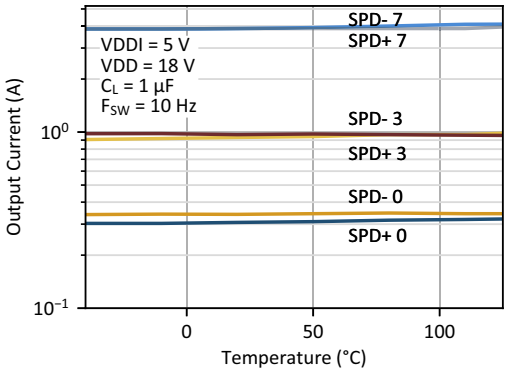


Figure 51. Output Current vs. Ambient Temperature

6.4. Thermal Characteristics

Table 8. Thermal Characteristics

Parameter	Symbol	Test Condition	NB SOIC-8	SSO-8	Unit
Thermal Resistance					
Junction-to-ambient	θ_{JA}	4-layer, 2s2p JEDEC test board	101	99	°C/W
Characterization Parameters					
Junction-to-top	Ψ_{JT}	4-layer, 2s2p JEDEC test board	9	15	°C/W
Junction-to-board	Ψ_{JB}	4-layer, 2s2p JEDEC test board	70	69	°C/W

6.5. Safety Certifications and Specifications

Table 9. Regulatory Information[1]

CSA
The Si82Cx is certified under CSA. For more details, see Master Contract Number 232873.
62368-1: Rated up to 600 V_{RMS} reinforced insulation working voltage; rated up to 1000 V_{RMS} basic insulation working voltage.
60601-1: Rated up to 250 V_{RMS} working voltage and two means of patient protection (MOPP).
VDE
The Si82Cx is certified under VDE. For more details, see File 5028467.
60747-17: Rated up to 2121 V_{PEAK} for reinforced insulation working voltage.
UL
The Si82Cx is certified under UL1577 component recognition program. For more details, see File E257455.
Rated up to 6.0 kV_{RMS} V_{ISO} isolation voltage for basic protection.
CQC
The Si82Cx is certified under GB4943.1.
Rated up to 250 V_{RMS} reinforced insulation working voltage at 5000 meters tropical climate.

1. For more information, see "10. Ordering Guide" on page 48.

Table 10. Insulation and Safety-Related Specifications

Parameter	Symbol	Test Condition	Value		Unit
			NB SOIC-8	SSO-8	
Nominal external air gap (clearance)	CLR		3.90	8.00	mm
Nominal external tracking (creepage)	CRP		3.90	8.00	mm
Minimum internal gap (internal clearance)	DTI		0.036	0.036	mm
Tracking resistance	CTI or PTI	IEC60112	600	600	V_{RMS}
Erosion depth	ED		0.031	0.040	mm
Resistance (input-output)[1]	R_{IO}	T_A = 25 °C, V_{IO} = 500 V	10^{12}	10^{12}	Ω
Capacitance (input-output)[1]	C_{IO}	f = 1 MHz	0.50	0.50	pF
Input capacitance[2]	C_I	f = 100 kHz	2.00	2.00	pF

1. To determine resistance and capacitance, the device is converted into a 2-terminal device. Pins on Side A are shorted together to form the first terminal, and pins on Side B are shorted together to form the second terminal. The parameters are then measured between these two terminals.
2. Measured from input pin to ground.

Table 11. IEC60664-1 Ratings

Parameter	Test Conditions	Specification	
		NB SOIC-8	SSO-8
Material group		I	I
Overvoltage category	Rated mains voltage ≤ 150 V_{RMS}	I-IV	I-IV
	Rated mains voltage ≤ 300 V_{RMS}	I-III	I-IV
	Rated mains voltage ≤ 600 V_{RMS}	I-II	I-IV
	Rated mains voltage ≤ 1000 V_{RMS}	I	I-III

Table 12. IEC60747-17 Insulation Characteristics[1]

Parameter	Symbol	Test Condition	Characteristic		Unit
			NB SOIC-8	SSO-8	
Maximum working isolation voltage	V_{IOWM}	According to Time-Dependent Dielectric Breakdown (TDDB) Test	445	1500	V_{RMS}
Maximum repetitive isolation voltage	V_{IORM}	According to Time-Dependent Dielectric Breakdown (TDDB) Test	630	2121	V_{PEAK}
Apparent charge	Q_{PD}	Method b: At routine test (100% production) and preconditioning (type test); V_{INI} = 1.2 x V_{IOTM}, t_{INI} = 1 s; $V_{PD(M)}$ = 1.875 x V_{IORM}, t_M = 1 s (method b1) or $V_{PD(M)}$ = V_{INI}, t_M = t_{INI} (method b2)	≤ 5	≤ 5	pC
Maximum transient isolation voltage	V_{IOTM}	V_{TEST} = V_{IOTM}, t = 60 s (qualification); V_{TEST} = 1.2 x V_{IOTM}, t = 1 s (100% production)	5302	8484	V_{PEAK}
Maximum surge isolation voltage	V_{IOSM}	Tested in oil with 1.3 x V_{IMP} or 10 kV minimum and 1.2 µs/50 µs profile (qualification)	10400	10400	V_{PEAK}
Maximum impulse voltage	V_{IMP}	Tested in air with 1.2 µs/50 µs profile (qualification)	5000	8000	V_{PEAK}
Isolation resistance	R_{IO_S}	T_A = T_S, V_{IO} = 500 V	$>10^9$	$>10^9$	Ω
Pollution degree			2	2	
Climatic category			40/125/21	40/125/21	

1. This coupler is suitable for “reinforced insulation” only within the safety limiting values. Compliance with the safety limiting values shall be ensured by means of suitable protective circuits.

Table 13. IEC60747-17 Safety Limiting Values

Parameter	Symbol	Test Condition	Max[1]		Unit
			NB SOIC-8	SSO-8	
Safety temperature	T_S		150	150	°C
Safety input, output, or supply current	I_S	Refer to θ_{JA} in “6.4. Thermal Characteristics” on page 36; VDDI = 5 V, VDD = 30 V, T_J = 150 °C, T_A = 25 °C	41.3	42.1	mA
Safety input, output, or total power	P_S	Refer to θ_{JA} in “6.4. Thermal Characteristics” on page 36; T_J = 150 °C, T_A = 25 °C	1.24	1.26	W

1. Maximum value allowed in the event of a failure; also see the temperature derating curves below.

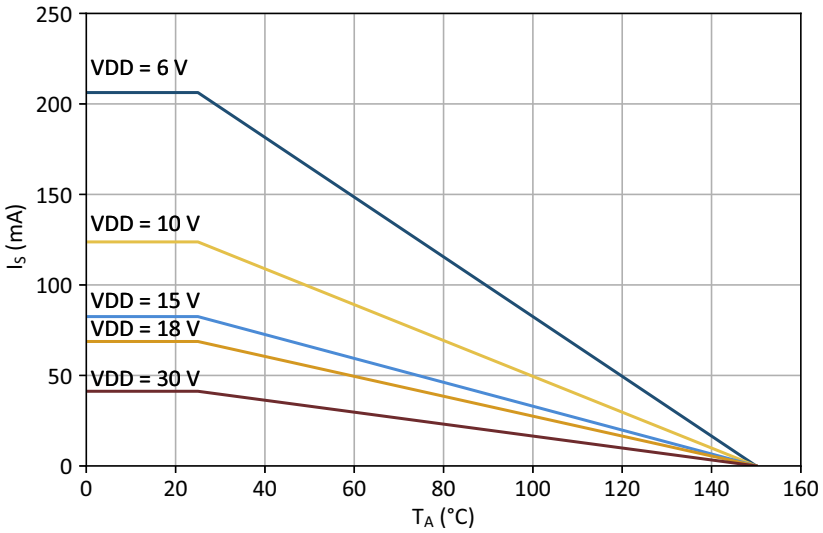


Figure 52. NB SOIC-8 Safety Current vs. Ambient Temperature Derating Curve

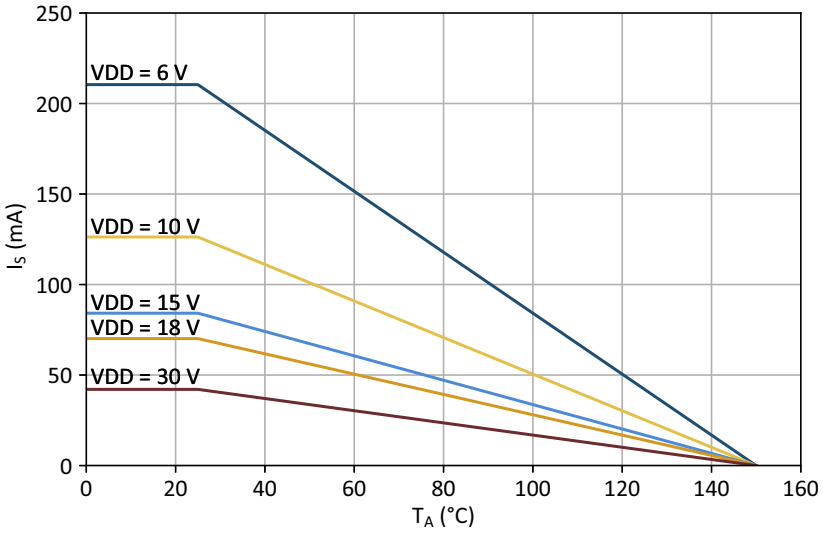


Figure 53. SSO-8 Safety Current vs. Ambient Temperature Derating Curve

Table 14. UL1577 Insulation Characteristics

Parameter	Symbol	Test Condition	Characteristic		Unit
			NB SOIC-8	SSO-8	
Maximum withstanding isolation voltage	V_{ISO}	$V_{TEST} = V_{ISO}$, t = 60 s (qualification); $V_{TEST} = 1.2 \times V_{ISO}$, t = 1 s (100% production)	3750	6000	V_{RMS}

7. Package Drawings

7.1. NB SOIC-8 Package Drawing

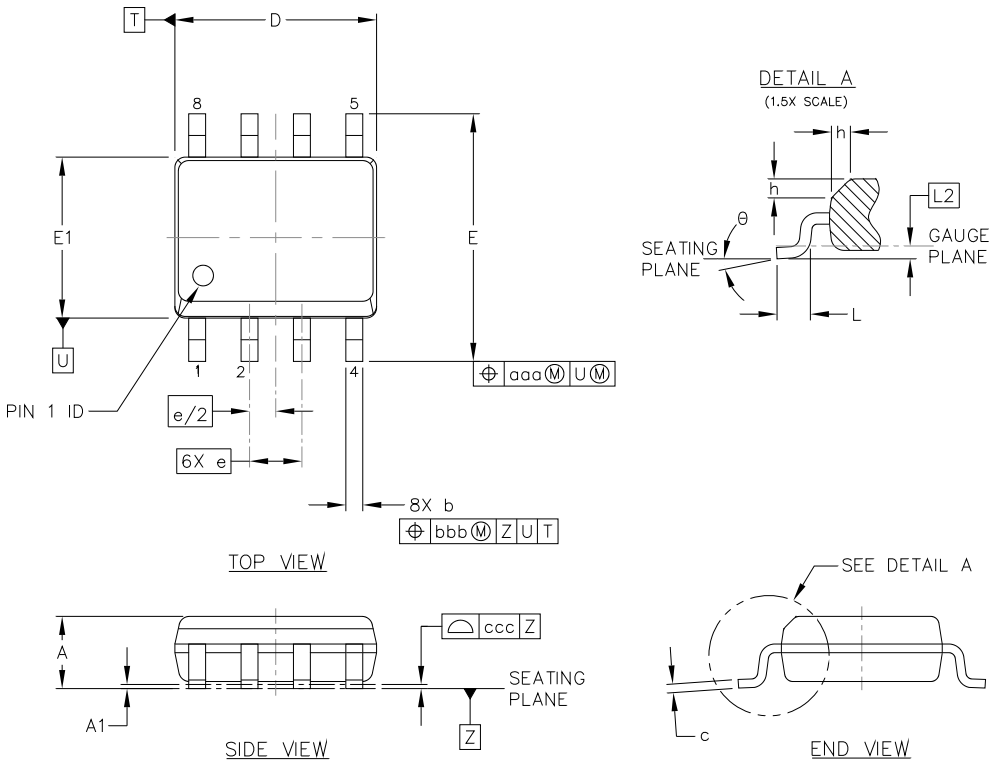


Figure 54. NB SOIC-8 Package Drawing

Table 15. NB SOIC-8 Package Drawing Dimensions[1,2,3,4,5]

Dimension	Min	Max
A	—	1.75
A1	0.10	0.25
b	0.33	0.51
c	0.19	0.25
D	4.80	5.00
E	5.80	6.20
E1	3.80	4.00
e	1.27 BSC	
L	0.40	1.27
L2	0.25 BSC	
h	0.25	0.50
θ	0°	8°

Table 15. NB SOIC-8 Package Drawing Dimensions[1,2,3,4,5] (Continued)

Dimension	Min	Max
aaa	0.10	
bbb	0.20	
ccc	0.10	

1. All dimensions shown are in millimeters (mm) unless otherwise noted.
2. Dimensioning and Tolerancing per ANSI Y14.5M.
   a. BSC: Basic Dimension. Theoretically exact shown without tolerance.
   b. REF: Reference Dimension: Usually without tolerance, for information purposes only.
3. Dimension D does not include mold flash, protrusions or gate burrs, which shall not exceed 0.15 mm per end. Dimension E1 does not include interlead flash or protrusion, which shall not exceed 0.25 mm per side.
4. This drawing conforms to the JEDEC Solid State Outline MS-137, Variation AB.
5. Recommended reflow profile per JEDEC J_STD_020 specification for small body, lead-free components.

7.2. SSO-8 Package Drawing

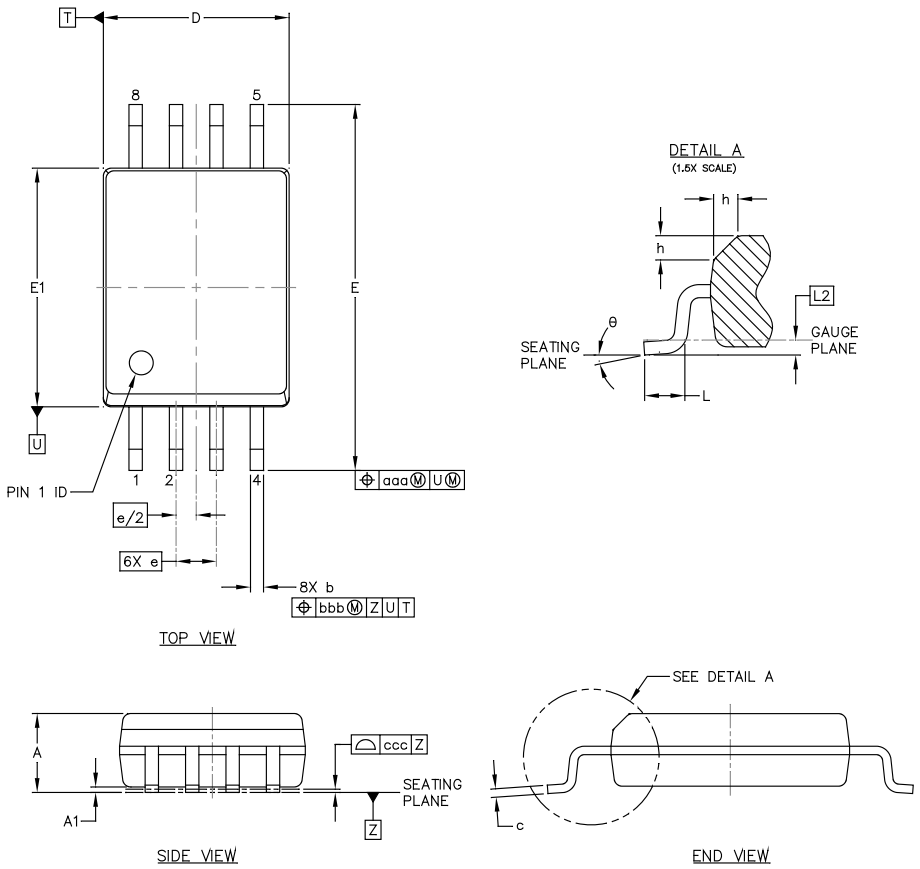


Figure 55. SSO-8 Package Drawing

Table 16. SSO-8 Package Drawing Dimensions[1,2,3,4]

Dimension	Min	Max
A	2.49	2.79
A1	0.36	0.46
b	0.30	0.51
c	0.13	0.33
D	5.74	5.94
E	11.25	11.76
E1	7.39	7.59
e	1.27 BSC	
L	0.51	1.02
L2	0.25 BSC	
h	0.25	0.76
θ	0°	8°

Table 16. SSO-8 Package Drawing Dimensions[1,2,3,4] (Continued)

Dimension	Min	Max
aaa	0.25	
bbb	0.25	
ccc	0.10	

1. All dimensions shown are in millimeters (mm) unless otherwise noted.
2. Dimensioning and Tolerancing per ANSI Y14.5M.
   a. BSC: Basic Dimension. Theoretically exact shown without tolerance.
   b. REF: Reference Dimension: Usually without tolerance, for information purposes only.
3. Dimension D does not include mold flash, protrusions or gate burrs, which shall not exceed 0.15 mm per end. Dimension E1 does not include interlead flash or protrusion, which shall not exceed 0.25 mm per side.
4. Recommended reflow profile per JEDEC J_STD_020 specification for small body, lead-free components.

8. Land Patterns

8.1. NB SOIC-8 Land Pattern

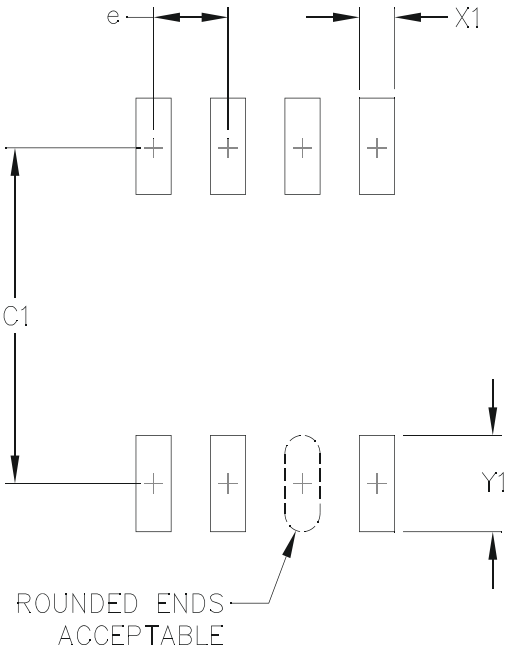


Figure 56. NB SOIC-8 Land Pattern

Table 17. NB SOIC-8 PCB Land Pattern Dimension[1,2,3]

Dimension	Feature	mm
C1	Pad Column Spacing	5.40
E	Pad Row Pitch	1.27
X1	Pad Width	0.60
Y1	Pad Length	1.55

1. All dimensions shown are in millimeters (mm) unless otherwise noted..
2. This Land Pattern Design is based on IPC-7351 pattern SOIC127P600X173-8AN for Density Level B (Median Land Protrusion).
3. All feature sizes shown are at Maximum Material Condition (MMC) and a card fabrication tolerance of 0.05 mm is assumed.

8.2. WB SSO-8 Land Pattern

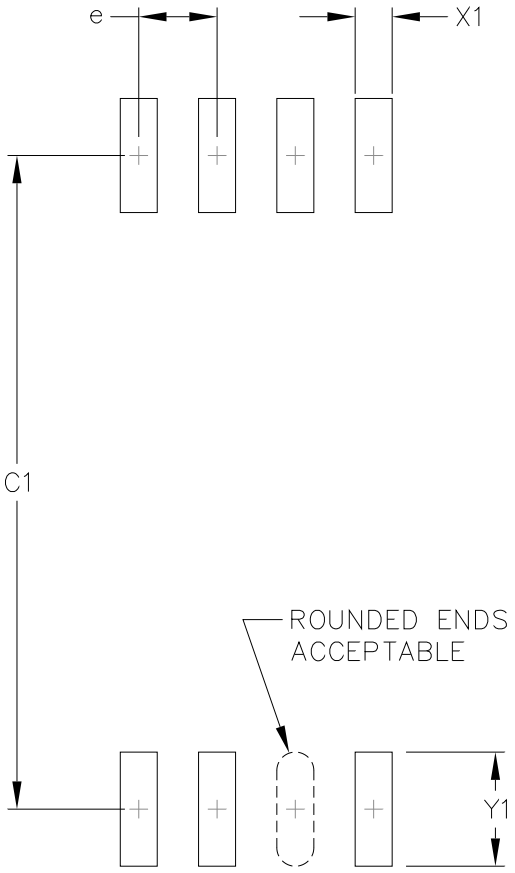


Figure 57. SSO-8 PCB Land Pattern

Table 18. SSO-8 PCB Land Pattern Dimensions[1,2,3]

Dimension	Feature	mm
C1	Pad Column Spacing	10.60
e	Pad Row Pitch	1.27
X1	Pad Width	0.60
Y1	Pad Length	1.85

1. All dimensions shown are in millimeters (mm) unless otherwise noted.
2. This Land Pattern Design is based on IPC-7351 guidelines.
3. All feature sizes shown are at Maximum Material Condition (MMC) and a card fabrication tolerance of 0.05 mm is assumed.

9. Top Markings

9.1. NB SOIC-8 Top Marking

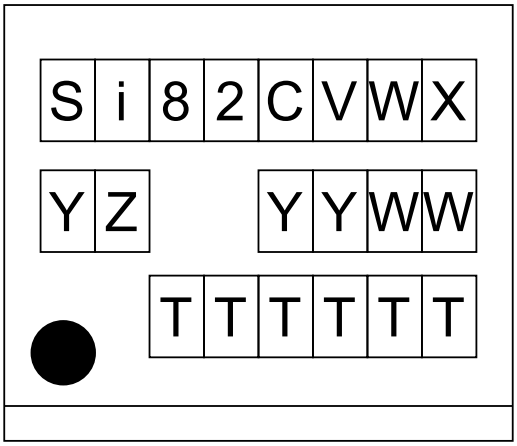


Figure 58. 8-Pin Narrow-Body SOIC Top Marking

Table 19. 8-Pin Narrow-Body SOIC Top Marking Explanation

Line 1 Marking:	Base Part Number Ordering Options (See "10. Ordering Guide" on page 48 for more information)	Si82C = One-channel Performance IsoDriver product series V = Input Pinout 5 = VI and SPD± inputs 6 = VI and SPD+ inputs 7 = VI and SPD– inputs W = Output Pinout 0 = Split Source/Sink Driver outputs X = Input Configuration A = No deglitch filter B = 30 ns deglitch filter E = 90 ns deglitch filter
Line 2 Marking:	Base Part Number Ordering Options (See "10. Ordering Guide" on page 48 for more information)	Y = Output Configuration G = 4 V UVLO B = 8 V UVLO C = 12 V UVLO E = 15 V UVLO Z = Isolation Rating C = 3.75 kV_{RMS}
	YY = Year WW = Workweek	Assigned by the assembly house. Corresponds to the year and workweek of the mold date.
Line 3 Marking:	TTTTTT = Mfg. Trace Code	Manufacturing Traceability Code The Manufacturing Traceability Code represented by "TTTTTT" contains, as its first character, a letter in the range A through M to indicate Industrial-Grade, or a letter in the range N through Z to indicate Automotive-Grade.

9.2. WB SSO-8 Top Marking

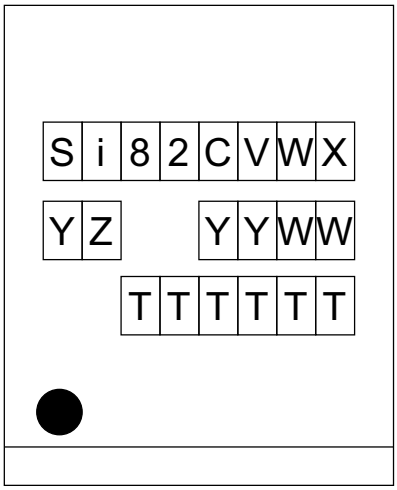


Figure 59. 8-Pin Stretched Small Outline (SSO) Top Marking

Table 20. 8-Pin Stretched Small Outline (SSO) Top Marking Explanation

Line 1 Marking:	Base Part Number Ordering Options (See "10. Ordering Guide" on page 48 for more information)	Si82C = One-channel Performance IsoDriver product series V = Input Pinout 5 = VI and SPD± inputs 6 = VI and SPD+ inputs 7 = VI and SPD– inputs W = Output Pinout 0 = Split Source/Sink Driver outputs X = Input Configuration A = No deglitch filter B = 30 ns deglitch filter E = 90 ns deglitch filter
Line 2 Marking:	Base Part Number Ordering Options (See "10. Ordering Guide" on page 48 for more information)	Y = Output Configuration B = 8 V UVLO C = 12 V UVLO E = 15 V UVLO Z = Isolation Rating E = 6.0 kV_{RMS}
	YY = Year WW = Workweek	Assigned by the assembly house. Corresponds to the year and workweek of the mold date.
Line 3 Marking:	TTTTTT = Mfg. Trace Code	Manufacturing Traceability Code The Manufacturing Traceability Code represented by "TTTTTT" contains, as its first character, a letter in the range A through M to indicate Industrial-Grade, or a letter in the range N through Z to indicate Automotive-Grade.

10. Ordering Guide

Table 21. Si82Cx Ordering Guide[1,2,3,4,5,6,7]

Ordering Part Number (OPN)	Automotive OPN	Inputs	Outputs	Deglitch Filter	Undervoltage Lockout (UVLO)	Isolation Rating	Package Type
NB SOIC-8 Package Options							
Si82C50AGC-IS	Si82C50AGC-AS	VI, SPD±	VO+, VO–	NA	4 V	3.75 kV_{RMS}	NB SOIC-8
Si82C50ABC-IS	Si82C50ABC-AS	VI, SPD±	VO+, VO–	NA	8 V	3.75 kV_{RMS}	NB SOIC-8
Si82C50ACC-IS	Si82C50ACC-AS	VI, SPD±	VO+, VO–	NA	12 V	3.75 kV_{RMS}	NB SOIC-8
Si82C50AEC-IS	Si82C50AEC-AS	VI, SPD±	VO+, VO–	NA	15 V	3.75 kV_{RMS}	NB SOIC-8
Si82C50BGC-IS	Si82C50BGC-AS	VI, SPD±	VO+, VO–	30 ns	4 V	3.75 kV_{RMS}	NB SOIC-8
Si82C50BBC-IS	Si82C50BBC-AS	VI, SPD±	VO+, VO–	30 ns	8 V	3.75 kV_{RMS}	NB SOIC-8
Si82C50BCC-IS	Si82C50BCC-AS	VI, SPD±	VO+, VO–	30 ns	12 V	3.75 kV_{RMS}	NB SOIC-8
Si82C50BEC-IS	Si82C50BEC-AS	VI, SPD±	VO+, VO–	30 ns	15 V	3.75 kV_{RMS}	NB SOIC-8
Si82C50ECC-IS	Si82C50ECC-AS	VI, SPD±	VO+, VO–	90 ns	12 V	3.75 kV_{RMS}	NB SOIC-8
Si82C50EEC-IS	Si82C50EEC-AS	VI, SPD±	VO+, VO–	90 ns	15 V	3.75 kV_{RMS}	NB SOIC-8
Si82C60AGC-IS	Si82C60AGC-AS	VI, SPD+	VO+, VO–	NA	4 V	3.75 kV_{RMS}	NB SOIC-8
Si82C60ABC-IS	Si82C60ABC-AS	VI, SPD+	VO+, VO–	NA	8 V	3.75 kV_{RMS}	NB SOIC-8
Si82C60ACC-IS	Si82C60ACC-AS	VI, SPD+	VO+, VO–	NA	12 V	3.75 kV_{RMS}	NB SOIC-8
Si82C60AEC-IS	Si82C60AEC-AS	VI, SPD+	VO+, VO–	NA	15 V	3.75 kV_{RMS}	NB SOIC-8
Si82C70AGC-IS	Si82C70AGC-AS	VI, SPD–	VO+, VO–	NA	4 V	3.75 kV_{RMS}	NB SOIC-8
Si82C70ABC-IS	Si82C70ABC-AS	VI, SPD–	VO+, VO–	NA	8 V	3.75 kV_{RMS}	NB SOIC-8
Si82C70ACC-IS	Si82C70ACC-AS	VI, SPD–	VO+, VO–	NA	12 V	3.75 kV_{RMS}	NB SOIC-8
Si82C70AEC-IS	Si82C70AEC-AS	VI, SPD–	VO+, VO–	NA	15 V	3.75 kV_{RMS}	NB SOIC-8

Table 21. Si82Cx Ordering Guide[1,2,3,4,5,6,7]

Ordering Part Number (OPN)	Automotive OPN	Inputs	Outputs	Deglitch Filter	Undervoltage Lockout (UVLO)	Isolation Rating	Package Type
WB SSO-8 Package Options							
Si82C50ABE-IS4	Si82C50ABE-AS4	VI, SPD±	VO+, VO–	NA	8 V	6 kV_{RMS}	SSO-8
Si82C50ACE-IS4	Si82C50ACE-AS4	VI, SPD±	VO+, VO–	NA	12 V	6 kV_{RMS}	SSO-8
Si82C50AEE-IS4	Si82C50AEE-AS4	VI, SPD±	VO+, VO–	NA	15 V	6 kV_{RMS}	SSO-8
Si82C50BBE-IS4	Si82C50BBE-AS4	VI, SPD±	VO+, VO–	30 ns	8 V	6 kV_{RMS}	SSO-8
Si82C50BCE-IS4	Si82C50BCE-AS4	VI, SPD±	VO+, VO–	30 ns	12 V	6 kV_{RMS}	SSO-8
Si82C50BEE-IS4	Si82C50BEE-AS4	VI, SPD±	VO+, VO–	30 ns	15 V	6 kV_{RMS}	SSO-8
Si82C50ECE-IS4	Si82C50ECE-AS4	VI, SPD±	VO+, VO–	90 ns	12 V	6 kV_{RMS}	SSO-8
Si82C50EEE-IS4	Si82C50EEE-AS4	VI, SPD±	VO+, VO–	90 ns	15 V	6 kV_{RMS}	SSO-8
Si82C60ABE-IS4	Si82C60ABE-AS4	VI, SPD+	VO+, VO–	NA	8 V	6 kV_{RMS}	SSO-8
Si82C60ACE-IS4	Si82C60ACE-AS4	VI, SPD+	VO+, VO–	NA	12 V	6 kV_{RMS}	SSO-8
Si82C60AEE-IS4	Si82C60AEE-AS4	VI, SPD+	VO+, VO–	NA	15 V	6 kV_{RMS}	SSO-8
Si82C70ABE-IS4	Si82C70ABE-AS4	VI, SPD–	VO+, VO–	NA	8 V	6 kV_{RMS}	SSO-8
Si82C70ACE-IS4	Si82C70ACE-AS4	VI, SPD–	VO+, VO–	NA	12 V	6 kV_{RMS}	SSO-8
Si82C70AEE-IS4	Si82C70AEE-AS4	VI, SPD–	VO+, VO–	NA	15 V	6 kV_{RMS}	SSO-8

1. “Si” and “SI” are used interchangeably.
2. An “R” at the end of the Ordering Part Number indicates tape and reel packaging option.
3. All packages are RoHS-compliant with peak reflow temperatures of 260 °C according to the JEDEC industry standard classifications and peak solder temperatures.
4. The Speed pins, SPD±, SPD+, and SPD–, also serve as active-high device DISABLE signals. See “1.2. Pin Details” on page 5.
5. VO+ and VO– outputs denote that the device sources current out of the VO+ pin and sinks current into the VO– pin.
6. Automotive-Grade devices (with an “-A” suffix) are identical in construction materials and electrical parameters to their Industrial Grade (with an “-I” suffix) version counterparts. Automotive-Grade products are produced utilizing full automotive process flows and additional statistical process controls throughout the manufacturing flow. The Automotive-Grade part number is included on shipping labels.
7. In Top Markings, the Manufacturing Code represented by either “RTTTTT” or “TTTTTT” contains as its first character a letter in the range N through Z to indicate Automotive-Grade.

11. Revision History

Revision	Date	Description
A	January, 2025	Initial release.