PRELIMINARY DATA SHEET

Si82Bx Single-Channel Isolated Gate Driver with 6 Amp Drive and Miller Clamp

The Si82Bx is a family of single-channel isolated gate drivers for high-power applications. The Si82Bx series comprises devices with either a single output or split outputs, with the split output configuration allowing for independent control of the output rise and fall times. These drivers can operate with a 3 to 20 V input supply and a maximum gate driver supply voltage of 30 V. The inputs are CMOS, which provides robust noise margin.

The Si82Bx is ideal for driving power silicon MOSFETs, IGBTs, and SiC FETs, and GaN FETs used in various switched power and motor control applications. These drivers utilize Skyworks' proprietary silicon isolation technology, supporting up to 6 kV_{RMS} for one minute isolation voltage. This technology enables high CMTI (200 kV/µs), lower propagation delays and skew, little variation with temperature and age, and tight part-to-part matching. The Si82Bx family offers longer service life and higher reliability than optocoupled gate drivers.

The output stage operates as a voltage source with robust current output across operating conditions. The output stage features voltage mode drive technology using a familiar current-limiting resistor, allowing a power designer to optimize for switching speed, emissions control, and overshoot limitation. The driver family also offers features, such as integrated Miller clamp for clamping any Miller current effects, Undervoltage Lockout (UVLO), input overlap protection, and defined output states in all operating conditions.

Automotive grade is available. These products are built using automotive-specific flows at all steps in the manufacturing process to ensure the robustness and low defectivity required for automotive applications.

Applications

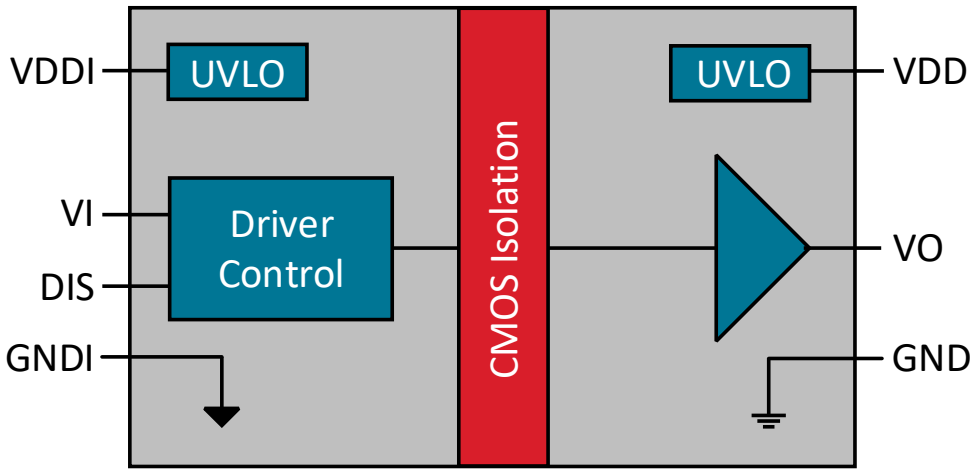
- Si MOSFET and IGBT, SiC, and GaN gate drive
- UPS inverters
- Onboard chargers
- Solar (PV) inverters
- Motor drives

Safety Regulator Approvals (Pending)

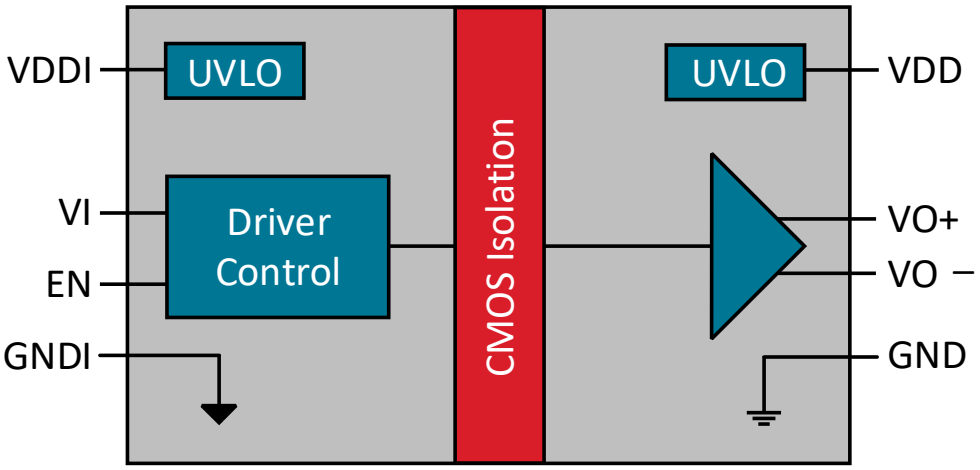
- UL 1577 recognized
  - Up to 6000 V_{RMS} for one minute
- CSA certification conformity
  - 62368-1 (reinforced insulation)
  - 60601-1 (2 MOPP)
- VDE certification conformity
  - 60747-17 (reinforced insulation)
- CQC certification approval
  - GB4943.1 (reinforced insulation)

Key Features

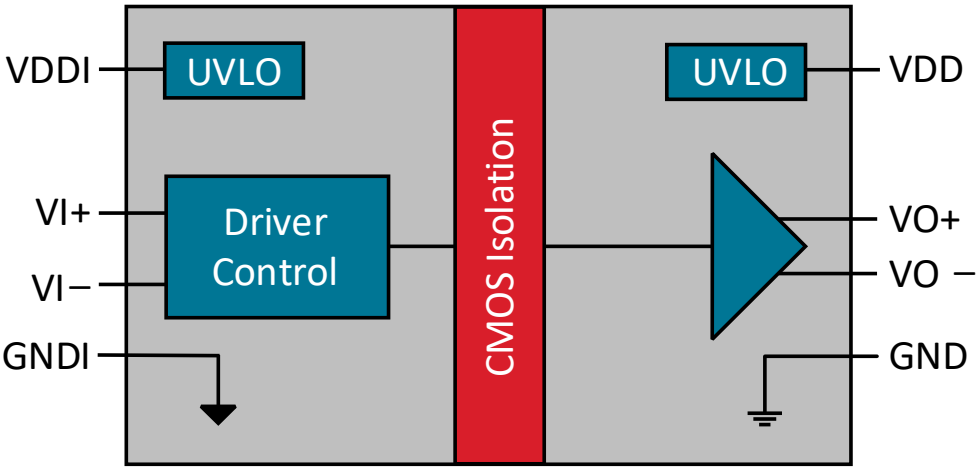
- Wide input range of 3 to 20 V
- Wide gate supply voltage of 5 to 30 V
- CMOS input with a selectable deglitch filter
- Overlap protection with VI+/VI– inputs
- Safety by default with VI/EN inputs
- Voltage mode drive
- Integrated Miller clamp option
- Unipolar or bipolar output voltages
- CMTI > 200 kV/µs
- 1500 V_{RMS} working voltage
- Optimized UVLOs of 4 V, 8 V, 12 V, and 15 V
- 4 kV HBM ESD rating
- No unknown output states
- <40 ns propagation delay with 5 ns part-to-part skew
- 6 kV_{RMS} safety rated isolation
- 10 kV bipolar surge
- Wide temperature range: –40 to 125 °C
- Narrow-body 8-pin SOIC and Stretched Small Outline (SSO) 8-pin packages
- AEC-Q100 qualification
- Automotive-grade OPNs available
- For RoHS and other product compliance information, see the Skyworks Certificate of Conformance.



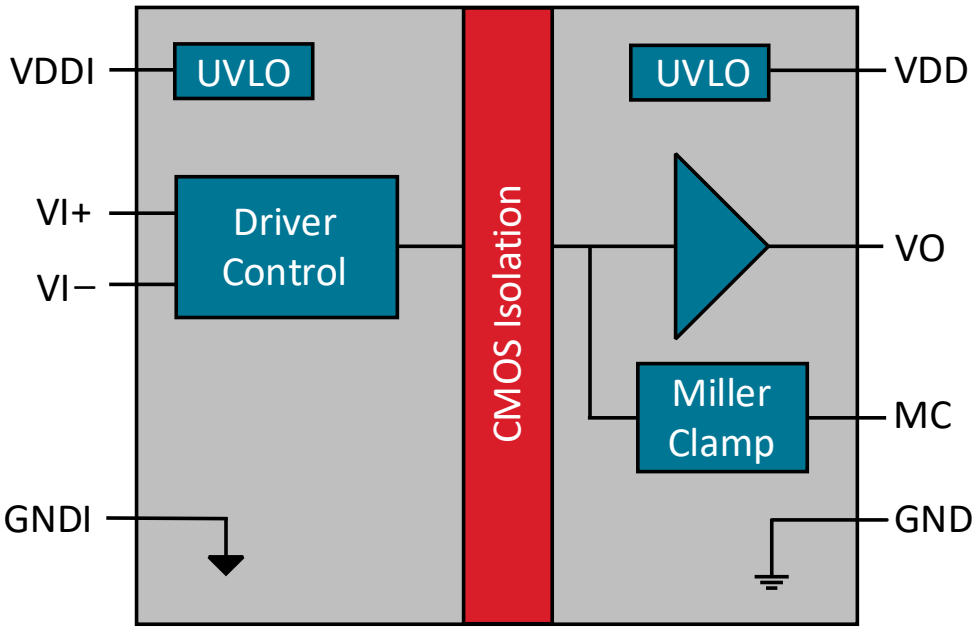
Si82B28x



Si82B30x



Si82B40x/43x



Si82B41x/44x/47x

1. Pin Descriptions

1.1. Device Pinouts

The Si82Bx consists of multiple die in packages with different bond-outs for different customer needs. Each bond-out corresponds to a pin-out below. See “10. Ordering Guide” on page 46 for the part numbers and features of these products.

1.1.1. NB SOIC-8 Pinouts

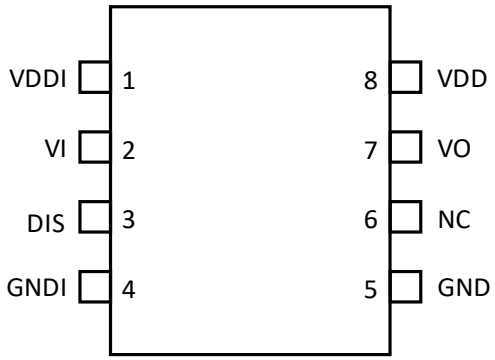


Figure 1. Si82B28x Pinout

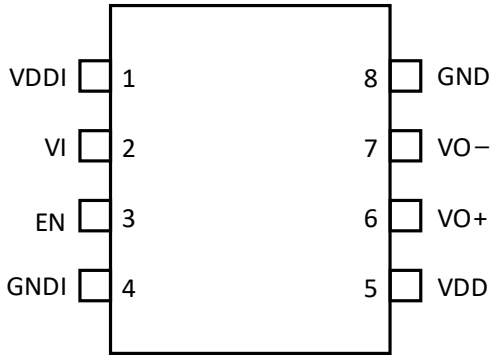


Figure 2. Si82B30x Pinout

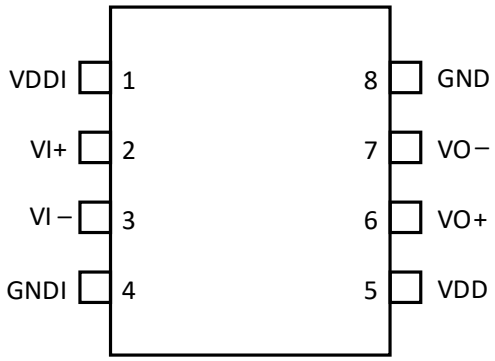


Figure 3. Si82B40x Pinout

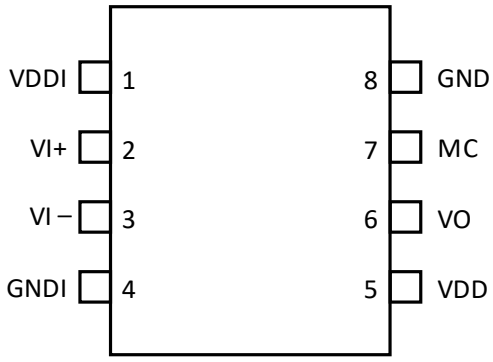


Figure 4. Si82B41x Pinout

1.1.2. SSO-8 Pinouts

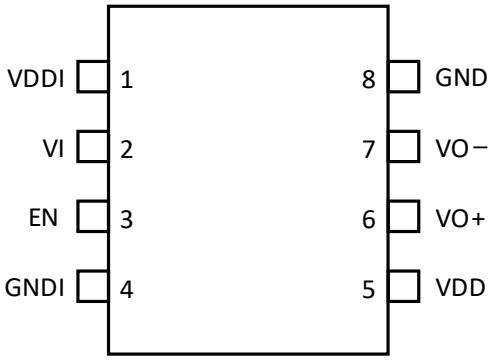


Figure 5. Si82B30x Pinout

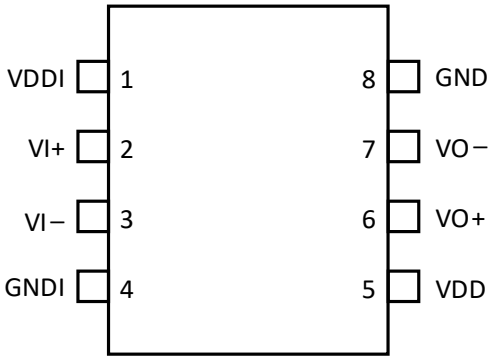


Figure 6. Si82B40x Pinout

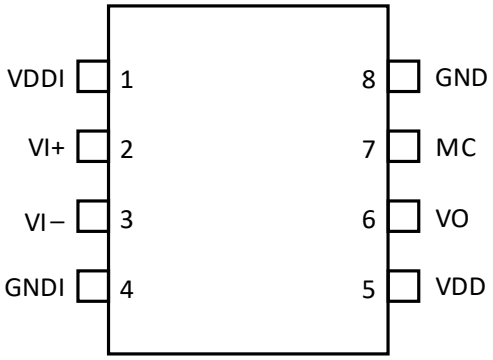


Figure 7. Si82B41x Pinout

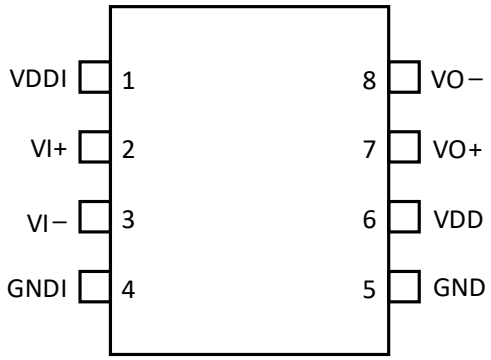


Figure 8. Si82B43x Pinout

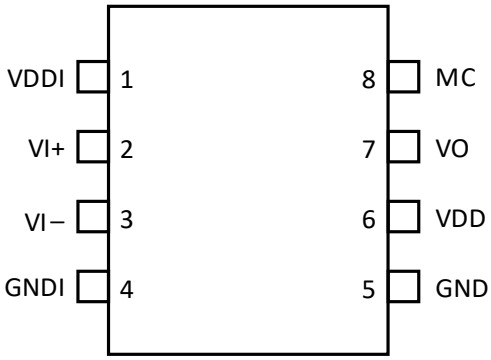


Figure 9. Si82B44x Pinout

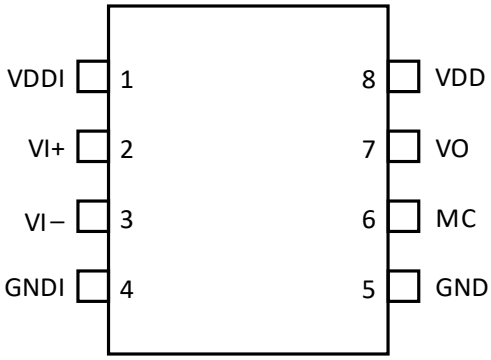


Figure 10. Si82B47x Pinout

1.2. Pin Details

Table 1. Si82Bx Pin Details

Pin Name	Pin Description
VDDI	Logic input power supply.
GNDI	Logic input ground terminal.
VI	Non-inverting logic input terminal for the gate driver.
VI+	Non-inverting complementary logic input terminal for the gate driver. Connect to VDDI when using the inverting input alone, or it should be connected to the inverting input of the HI/LO side driver in a half-bridge configuration for overlap protection.
VI–	Inverting complementary logic input terminal for the gate driver. Connect to GNDI when using the non-inverting input alone, or it should be connected to the non-inverting input of the HI/LO side driver in a half-bridge configuration for overlap protection.
EN	Active high device ENABLE signal. When asserted (logic high), the device is enabled to perform in normal operating mode. When de-asserted (logic low), this input unconditionally drives the output logic low. See 4.1. "Truth Tables" and 4.4. "Logic Input Signals" for more details.
DIS	Active high device DISABLE signal. When asserted (logic high), the device is enabled to perform in normal operating mode. When de-asserted (logic low), this input unconditionally drives VO/VO– low and VO+ High-Z. See 4.1. "Truth Tables" and 4.4. "Logic Input Signals" for more details.
VDD	Gate driver power supply.
GND	Gate driver ground terminal.
VO	Combined pull-up and pull-down output for the gate driver.
VO+	Split pull-up (sourcing) output for the gate driver.
VO–	Split pull-down (sinking) output for the gate driver.
MC	Active Miller clamp pull-down output.

2. Device Overview

The Si82Bx is an isolated single-channel gate driver that comes in three configurations: single output, single output with a separate Miller clamp pin, and split output. Each configuration can be purchased with either an asynchronous enable or disable input. Additional features such as undervoltage lockout (UVLO) level and deglitch filter time can be configured through device selection. Refer to 10. "Ordering Guide" for more details. Safety-rated isolation is provided from logic input to gate driver output by a pair of high-voltage silicon dioxide (SiO_2) capacitors. These capacitors are duplicated to form a differential path for signals modulated with an RF carrier and using an on-off keying (OOK) modulation scheme. This optimizes for fault tolerance and timing performance between input and output.

The digital logic inputs are high-voltage capable, CMOS-compatible, Schmitt triggered, and deglitched for high noise immunity and a wide range of compatibility. See Logic Input Signals for more details. Devices with an active Miller clamp pin can aid in preventing unintentional or false gate turn-on. See “4.5. Active Miller Clamp” on page 15 for more information. The gate driver output operates as a voltage source. Output current is adjusted through the selection of gate resistors. See “5.1. Recommended Application Circuits” on page 19 for more information.

3. Functional Block Diagrams

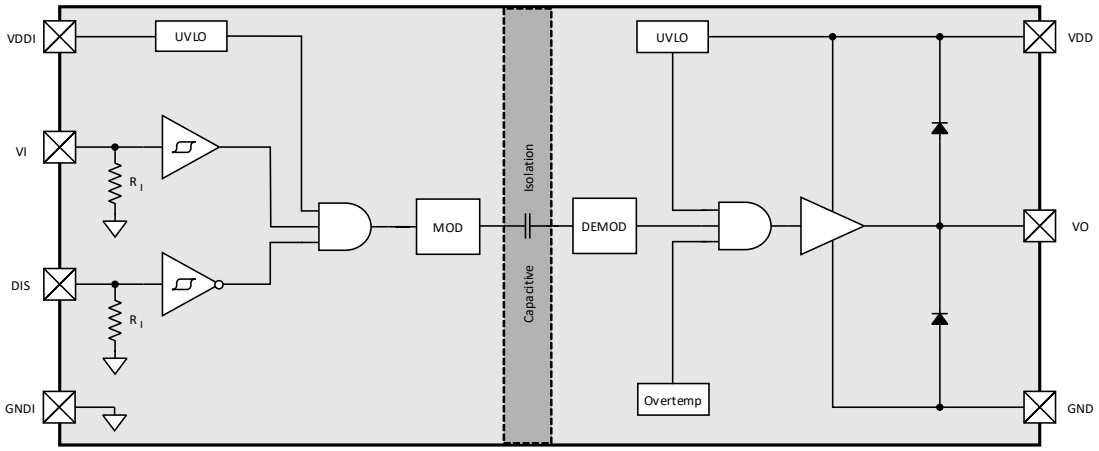


Figure 11. Si82B28x Device with Single Output and Disable Input

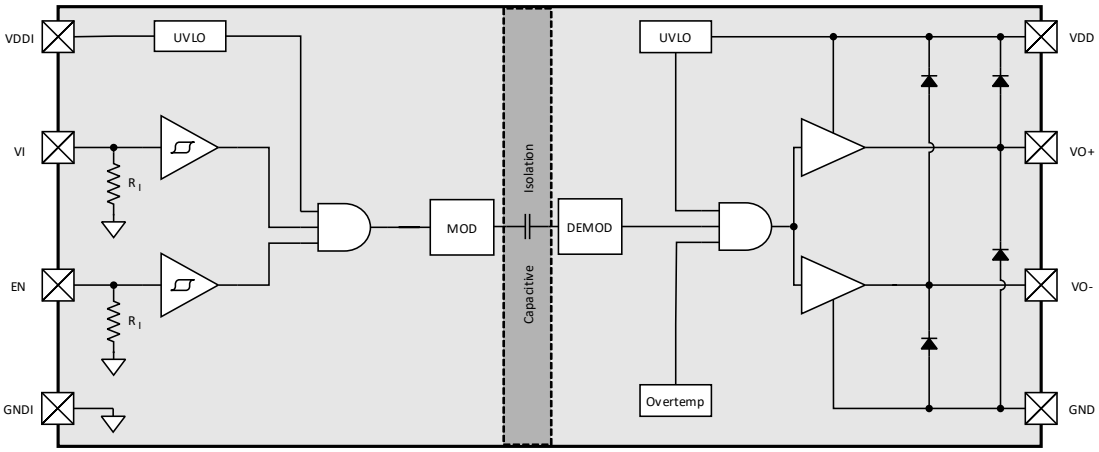


Figure 12. Si82B30x with Split Output and Enable Input

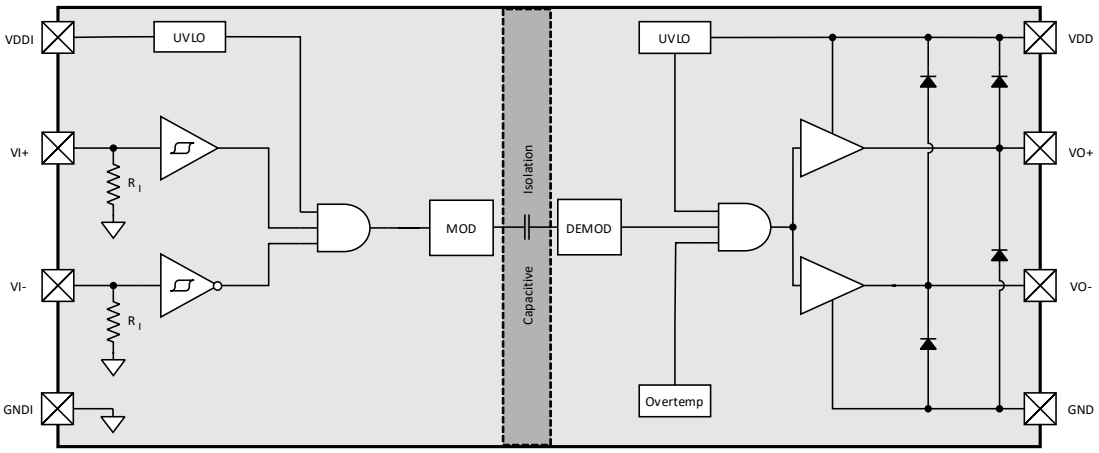


Figure 13. Si82B40x/43x with Split Output and Complementary Input

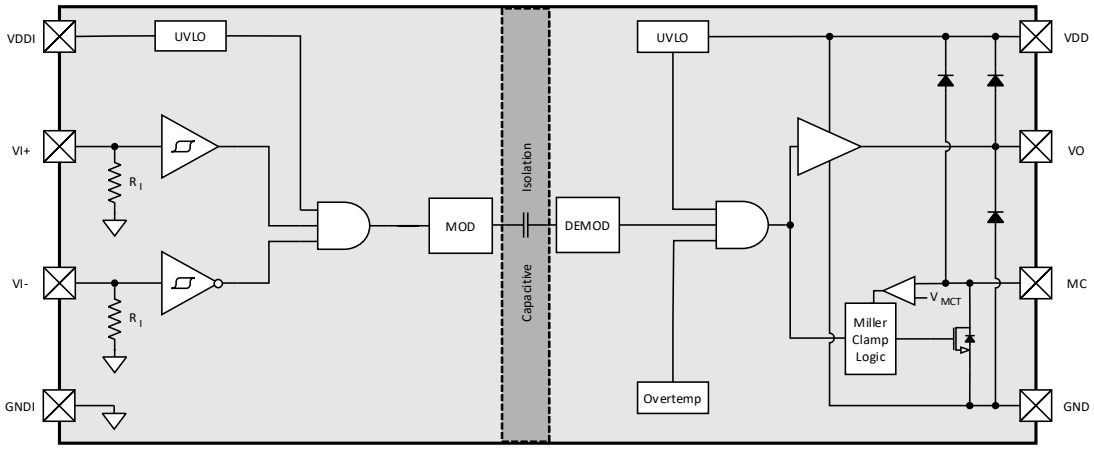


Figure 14. Si82B41x/44x/47x Device with Miller Clamp and Complementary Input

4. Device Operation

This section describes the capabilities of the device and how it should be used to achieve different goals within a design. Refer to 5.1. "Recommended Application Circuits" and 10. "Ordering Guide" for information on how to best utilize each device for different applications.

4.1. Truth Tables

The following tables describe the logical behavior of the Si82Bx Isolated Gate Driver devices.

Table 2. Si82B28x Truth Table

Inputs[1]		Power Supply State[2]		Output[3]
VI	DIS	VDDI[4]	VDD[5]	VO
H	L	P	P	H
L	X	—	—	L
X	H	—	—	L
X	X	—	NP	L

1. "X" is any logic value; "H" is a logic high (true) value, and "L" is a logic low (false) value. Input pins should always be connected to either logic high or low. Logic values listed in this table are assumed to transition at the same time as the power supply state.
2. "NP" is the "not powered" state; "P" is the "powered" state, and "—" is an irrelevant state.
3. "H" is a logic high (true) value, and "L" is a logic low (false). The logic low (L) value is enforced by the shutdown clamp (see "4.8. Shutdown Clamp" on page 16) if the gate driver's power supply (VDD) is not powered (NP).
4. "Not powered" (NP) state is defined as VDDI < $VDDI_{UV}$. "Powered" (P) state is defined as VDDI > $VDDI_{UV}$.
5. "Not powered" (NP) state is defined as VDD < VDD_{UV}. "Powered" (P) state is defined as VDD > VDD_{UV}.

Table 3. Si82B30x Truth Table

Inputs[1]		Power Supply State[2]		Outputs[3]	
VI	EN	VDDI[4]	VDD[5]	VO+	VO–
H	H	P	P	H	High-Z
L	X	—	—	High-Z	L
X	L	—	—	High-Z	L
X	X	—	NP	High-Z	L

1. "X" is any logic value; "H" is a logic high (true) value, and "L" is a logic low (false) value. Input pins should always be connected to either logic high or low. Logic values listed in this table are assumed to transition at the same time as the power supply state.
2. "NP" is the "not powered" state; "P" is the "powered" state, and "—" is an irrelevant state.
3. "H" is a logic high (true) value, and "L" is a logic low (false). The logic low (L) value is enforced by the shutdown clamp (see "4.8. Shutdown Clamp" on page 16) if the gate driver's power supply (VDD) is not powered (NP).
4. "Not powered" (NP) state is defined as VDDI < $VDDI_{UV}$. "Powered" (P) state is defined as VDDI > $VDDI_{UV}$.
5. "Not powered" (NP) state is defined as VDD < VDD_{UV}. "Powered" (P) state is defined as VDD > VDD_{UV}.

Table 4. Si82B41x/44x/47x Truth Table

Inputs[1]		Power Supply State[2]		Outputs[3]	
VI+	VI–	VDDI[4]	VDD[5]	VO	MC
H	L	P	P	H	High-Z
L	X	—	—	L	L
X	H	—	—	L	L
X	X	—	NP	L	L

1. “X” is any logic value; “H” is a logic high (true) value, and “L” is a logic low (false) value. Input pins should always be connected to either logic high or low. Logic values listed in this table are assumed to transition at the same time as the power supply state.
2. “NP” is the “not powered” state; “P” is the “powered” state, and “—” is an irrelevant state.
3. “H” is a logic high (true) value, and “L” is a logic low (false). The logic low (L) value is enforced by the shutdown clamp (see “4.8. Shutdown Clamp” on page 16) if the gate driver's power supply (VDD) is not powered (NP).
4. “Not powered” (NP) state is defined as VDDI < $VDDI_{UV}$. “Powered” (P) state is defined as VDDI > $VDDI_{UV}$.
5. “Not powered” (NP) state is defined as VDD < VDD_{UV}. “Powered” (P) state is defined as VDD > VDD_{UV}.

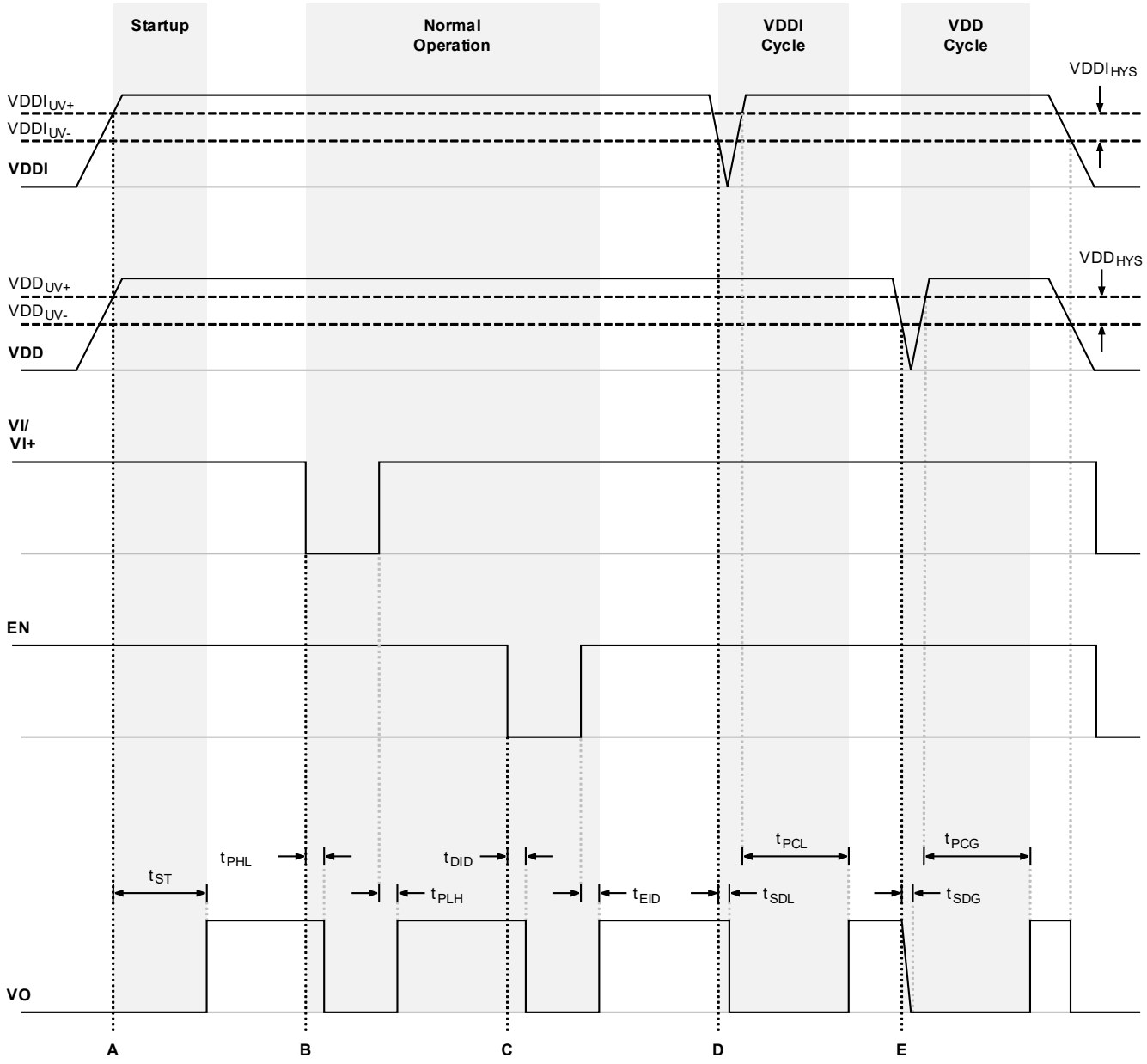
Table 5. Si82B40x/43x Truth Table

Inputs[1]		Power Supply State[2]		Outputs[3]	
VI+	VI–	VDDI[4]	VDD[5]	VO+	VO–
H	L	P	P	H	High-Z
L	X	—	—	High-Z	L
X	H	—	—	High-Z	L
X	X	—	NP	High-Z	L

1. “X” is any logic value; “H” is a logic high (true) value, and “L” is a logic low (false) value. Input pins should always be connected to either logic high or low. Logic values listed in this table are assumed to transition at the same time as the power supply state.
2. “NP” is the “not powered” state; “P” is the “powered” state, and “—” is an irrelevant state.
3. “H” is a logic high (true) value, and “L” is a logic low (false). The logic low (L) value is enforced by the shutdown clamp (see “4.8. Shutdown Clamp” on page 16) if the gate driver's power supply (VDD) is not powered (NP).
4. “Not powered” (NP) state is defined as VDDI < $VDDI_{UV}$. “Powered” (P) state is defined as VDDI > $VDDI_{UV}$.
5. “Not powered” (NP) state is defined as VDD < VDD_{UV}. “Powered” (P) state is defined as VDD > VDD_{UV}.

4.2. Power Sequence and Timing Behavior

The device exhibits different timing behavior depending on the state of the power supplies, as well as the driver inputs. In the figure below, the analog power supply voltages are plotted against the digital input and output state of the device, with relevant device timings listed.



VI- = Logic low
VO = VO+ and VO- combined or VO and MC combined

Figure 15. Gate Driver Timing Behavior

4.3. Undervoltage Lockout

Undervoltage Lockout (UVLO) is provided to prevent erroneous operation during device startup and shutdown or when VDDI or VDD is below its specified operating circuits range. The power supplies associated with the logic input and the gate driver each have undervoltage lockout monitors. The device's logic input enters UVLO when VDDI ≤ $VDDI_{UV-}$, and exits UVLO when VDDI > $VDDI_{UV+}$. The gate driver outputs, VO/VO–, remain low, and VO+ remains High-Z when the logic input supply of the device is in UVLO while its respective power supply (VDD) is within the specified range. The gate driver outputs, VO/VO–, remain low and VO+ remains High-Z when VDD falls below VDD_{UV-} and exit UVLO when VDD rises above $VDDI_{UV+}$. See "4.2. Power Sequence and Timing Behavior" on page 14 and "4.1. Truth Tables" on page 12 for more details.

4.4. Logic Input Signals

4.4.1. Control Inputs

VI, VI+, VI–, EN, and DIS inputs are CMOS level-compatible, active-high inputs. When VDDI is in undervoltage lockout (UVLO), the inputs of these pins are ignored and the gate driver's output is pulled low. For VI input devices, the output follows the corresponding VI input logic. For complementary input devices with a split output, VO+ is high and VO- is High-Z only when VI+ input is high and VI– input is low. For all other combinations of VI+ and VI–, VO+ is High-Z and VO– is low. For complementary input devices with a combined output and Miller clamp, VO is high when VI+ input is high and VI– input is low, and VO and MC are low when VO– input is high. Refer to "4.1. Truth Tables" on page 12 for detailed information on overlap protection behavior.

4.4.2. Enable and Disable Input

For devices with an enable (EN) input, when the EN input is driven low, it unconditionally drives VO– low and VO+ to High-Z regardless of the states of VI. Device operation terminates within t_{DID} after EN falls below V_{IL} and resumes within t_{EID} after EN rises above V_{IH}. For devices with a disable (DIS) input, when the DIS input is brought high, it unconditionally drives VO/VO–/MC low and VO+ High-Z regardless of the states of VI. Device operation terminates within t_{DID} after DIS rises above V_{IH} and resumes within t_{EID} after DIS falls below V_{IL}. See "4.2. Power Sequence and Timing Behavior" on page 14. The EN and DIS inputs have no effect if VDDI is below its UVLO level (i.e., VO/VO–/MC remain low and VO+ remains High-Z).

4.4.3. Deglitch Filter

A deglitch feature is provided on some devices. The deglitch feature ignores input noise with a duration shorter than the deglitch filter setting, but also introduces additional propagation delay. See "6.2.4. Timing Characteristics" on page 28 for the delays associated with this feature. The deglitch filter can be adjusted by selecting different product options. See "10. Ordering Guide" on page 46 for more details.

4.5. Active Miller Clamp

The Si82B41x/44x/47x devices provide a separate Miller clamp pin, MC. The Miller clamp pin is designed to directly attach to the power switch's gate/base to bypass any gate resistors. The Miller clamp engages during the transition from V_{OH} to V_{OL}. When the Miller clamp pin voltage, V_{MC}, falls below V_{MCT}, the output of the Miller clamp pulls strongly low. The Miller clamp will stay engaged until the next V_{OL} to V_{OH} transition. If any voltage transients occur on the MC pin during the Off period, the Miller clamp will strongly clamp these to GND.

4.6. Short-Circuit Clamp

The short circuit clamp is used to clamp voltages at the driver output (VO/VO+) to slightly higher than the VDD voltage during short circuit conditions. The short circuit clamp helps protect the driven switch gate from overvoltage breakdown or degradation. The clamp is implemented by adding a diode connection between VO/VO+ and the VDD pin inside the driver. See “6.2.3. Gate Driver Characteristics” on page 26 for detailed specifications of this clamping feature. External diodes between VO/VO+ and VDD can increase current conduction capability as needed.

4.7. Thermal Protection

The device includes a temperature sensor in the gate driver. The sensor is monitored continuously. If the temperature exceeds the Trigger Temperature (T_{SD+}), a thermal shutdown fault will occur, and the driver will pull low. After 1 ms, if the driver temperature fails to fall below the Reset Temperature ($T_{SD–}$), the driver will pull weakly low. The driver will continuously pull weakly low until the temperature falls below $T_{SD–}$. Once the fault is removed, normal operation resumes.

4.8. Shutdown Clamp

The device includes a voltage clamp between the gate driver output or Miller clamp pin (VO/VO– or MC) and ground (GND) when the gate driver is unpowered (VDD = High-Z). This clamp is sometimes referred to as an “active pull-down clamp”. It provides a path to ground for transient currents which could otherwise cause parasitic turn-on of a driven switch when the gate driver is unpowered. See “6.2.3. Gate Driver Characteristics” on page 26 and “4.1. Truth Tables” on page 12 for details.

4.9. ESD Structure

The Si82Bx device’s I/O pin electrostatic discharge (ESD) diodes and associated supply pin ESD clamp diodes are illustrated in the Figure 16, Figure 17, and Figure 18 Device ESD Structures below. On the logic input side, a pair of ESD protection diodes are used on each input pin, and all upper diodes are connected to one shared clamp diode. This structure prevents the VDDI pin from being powered up through the input pin when the VDDI power supply is lost. The other clamp diode is present between the VDDI pin and the GNDI pin. The ESD structure of the gate driver output is similar to the logic input, except that the gate driver output’s upper ESD diode is connected to a clamp diode at the VDD pin.

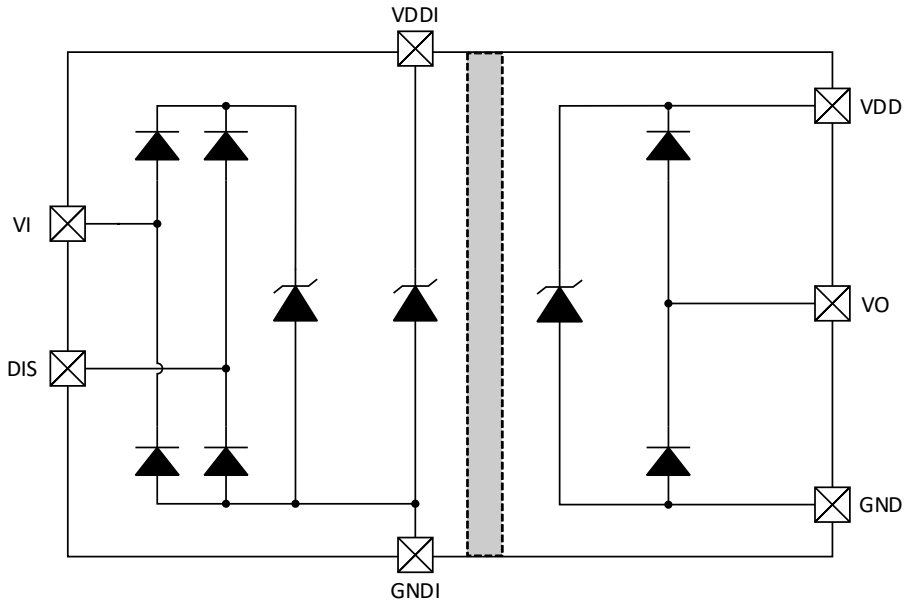


Figure 16. Si82B28x Device ESD Structure

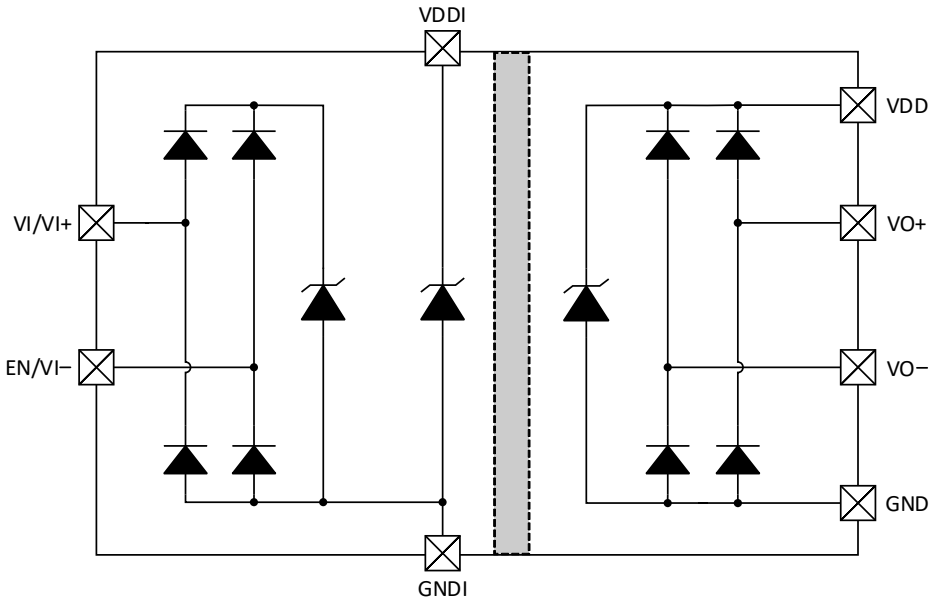


Figure 17. Si82B30x/40x/43x Device ESD Structure

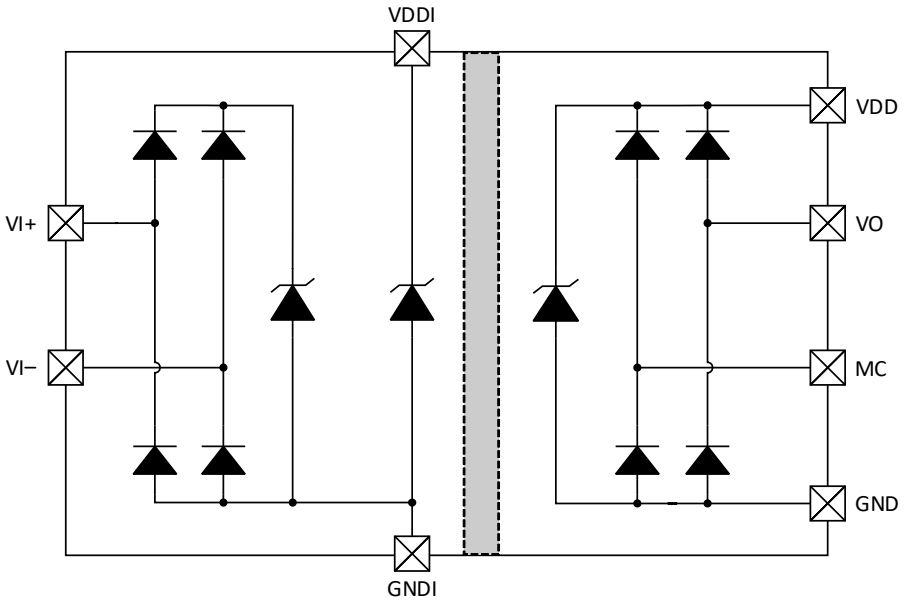


Figure 18. Si82B41x/44x/47x Device ESD Structure

5. Application Information

The Si82Bx is designed to be both flexible and robust to meet a wide range of application requirements, safely survive overloads, and rapidly recover normal operation. To achieve these objectives, the appropriate configuration must be selected and its circuit carefully designed.

5.1. Recommended Application Circuits

Figure 19 below and Figure 20 on page 20 illustrate Si82Bx typical application circuits. The controller provides the Si82Bx input signal and can also use the EN/DIS signal to turn off the driver immediately once a system fault is detected.

On the gate driver side, the Si82Bx device's output current is controlled by the external gate resistors R15 and R21. The peak sourcing current for gate drivers is shown in Equation 1, and the peak sinking current for the gate driver is shown in Equation 2.

$$\frac{VDD}{R15 + R_{ON+}}$$

Equation 1. Peak Sourcing Current for Gate Drivers

$$\frac{VDD}{R15 \parallel R21 + R_{ON-}}$$

Equation 2. Peak Sinking Current for Gate Driver

The gate resistor values should be selected to meet the gate voltage rise-time/fall-time requirement based on the actual capacitive loading of FET Q1. When the package supports the split output, the D1 diode can be eliminated. For devices with a dedicated MC (Miller clamp) pin, the MC pin should be connected to FET Q1's gate.

The high-voltage Y2-class capacitor (not shown in the diagrams) between the logic input reference (GNDI) and the gate driver reference (GND) is recommended if additional radiated emissions or electrostatic discharge (ESD) mitigation is desired. The typical value for Y2 capacitor is between 47 pF and 100 pF. See "AN1131: Design Guide for Reducing Radiated and Conducted Emissions in Isolated Systems Using Skyworks' Isolators" for additional techniques to mitigate radiated and conducted emissions. Note that the Si82Bx device provides excellent common-mode transient immunity (CMTI) without employing any additional components or techniques. However, if your application requires extremely high common-mode transient immunity (CMTI) performance, it is recommended to add a 10 nF capacitor between each of the logic input pins and the logic input ground (GNDI). This will help improve the CMTI performance.

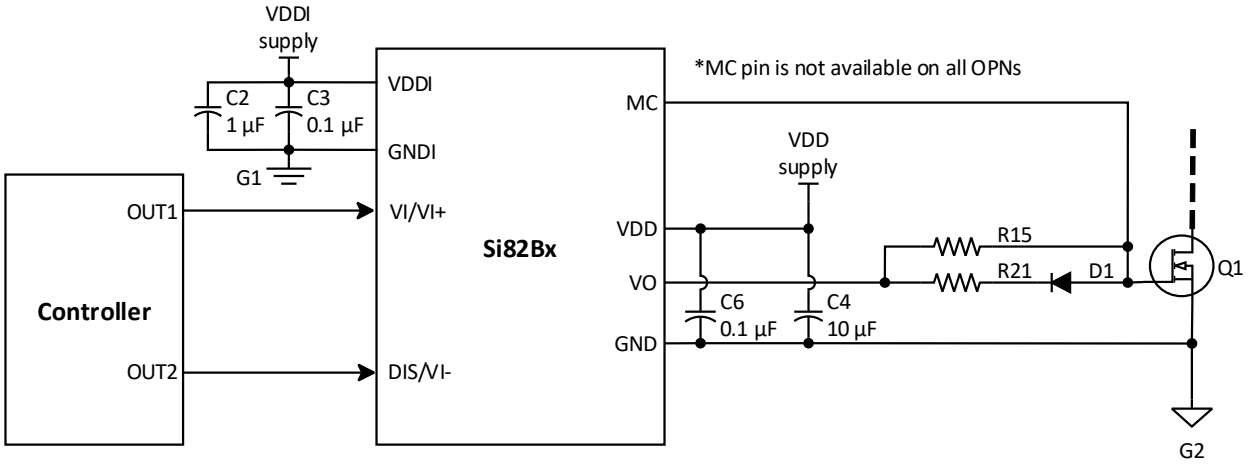


Figure 19. Si82Bx Single Supply Application

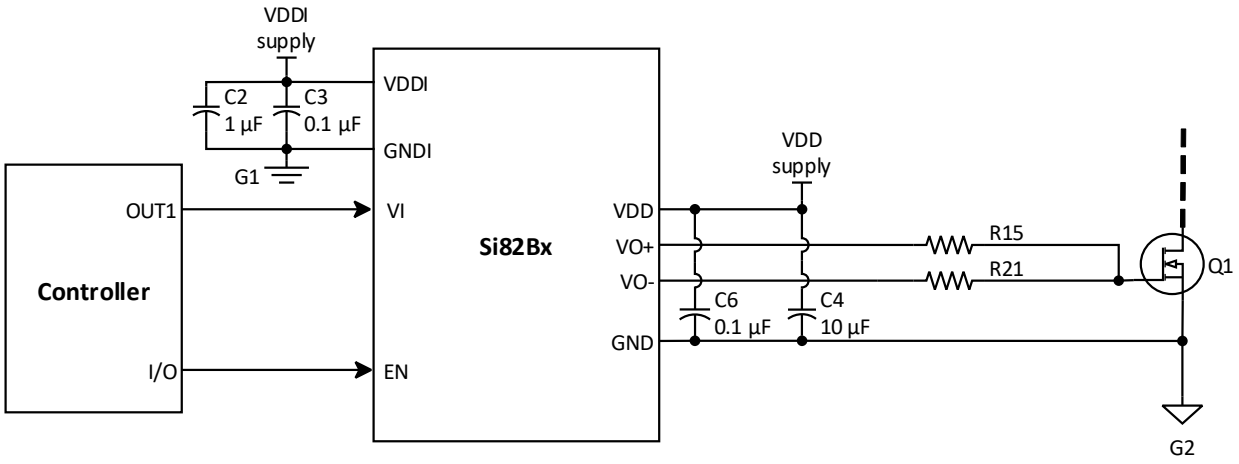


Figure 20. Si82Bx Split Output Application

The diagram shown in Figure 21, "Si82Bx Bipolar Output Connection," on page 20 is similar to the above circuits except that the drivers produce the bipolar V_{GS} output voltage. The bipolar V_{GS} output requires the system to provide positive and negative voltage sources. Note that the bootstrap circuit cannot be used to share the low-side voltage sources with the high-side gate driver for a bipolar V_{GS} output application. In this example, +15 V and –5 V sources are used. The voltage sources' reference G2 is electrically connected to FET Q1's source.

For the bipolar V_{GS} output application, the additional bypass capacitors form a capacitor divider in order to shorten the current flow loop. These capacitors should be placed close to the Si82Bx device's output power pins (VDD/GND). The ac component of the gate drive current flows from the VDDA net to the Si82Bx device's VDD pin, VO pin, external gate resistor, Q1's gate, Q1's source, the midpoint of capacitors C16 and C17, and back to VDDA. Since the original bypass capacitors C6 and C4 don't connect to reference G2 (which is connected to FET Q1's source), without capacitor C16, the return current needs to travel further to the system's +15 V source to complete the loop. This prolonged loop increases the chance of radiated emissions.

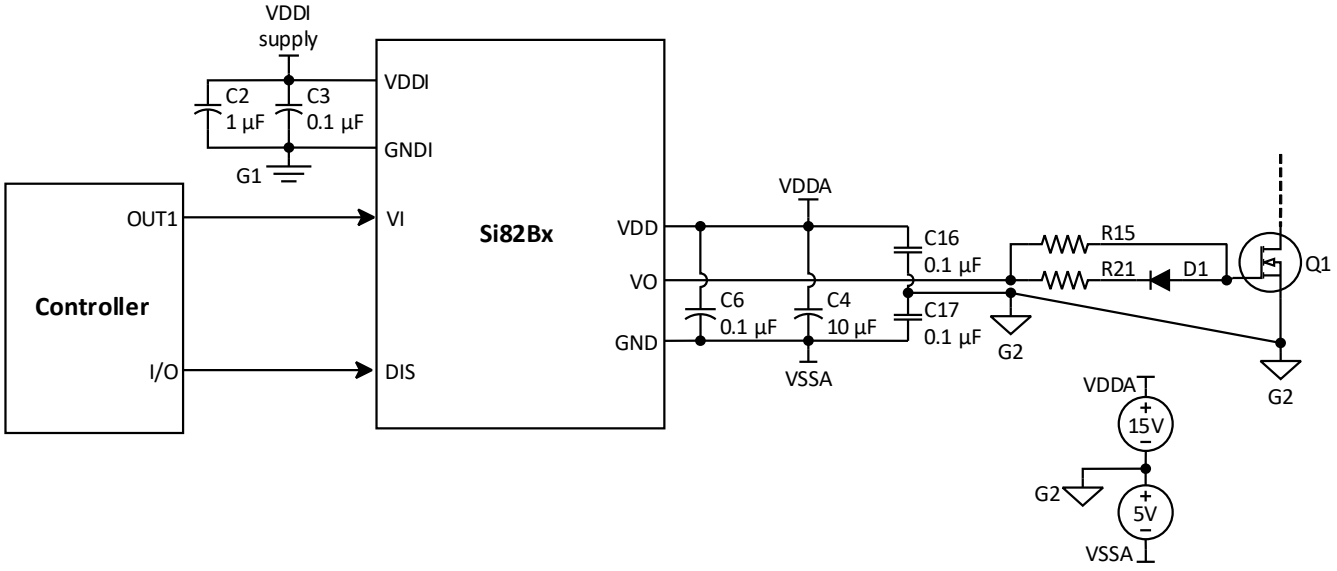


Figure 21. Si82Bx Bipolar Output Connection

5.2. Layout Considerations

The layout considerations are divided into general considerations for the entire device, the logic input side of the device, and the gate driver side. Refer to “5.1. Recommended Application Circuits” on page 19 for specific parts referenced.

5.2.1. General Considerations

- The bypass capacitors (usually 0.1 µF || 10 µF) should be placed close to the device's power supply pins and connected to the device with thick and short traces.
- The isolation barrier should have the required distance for the traces, power planes, ground planes, and copper areas on the device's logic input and gate drive sides.
- Safety isolation between two Si82Bx drivers is usually not required. If the system requires safety isolation between two drivers, the trace, power plane, ground plane, and the copper area between the two gate drivers should have the required distance. Even though safety isolation between two drivers is usually not required, to avoid arcing through the air, the traces operating at high voltage should have some distance (approximately 1 mm per 1 kV) from the low voltage signals.
- The Si82Bx device is often used in high-power systems with significant switching current and transient voltage. Attention should be paid to the proximity and orientation of the Si82Bx device and any high-current switching circuits. This should also apply to the traces and components surrounding the Si82Bx device to avoid unwanted noise coupling.

5.2.2. Logic Input Considerations

- If the application requires extremely high common-mode transient immunity (CMTI) performance, it is recommended to add a 10 nF capacitor between each of the logic input pins and the logic input ground (GNDI), including the no connect (NC) pins. This will help improve the CMTI performance.
- Using ≥6 mil trace width on all logic input pins is recommended. The interconnection between the controller and the Si82Bx device should be kept from any noisy signals in the system.

5.2.3. Gate Driver Considerations

- If the system is designed to provide a bipolar V_{GS} output, additional bypass capacitors (C16 and C17 in Figure 21, "Si82Bx Bipolar Output Connection," on page 20) are required to minimize the return path length of the gate drive signals.
- It is recommended to use ≥20 mil trace width for the VO gate driver trace and its return path.
- For a unipolar V_{GS} output, the return path of the V_{GS} gate drive signal is from the power device's source/emitter to the Si82Bx device's gate driver ground pin (GND). Explicitly use ≥20 mil trace width for this return current path and route this trace close to the VO gate driver trace to reduce the loop area of the whole V_{GS} gate drive signal. Moreover, it is a good practice to set the copper keep-out region along the return path trace so the system ground copper will not flood over this return trace.
- For a bipolar V_{GS} output, the return path of the V_{GS} gate drive signal is from the power device's source/emitter to the midpoint of capacitors C16 and C17. Therefore, these capacitors must be placed close to the Si82Bx device to minimize this current loop. Explicitly use ≥20 mil trace width for the return current path and route this return trace close to the VO gate driver trace to reduce the loop area of the whole V_{GS} gate drive signal. Moreover, it is a good practice to set the copper keep-out region along the return path trace so the system ground copper will not flood over this return trace.
- For a multiple-layer PCB design, ground and power planes are recommended to create a power supply current path with the least inductance. If there is no dedicated power or ground plane on the gate driver side, use ≥20 mil trace width for the power supply connections.
- If the design utilizes a Y2 capacitor between the logic input and the gate driver, the Y2 capacitor across the isolation barrier should be placed as close as possible to the sides of the Si82Bx device without pins.

5.3. Power Dissipation Considerations

The device's average power dissipation is often required in order to estimate the silicon junction temperature and can be estimated using the equation provided in "AN1339: Driver Power Dissipation Considerations". To solve the equation, the intended supply voltages, the load characteristics, the gate resistor values, and the switching frequency need to be collected. Skyworks provides a Microsoft Excel® based calculator as part of AN1339 to easily estimate the device's power dissipation and silicon junction temperature.

6. Specifications

6.1. Absolute Maximum Ratings

Table 6. Absolute Maximum Ratings[1]

Parameter	Symbol	Condition	Min	Max	Unit
Storage temperature	T_{STG}		–65	150	°C
Operating temperature	T_A		–40	125	°C
Junction temperature	T_J		—	150	°C
Logic input supply voltage	VDDI		–0.30	24.0	V
Gate driver supply voltage	VDD		–0.30	36.0	V
Input signal voltage	VI, VI+, VI–, EN, DIS		–0.30	VDDI + 0.30	V
	VI, VI+, VI–, EN, DIS	Transient for 100 ns[2]	–5.00	VDDI + 0.30	V
Output signal voltage	VO, VO+, VO–, MC		–0.30	VDD + V_{SCC}	V
		Transient for 200 ns[2]	–2.00	VDD + V_{SCC}	V
Lead solder temperature		Duration = 10 s	—	260	°C
ESD per AEC-Q100					
Human body model	HBM		–4	4	kV
Charged device model	CDM		–2	2	kV

1. Permanent device damage may occur if the absolute maximum ratings are exceeded. Functional operation should be restricted to the conditions as specified in the operational sections of this data sheet. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.
2. This parameter is not subject to production test. It is guaranteed by characterization.

ESD Handling: Industry-standard ESD handling precautions must be adhered to at all times to avoid damage to this device.

6.2. Electrical Characteristics

The following tables provide electrical parametric data for this device.

6.2.1. Power Supply Characteristics

Table 7. Power Supply Characteristics

Operating range for the following specifications: VDDI = 3.0–20 V; VDD = 5.0–30 V; T_A = –40 to +125 °C; F_{IN} ≤ 1 MHz.

Typical specifications: VDDI = 5 V; VDD = 6 V for 4 V UVLO devices, 10 V for 8 V UVLO devices, 15 V for 12 V UVLO devices, and 18 V for 15 V UVLO devices. T_A = 25 °C unless otherwise noted.

Parameter	Symbol	Test Condition	Min	Typ	Max	Unit
Supply Voltage						
Logic input supply	VDDI		3.00	—	20.0	V
Gate driver supply	VDD		5.00	—	30.0	V
Supply Current						
Logic Input Supply						
Quiescent current	$IDDI_Q$	EN/VI+ = logic low or DIS = logic high	—	0.81	1.27	mA
Active current	IDDI	VI or VI+/VI– = 1 MHz; 50% duty cycle	—	1.30	1.77	mA
Gate Driver Supply						
4 V Undervoltage Lockout (Si82BxxxGx) Devices						
Quiescent current	IDD_Q	EN/VI+ = logic low or DIS = logic high	—	2.40	3.50	mA
Active current	IDD	VO or VO+/VO– = 1 MHz; 50% duty cycle; no load	—	5.59	12.58	mA
8 V Undervoltage Lockout (Si82BxxxBx) Devices						
Quiescent current	IDD_Q	EN/VI+ = logic low or DIS = logic high	—	2.43	3.50	mA
Active current	IDD	VO or VO+/VO– = 1 MHz; 50% duty cycle; no load	—	6.72	12.58	mA
12 V Undervoltage Lockout (Si82BxxxCx) Devices						
Quiescent current	IDD_Q	EN/VI+ = logic low or DIS = logic high	—	2.46	3.50	mA
Active current	IDD	VO or VO+/VO– = 1 MHz; 50% duty cycle; no load	—	7.95	12.58	mA
15 V Undervoltage Lockout (Si82BxxxEx) Devices						
Quiescent current	IDD_Q	EN/VI+ = logic low or DIS = logic high	—	2.49	3.50	mA
Active current	IDD	VO or VO+/VO– = 1 MHz; 50% duty cycle; no load	—	8.67	12.58	mA

Table 7. Power Supply Characteristics (Continued)

Operating range for the following specifications: VDDI = 3.0–20 V; VDD = 5.0–30 V; T_A = –40 to +125 °C; F_{IN} ≤ 1 MHz.

Typical specifications: VDDI = 5 V; VDD = 6 V for 4 V UVLO devices, 10 V for 8 V UVLO devices, 15 V for 12 V UVLO devices, and 18 V for 15 V UVLO devices. T_A = 25 °C unless otherwise noted.

Parameter	Symbol	Test Condition	Min	Typ	Max	Unit
Undervoltage Lockout						
Logic Input Supply						
Positive-going threshold	$VDDI_{UV+}$	VDDI rising	2.74	2.88	2.99	V
Negative-going threshold	$VDDI_{UV–}$	VDDI falling	2.67	2.79	2.91	V
VDDI undervoltage hysteresis	$VDDI_{HYS}$		—	90.0	—	mV
Gate Driver Supply						
4 V Undervoltage Lockout (Si82BxxxGx) Devices						
Positive-going threshold	VDD_{UV+}	VDD rising	4.09	4.30	4.54	V
Negative-going threshold	$VDD_{UV–}$	VDD falling	3.89	4.10	4.33	V
Threshold hysteresis	VDD_{HYS}		—	200	—	mV
8 V Undervoltage Lockout (Si82BxxxBx) Devices						
Positive-going threshold	VDD_{UV+}	VDD rising	7.58	8.07	8.55	V
Negative-going threshold	$VDD_{UV–}$	VDD falling	7.14	7.57	8.05	V
Threshold hysteresis	VDD_{HYS}		—	500	—	mV
12 V Undervoltage Lockout (Si82BxxxCx) Devices						
Positive-going threshold	VDD_{UV+}	VDD rising	11.21	11.90	12.61	V
Negative-going threshold	$VDD_{UV–}$	VDD falling	10.29	10.90	11.52	V
Threshold hysteresis	VDD_{HYS}		—	1.00	—	V
15 V Undervoltage Lockout (Si82BxxxEx) Devices						
Positive-going threshold	VDD_{UV+}	VDD rising	14.19	15.15	16.13	V
Negative-going threshold	$VDD_{UV–}$	VDD falling	13.81	14.70	15.66	V
Threshold hysteresis	VDD_{HYS}		—	450	—	mV

6.2.2. Logic Input Characteristics

Table 8. Logic Input Characteristics

Operating range for the following specifications: VDDI = 3.0–20 V; VDD = 5.0–30 V; T_A = –40 to +125 °C; F_{IN} ≤ 1 MHz.

Typical specifications: VDDI = 5 V; VDD = 6 V for 4 V UVLO devices, 10 V for 8 V UVLO devices, 15 V for 12 V UVLO devices, 18 V for 15 V UVLO devices; T_A = 25 °C unless otherwise noted.

Parameter	Symbol	Test Condition	Min	Typ	Max	Unit
Input Threshold						
High input	V_{IH}	VI, VI+, VI–, EN, DIS rising	VDDI x 0.85	—	—	V
Low input	V_{IL}	VI, VI+, VI–, EN, DIS falling	—	—	VDDI x 0.22	V
Hysteresis	V_{HYS}	VI, VI+, VI–, EN, DIS	VDDI x 0.06	VDDI x 0.15	—	V
Input pull-down resistance	R_I	VI, VI+, VI–, EN, DIS	152	200	279	kΩ
Input leakage current	$\lvert I_{LKG} \rvert$	VI, VI+, VI–, EN, DIS	—	—	131	µA

6.2.3. Gate Driver Characteristics

Table 9. Gate Driver Characteristics[1]

Operating range for the following specifications: VDDI = 3.0–20 V; VDD = 5.0–30 V; T_A = –40 to +125 °C; F_{IN} ≤ 1 MHz

Typical specifications: VDDI = 5 V; VDD = 6 V for 4 V UVLO devices, 10 V for 8 V UVLO devices, 15 V for 12 V UVLO devices, and 18 V for 15 V UVLO devices. T_A = 25 °C unless otherwise noted.

Parameter	Symbol	Test Condition	Min	Typ	Max	Unit
Output Voltage						
Logic high (sourcing)	V_{OH}	I_O = –20 mA	VDD x 0.98	—	—	V
Logic Low (Sinking)						
Si82B28x, Si82B30x, Si82B40x, and Si82B43x devices	V_{OL}	I_O = 20 mA	—	—	0.10	V
Si82B41x, Si82B44x, and Si82B47x devices	V_{OL}	I_O = 20 mA	—	—	0.20	V
Output Resistance						
Logic high (sourcing)	R_{ON+}		0.50	1.00	2.50	Ω
Logic Low (Sinking)						
Si82B28x, Si82B30x, Si82B40x, and Si82B43x devices	$R_{ON–}$		0.30	0.70	2.20	Ω
Si82B41x, Si82B44x, and Si82B47x devices	$R_{ON–}$		0.60	1.40	4.40	Ω
Peak Output Current						
Logic high (sourcing)	I_{O+}	VDD = 6 V, VO/VO+ = 1.5 V	—	3.80	—	A
		VDD = 10 V, VO/VO+ = 3 V	—	5.40	—	A
		VDD = 15 V, VO/VO+ = 5 V	—	6.65	—	A
		VDD = 18 V, VO/VO+ = 6 V	5.50	7.50	—	A

Table 9. Gate Driver Characteristics[1] (Continued)

Operating range for the following specifications: VDDI = 3.0–20 V; VDD = 5.0–30 V; T_A = –40 to +125 °C; F_{IN} ≤ 1 MHz

Typical specifications: VDDI = 5 V; VDD = 6 V for 4 V UVLO devices, 10 V for 8 V UVLO devices, 15 V for 12 V UVLO devices, and 18 V for 15 V UVLO devices. T_A = 25 °C unless otherwise noted.

Parameter	Symbol	Test Condition	Min	Typ	Max	Unit
Logic Low (Sinking)						
Si82B28x, Si82B30x, Si82B40x, and Si82B43x devices	$I_{O–}$	VDD = 6 V, VO/VO– = 4.5 V	—	5.10	—	A
		VDD = 10 V, VO/VO– = 7 V	—	6.55	—	A
		VDD = 15 V, VO/VO– = 10 V	—	7.40	—	A
		VDD = 18 V, VO/VO– = 12 V	5.50	7.50	—	A
Si82B41x, Si82B44x, and Si82B47x devices	$I_{O–}$	VDD = 6 V, VO/VO– = 4.5 V	—	2.81	—	A
		VDD = 10 V, VO/VO– = 7 V	—	3.14	—	A
		VDD = 15 V, VO/VO– = 10 V	—	3.56	—	A
		VDD = 18 V, VO/VO– = 12 V	2.59	3.66	—	A
Miller Clamp (Si82B41x, Si82B44x, and Si82B47x) Devices						
Threshold voltage	V_{MCT}		1.75	2.00	2.35	V
Output Current						
4 V undervoltage lockout (Si82BxxxGx) devices	I_{OMC}	VDD = 6 V, VO = V_{MCT}	—	1.50	—	A
		VDD = 6 V, VO = 4.5 V	—	2.81	—	A
8 V undervoltage lockout (Si82BxxxBx) devices		VDD = 10 V, VO = V_{MCT}	—	1.80	—	A
		VDD = 10 V, VO = 7 V	—	3.14	—	A
12 V undervoltage lockout (Si82BxxxCx) devices		VDD = 15 V, VO = V_{MCT}	—	1.90	—	A
		VDD = 15 V, VO = 10 V	—	3.56	—	A
15 V undervoltage lockout (Si82BxxxEx) devices		VDD = 18 V, VO = V_{MCT}	—	2.10	—	A
		VDD = 18 V, VO = 12 V	2.59	3.66	—	A
Output resistance	R_{ONMC}		0.60	1.40	4.40	Ω
Switch Short Circuit Clamp						
Clamping Voltage						
Si82B28x, Si82B30x, Si82B40x, and Si82B43x devices	V_{SCC}	VO+ – VDD or GND – VO–, I_O = 70 mA	—	70.0	—	mV
		VO+ – VDD or GND – VO–, I_O = 500 mA, t_{SCC} = 10 µs	—	530	—	mV
Si82B41x, Si82B44x, and Si82B47x devices	V_{SCC}	VO+ – VDD, I_O = 70 mA	—	70.0	—	mV
		VO+ – VDD, I_O = 500 mA	—	530	—	mV
		GND – VO–/MC, I_O = 70 mA	—	75.0	—	mV
		GND – VO–/MC, I_O = 500 mA	—	550	—	mV
Thermal Shutdown						
Threshold temperature	T_{SD+}	T_J rising	—	163	—	°C
Release temperature	$T_{SD–}$	T_J falling	—	131	—	°C
Shutdown clamp output voltage	V_{SDC}	VDD = High-Z, $I_{O/MC}$ = 50 mA	—	1.55	2.00	V

1. Adding the suffix +/– to any symbol, parameter, or test condition variable denotes that the term applies interchangeably to the pull-up (sourcing) output VO+ or the pull-down (sinking) output VO–.

6.2.4. Timing Characteristics

Table 10. Timing Charcteristics

Operating range for the following specifications: VDDI = 3.0–20 V; VDD = 5.0–30 V; T_A = –40 to +125 °C; $F_{IN} \leq 1$ MHz.

Typical specifications: VDDI = 5 V; VDD = 6 V for 4 V UVLO devices, 10 V for 8 V UVLO devices, 15 V for 12 V UVLO devices, 18 V for 15 V UVLO devices; T_A = 25 °C unless otherwise noted.

Parameter	Symbol	Test Condition	Min	Typ	Max	Unit
Minimum Pulse Width						
Si82BxxAx devices	PW_{MIN}	No load	—	10.0	—	ns
Si82BxxBx devices			—	30.0	—	ns
Propagation Delay						
Positive-Going Control Input Delay[1]						
0 ns deglitch (Si82BxxAx) devices	t_{PLH}	VI, VI+ rising; no load	17.7	26.0	38.2	ns
30 ns deglitch (Si82BxxBx) devices			41.8	51.0	63.1	ns
Negative-Going Control Input Delay[1]						
0 ns deglitch (Si82BxxAx) devices	t_{PHL}	VI, VI+ falling; no load	17.7	26.0	38.2	ns
30 ns deglitch (Si82BxxBx) devices			41.8	51.0	63.1	ns
Enable input delay[2]	t_{EID}	EN rising or DIS falling, no load	16.2	26.0	39.3	ns
Disable input delay[2]	t_{DID}	EN falling or DIS rising, no load	16.2	26.0	39.3	ns
Pulse width distortion	PWD	$\lvert t_{PLH} - t_{PHL} \rvert$	—	5.00	10.0	ns
Part-to-Part Propagation Delay Skew[3]						
0 ns deglitch (Si82BxxAx) devices	$t_{PSK(PP)}$	MAX{ $\lvert t_{PLHx} - t_{PLHy} \rvert$, $\lvert t_{PHLx} - t_{PHLy} \rvert$ }	—	—	5.00	ns
30 ns deglitch (Si82BxxBx) devices			—	—	8.00	ns
Output rise time[1]	t_R	VDD = 6 V, C_L = 1 nF, R_G = 0 Ω	—	7.50	—	ns
		VDD = 10 V, C_L = 1 nF, R_G = 0 Ω	—	7.20	—	ns
		VDD = 15 V, C_L = 1 nF, R_G = 0 Ω	—	7.90	—	ns
		VDD = 18 V, C_L = 1 nF, R_G = 0 Ω	—	8.30	—	ns
Output Fall Time[1]						
Si82B28x, Si82B30x, Si82B40x, and Si82B43x devices	t_F	VDD = 6 V, C_L = 1 nF, R_G = 0 Ω	—	6.60	—	ns
		VDD = 10 V, C_L = 1 nF, R_G = 0 Ω	—	7.00	—	ns
		VDD = 15 V, C_L = 1 nF, R_G = 0 Ω	—	7.95	—	ns
		VDD = 18 V, C_L = 1 nF, R_G = 0 Ω	—	8.60	—	ns
Si82B41x, Si82B44x, and Si82B47x devices	t_F	VDD = 6 V, C_L = 1 nF, R_G = 0 Ω, MC = High-Z	—	5.80	—	ns
		VDD = 10 V, C_L = 1 nF, R_G = 0 Ω, MC = High-Z	—	6.15	—	ns
		VDD = 15 V, C_L = 1 nF, R_G = 0 Ω, MC = High-Z	—	7.00	—	ns
		VDD = 18 V, C_L = 1 nF, R_G = 0 Ω, MC = High-Z	—	7.50	—	ns

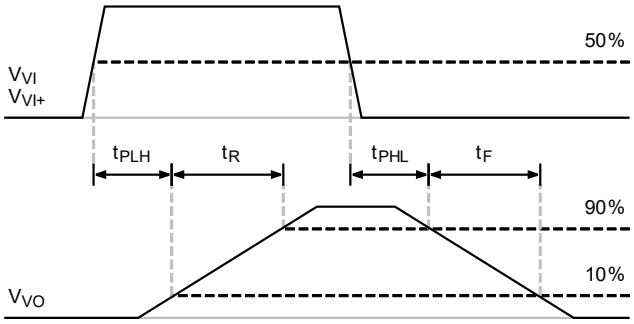
Table 10. Timing Charcteristics (Continued)

Operating range for the following specifications: VDDI = 3.0–20 V; VDD = 5.0–30 V; T_A = –40 to +125 °C; $F_{IN} \leq 1$ MHz.

Typical specifications: VDDI = 5 V; VDD = 6 V for 4 V UVLO devices, 10 V for 8 V UVLO devices, 15 V for 12 V UVLO devices, 18 V for 15 V UVLO devices; T_A = 25 °C unless otherwise noted.

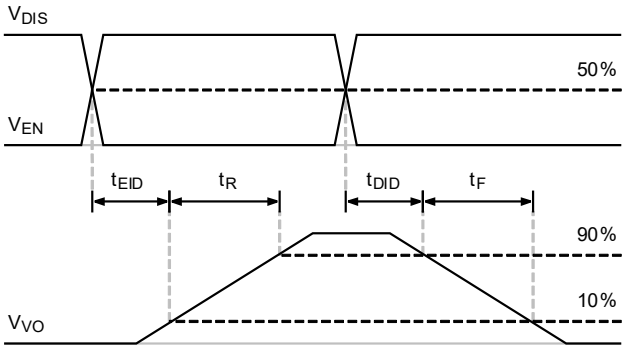
Parameter	Symbol	Test Condition	Min	Typ	Max	Unit
Startup time[4]	t_{ST}		—	50.0	—	µs
VDDI logic input power cycle time[4]	t_{PCL}		—	40.0	—	µs
VDDI logic input shutdown time[4]	t_{SDL}		—	300	—	ns
VDD gate driver power cycle time[4]	t_{PCG}		—	50.0	—	µs
VDD gate driver shutdown time[4]	t_{SDG}		—	240	—	ns
Common-mode transient immunity	CMTI		200	—	—	kV/µs

1. See Figure 22, "Control Input Timing Measurements," on page 29 for details.
2. See Figure 23, "Enable or Disable Input Timing Measurements," on page 29 for details.
3. $t_{PSK(PP)}$ is the largest absolute value difference in propagation delays measured between different channels on different units operating at the same supply voltages, load, and ambient temperature.
4. Startup, power cycle, and shutdown timing are detailed in "4.2. Power Sequence and Timing Behavior" on page 14.



VO = VO+ and VO- combined
EN = Logic high
DIS = Logic low
VI- = Logic low

Figure 22. Control Input Timing Measurements



VO = VO+ and VI- combined
VI, VI+ = Logic High, VI- = Logic Low

Figure 23. Enable or Disable Input Timing Measurements

6.3. Typical Performance Characteristics

The typical performance characteristics depicted in the figures below are for information purposes only. Refer to the data tables in "6.2. Electrical Characteristics" on page 24 for actual specification limits.

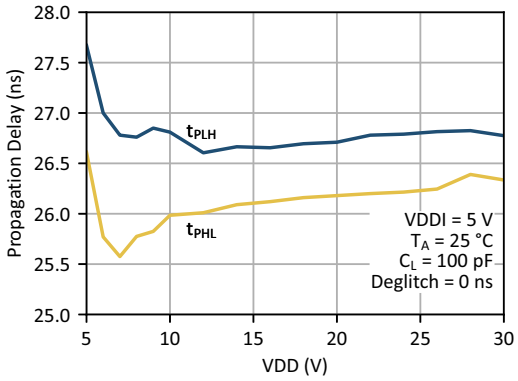


Figure 24. Propagation Delay vs. Gate Driver Supply Voltage

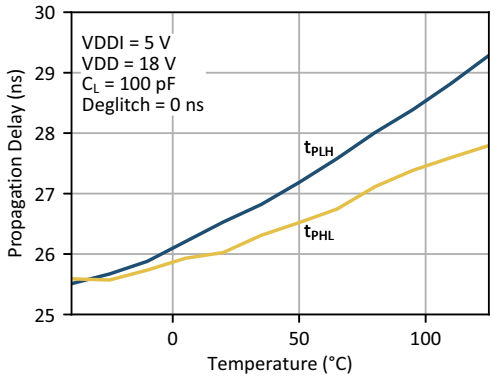


Figure 25. Propagation Delay vs. Ambient Temperature

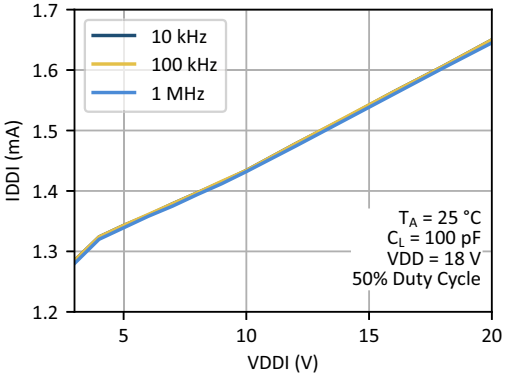


Figure 26. Logic Input Active Supply Current vs. Logic Input Supply Voltage

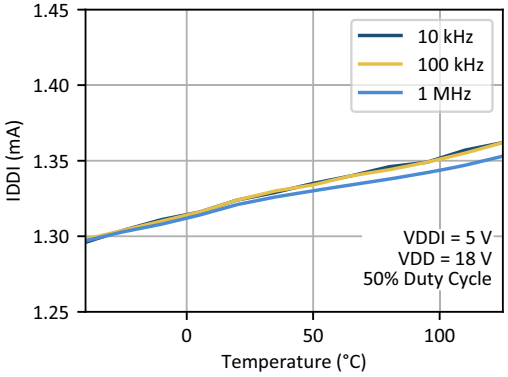


Figure 27. Logic Input Active Supply Current vs. Ambient Temperature

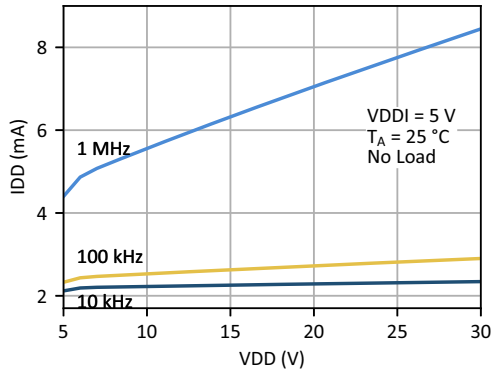


Figure 28. Gate Driver Active Supply Current vs. Gate Driver Supply Voltage

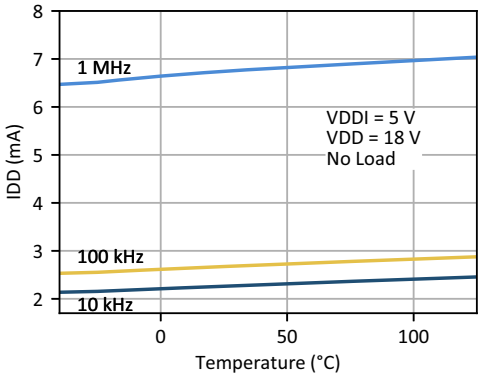


Figure 29. Gate Driver Active Supply Current vs. Ambient Temperature

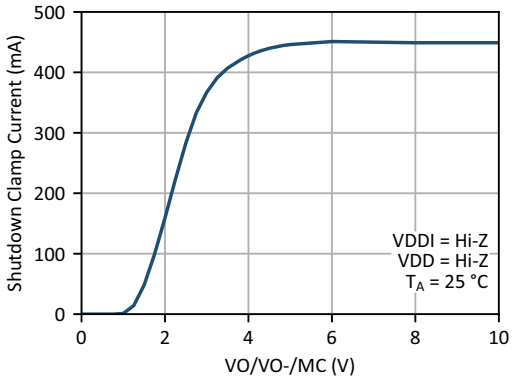


Figure 30. Shutdown Clamp Current vs. Shutdown Clamp Voltage

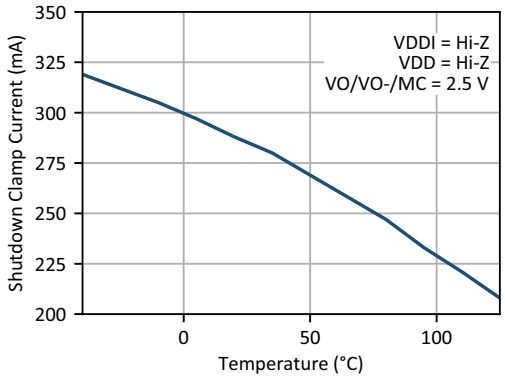


Figure 31. Shutdown Clamp Current vs. Ambient Temperature

6.3.1. Combined and Split Output (Si82B28x/30x/40x/43x) Devices

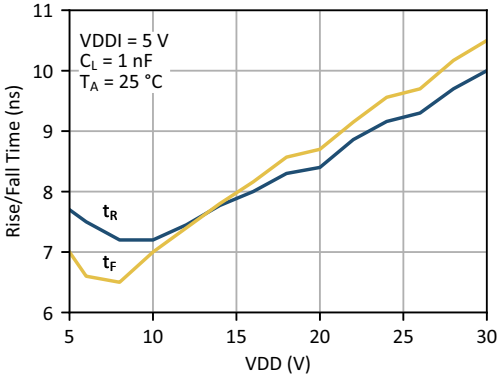


Figure 32. Output Rise/Fall Time vs. Gate Driver Supply Voltage

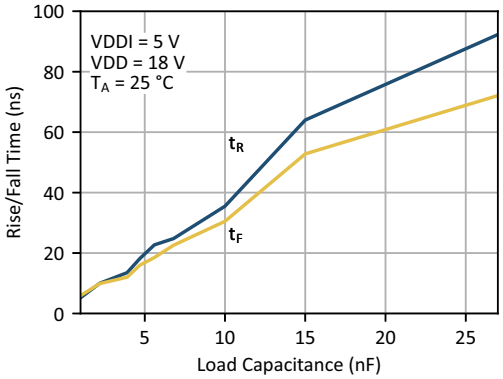


Figure 33. Output Rise/Fall Time vs. Output Load

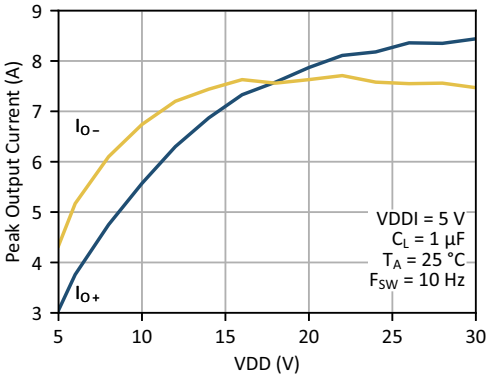


Figure 34. Peak Output Current vs. Gate Driver Supply Voltage

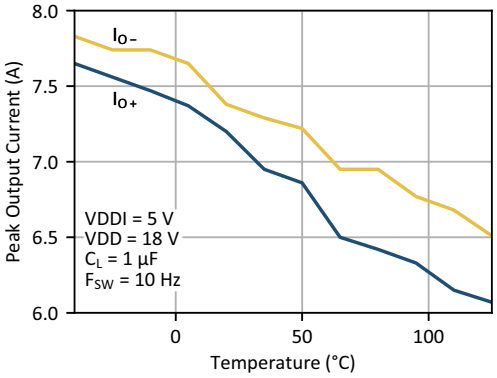


Figure 35. Output Current vs. Ambient Temperature

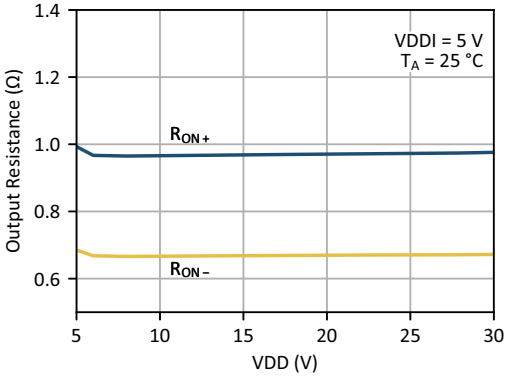


Figure 36. Output Resistance vs. Gate Driver Supply Voltage

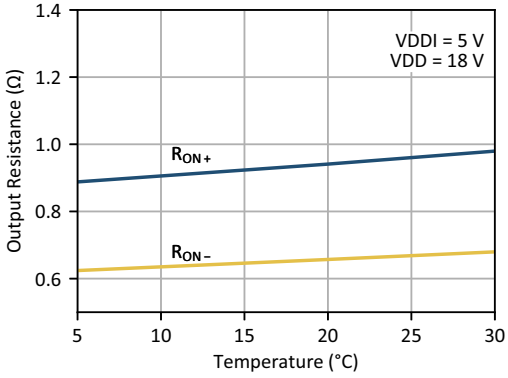


Figure 37. Output Resistance vs. Ambient Temperature

6.3.2. Miller Clamp (Si82B41x/44x/47x) Devices

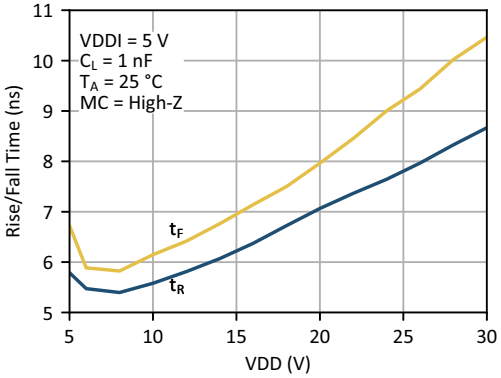


Figure 38. Output Rise/Fall Time vs. Gate Driver Supply Voltage

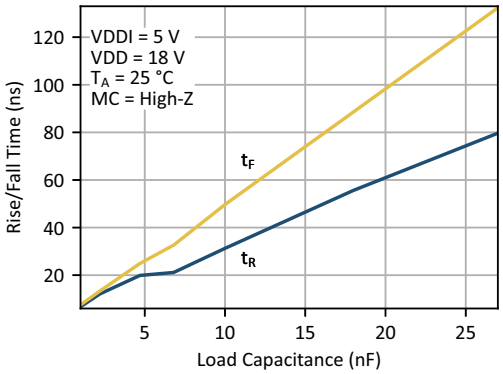


Figure 39. Output Rise/Fall Time vs. Output Load

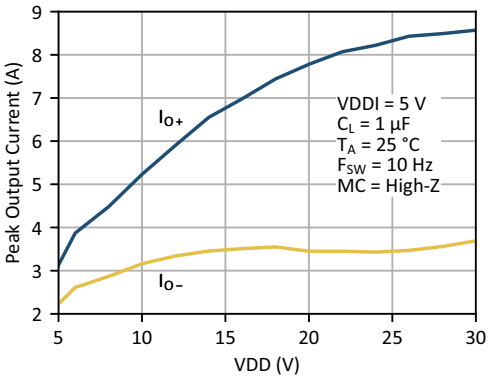


Figure 40. Output Current vs. Gate Driver Supply Voltage

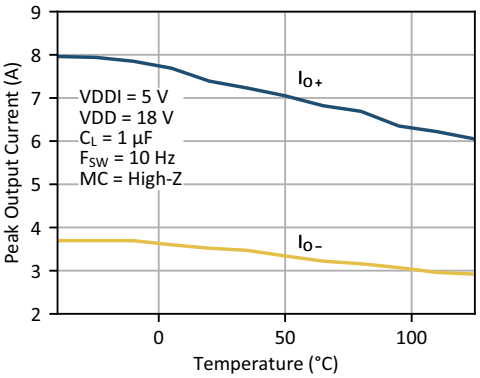


Figure 41. Output Current vs. Ambient Temperature

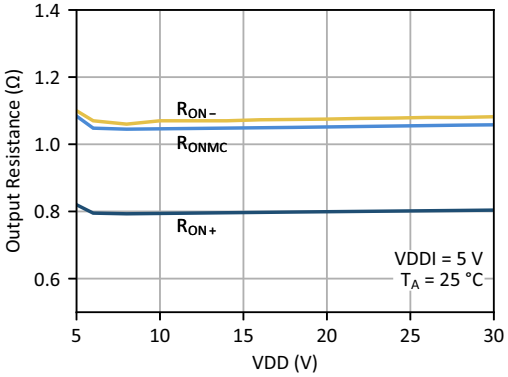


Figure 42. Output Resistance vs. Gate Driver Supply Voltage

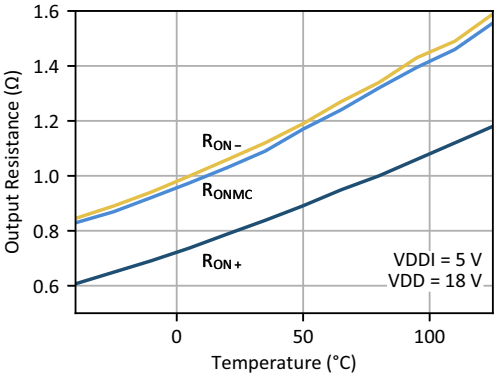


Figure 43. Output Resistance vs. Ambient Temperature

6.4. Thermal Characteristics

Table 11. Thermal Characteristics

Parameter	Symbol	Test Condition	NB SOIC-8	SSO-8	Unit
Thermal Resistance					
Junction-to-ambient	θ_{JA}	4-layer, 2s2p JEDEC test board	101	99	°C/W
Characterization Parameters					
Junction-to-top	Ψ_{JT}	4-layer, 2s2p JEDEC test board	9	15	°C/W
Junction-to-board	Ψ_{JB}	4-layer, 2s2p JEDEC test board	70	69	°C/W

6.5. Safety Certifications and Specifications

Table 12. Regulatory Information[1]

CSA
The Si82Bx is certified under CSA. For more details, see Master Contract Number 232873.
62368-1: Rated up to 600 V_{RMS} reinforced insulation working voltage; rated up to 1000 V_{RMS} basic insulation working voltage.
60601-1: Rated up to 250 V_{RMS} working voltage and two means of patient protection (MOPP).
VDE
The Si82Bx is certified under VDE. For more details, see File 5028467.
60747-17: Rated up to 2121 V_{PEAK} for reinforced insulation working voltage.
UL
The Si82Bx is certified under UL1577 component recognition program. For more details, see File E257455.
Rated up to 6.0 kV_{RMS} V_{ISO} isolation voltage for basic protection.
CQC
The Si82Bx is certified under GB4943.1.
Rated up to 250 V_{RMS} reinforced insulation working voltage at 5000 meters tropical climate.

1. For more information, see "10. Ordering Guide" on page 46.

Table 13. Insulation and Safety-Related Specifications

Parameter	Symbol	Test Condition	Value		Unit
			NB SOIC-8	SSO-8	
Nominal external air gap (clearance)	CLR		3.90	8.00	mm
Nominal external tracking (creepage)	CRP		3.90	8.00	mm
Minimum internal gap (internal clearance)	DTI		0.036	0.036	mm
Tracking resistance	CTI or PTI	IEC60112	600	600	V_{RMS}
Erosion depth	ED		0.031	0.040	mm
Resistance (input-output)[1]	R_{IO}	T_A = 25 °C, V_{IO} = 500 V	10^{12}	10^{12}	Ω
Capacitance (input-output)[1]	C_{IO}	f = 1 MHz	0.50	0.50	pF
Input capacitance[2]	C_I	f = 100 kHz	2.00	2.00	pF

1. To determine resistance and capacitance, the device is converted into a 2-terminal device. Pins on Side A are shorted together to form the first terminal, and pins on Side B are shorted together to form the second terminal. The parameters are then measured between these two terminals.
2. Measured from input pin to ground.

Table 14. IEC60664-1 Ratings

Parameter	Test Conditions	Specification	
		NB SOIC-8	SSO-8
Material group		I	I
Overvoltage category	Rated mains voltage ≤ 150 V_{RMS}	I-IV	I-IV
	Rated mains voltage ≤ 300 V_{RMS}	I-III	I-IV
	Rated mains voltage ≤ 600 V_{RMS}	I-II	I-IV
	Rated mains voltage ≤ 1000 V_{RMS}	I	I-III

Table 15. IEC60747-17 Insulation Characteristics[1]

Parameter	Symbol	Test Condition	Characteristic		Unit
			NB SOIC-8	SSO-8	
Maximum working isolation voltage	V_{IOWM}	According to Time-Dependent Dielectric Breakdown (TDDB) Test	445	1500	V_{RMS}
Maximum repetitive isolation voltage	V_{IORM}	According to Time-Dependent Dielectric Breakdown (TDDB) Test	630	2121	V_{PEAK}
Apparent charge	Q_{PD}	Method b: At routine test (100% production) and preconditioning (type test); V_{INI} = 1.2 x V_{IOTM}, t_{INI} = 1 s; $V_{PD(M)}$ = 1.875 x V_{IORM}, t_M = 1 s (method b1) or $V_{PD(M)}$ = V_{INI}, t_M = t_{INI} (method b2)	≤ 5	≤ 5	pC
Maximum transient isolation voltage	V_{IOTM}	V_{TEST} = V_{IOTM}, t = 60 s (qualification); V_{TEST} = 1.2 x V_{IOTM}, t = 1 s (100% production)	5302	8484	V_{PEAK}
Maximum surge isolation voltage	V_{IOSM}	Tested in oil with 1.3 x V_{IMP} or 10 kV minimum and 1.2 µs/50 µs profile (qualification)	10400	10400	V_{PEAK}
Maximum impulse voltage	V_{IMP}	Tested in air with 1.2 µs/50 µs profile (qualification)	5000	8000	V_{PEAK}
Isolation resistance	R_{IO_S}	T_A = T_S, V_{IO} = 500 V	$>10^9$	$>10^9$	Ω
Pollution degree			2	2	
Climatic category			40/125/21	40/125/21	

1. This coupler is suitable for “reinforced insulation” only within the safety limiting values. Compliance with the safety limiting values shall be ensured by means of suitable protective circuits.

Table 16. IEC60747-17 Safety Limiting Values

Parameter	Symbol	Test Condition	Max[1]		Unit
			NB SOIC-8	SSO-8	
Safety temperature	T_S		150	150	°C
Safety input, output, or supply current	I_S	Refer to θ_{JA} in “6.4. Thermal Characteristics” on page 34; VDDI = 5 V, VDD = 30 V, T_J = 150 °C, T_A = 25 °C.	41.3	42.1	mA
Safety input, output, or total power	P_S	Refer to θ_{JA} in “6.4. Thermal Characteristics” on page 34; T_J = 150 °C, T_A = 25 °C.	1.24	1.26	W

1. Maximum value allowed in the event of a failure; also see the temperature derating curves below.

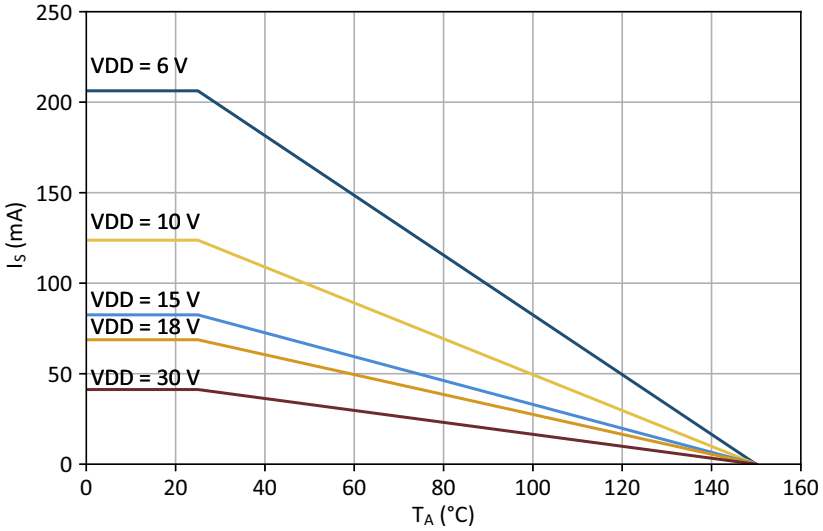


Figure 44. NB SOIC-8 Safety Current vs. Ambient Temperature Derating Curve

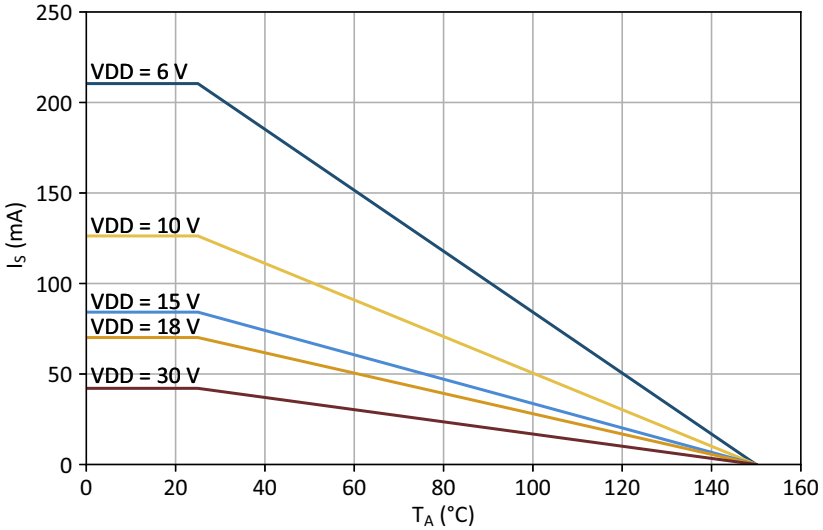


Figure 45. SSO-8 Safety Current vs. Ambient Temperature Derating Curve

Table 17. UL1577 Insulation Characteristics

Parameter	Symbol	Test Condition	Characteristic		Unit
			NB SOIC-8	SSO-8	
Maximum withstanding isolation voltage	V_{ISO}	$V_{TEST} = V_{ISO}$, t = 60 s (qualification); $V_{TEST} = 1.2 \times V_{ISO}$, t = 1 s (100% production)	3750	6000	V_{RMS}

7. Package Drawings

7.1. NB SOIC-8 Package Drawing

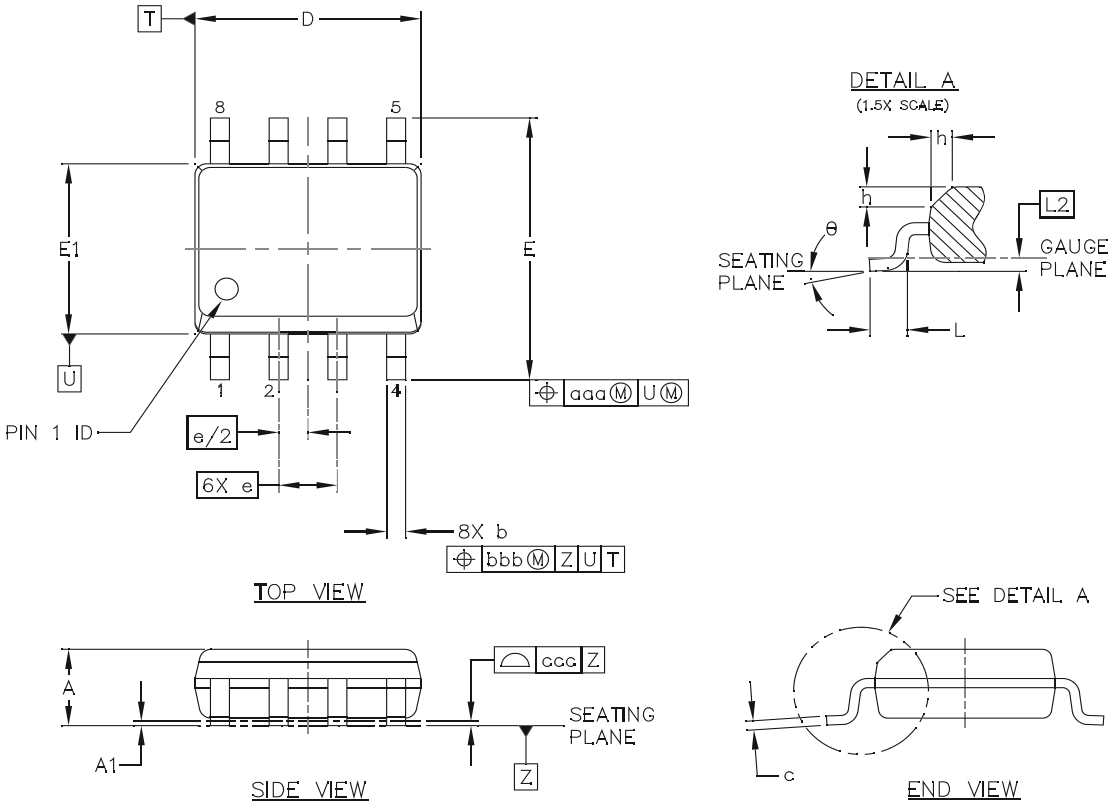


Figure 46. NB SOIC-8 Package Drawing

Table 18. NB SOIC-8 Package Drawing Dimensions[1,2,3,4,5]

Dimension	Min	Max
A	—	1.75
A1	0.10	0.25
b	0.33	0.51
c	0.19	0.25
D	4.80	5.00
E	5.80	6.20
E1	3.80	4.00
e	1.27 BSC	
L	0.40	1.27
L2	0.25 BSC	
h	0.25	0.50
θ	0°	8°

Table 18. NB SOIC-8 Package Drawing Dimensions[1,2,3,4,5] (Continued)

Dimension	Min	Max
aaa	0.10	
bbb	0.20	
ccc	0.10	

1. All dimensions shown are in millimeters (mm) unless otherwise noted.
2. Dimensioning and Tolerancing per ANSI Y14.5M.
   a. BSC: Basic Dimension. Theoretically exact shown without tolerance.
   b. REF: Reference Dimension: Usually without tolerance, for information purposes only.
3. Dimension D does not include mold flash, protrusions or gate burrs, which shall not exceed 0.15 mm per end. Dimension E1 does not include interlead flash or protrusion, which shall not exceed 0.25 mm per side.
4. This drawing conforms to the JEDEC Solid State Outline MS-137, Variation AB.
5. Recommended reflow profile per JEDEC J_STD_020 specification for small body, lead-free components.

7.2. SSO-8 Package Drawing

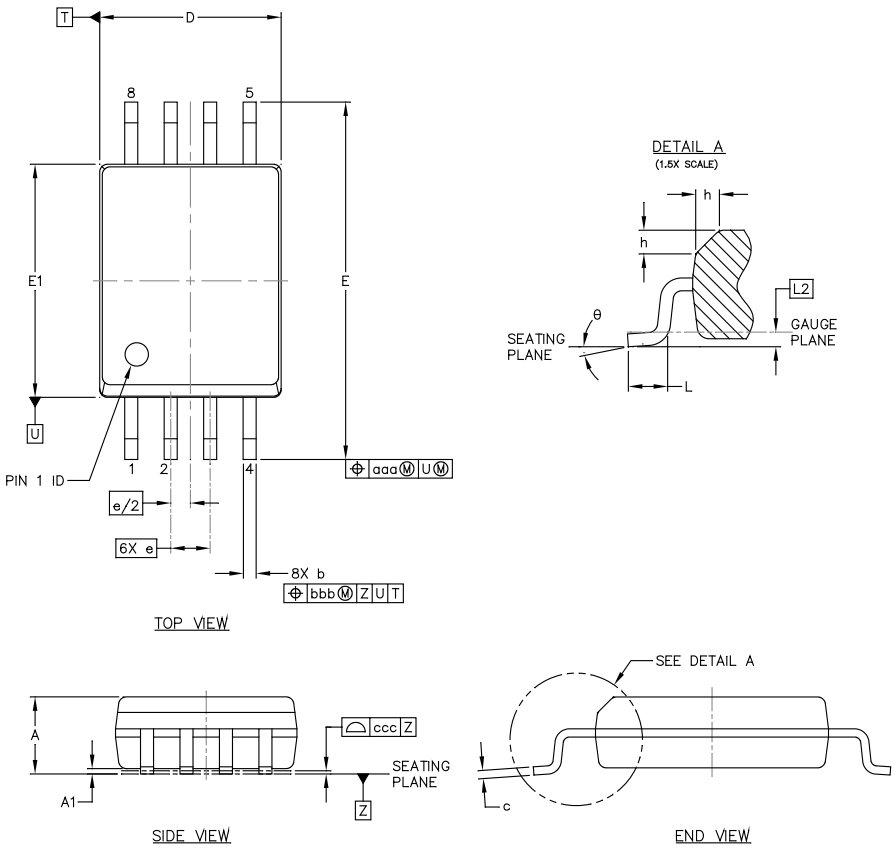


Figure 47. SSO-8 Package Drawing

Table 19. SSO-8 Package Drawing Dimensions[1,2,3,4]

Dimension	Min	Max
A	2.49	2.79
A1	0.36	0.46
b	0.30	0.51
c	0.13	0.33
D	5.74	5.94
E	11.25	11.76
E1	7.39	7.59
e	1.27 BSC	
L	0.51	1.02
L2	0.25 BSC	
h	0.25	0.76
θ	0°	8°

Table 19. SSO-8 Package Drawing Dimensions[1,2,3,4] (Continued)

Dimension	Min	Max
aaa	0.25	
bbb	0.25	
ccc	0.10	

1. All dimensions shown are in millimeters (mm) unless otherwise noted.
2. Dimensioning and Tolerancing per ANSI Y14.5M.
   a. BSC: Basic Dimension. Theoretically exact shown without tolerance.
   b. REF: Reference Dimension: Usually without tolerance, for information purposes only.
3. Dimension D does not include mold flash, protrusions or gate burrs, which shall not exceed 0.15 mm per end. Dimension E1 does not include interlead flash or protrusion, which shall not exceed 0.25 mm per side.
4. Recommended reflow profile per JEDEC J_STD_020 specification for small body, lead-free components.

8. Land Patterns

8.1. NB SOIC-8 Land Pattern

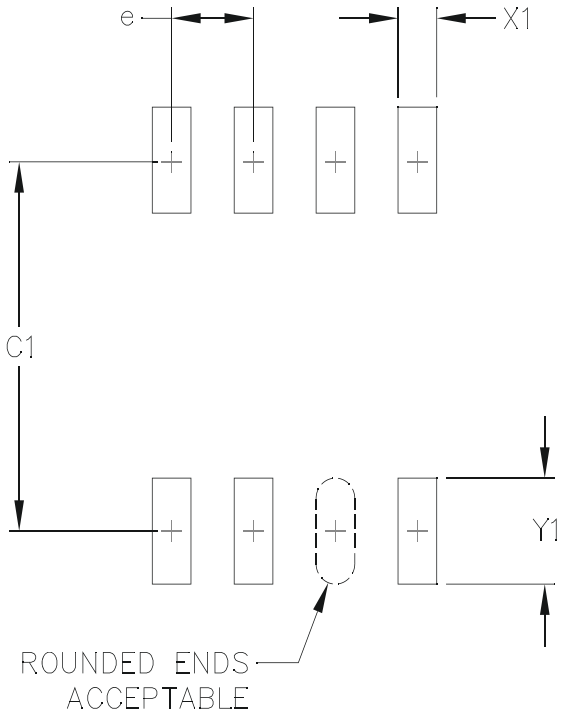


Figure 48. NB SOIC-8 Land Pattern

Table 20. NB SOIC-8 PCB Land Pattern Dimensions[1,2,3]

Dimension	Feature	mm
C1	Pad Column Spacing	5.40
e	Pad Row Pitch	1.27
X1	Pad Width	0.60
Y1	Pad Length	1.55

1. All dimensions shown are in millimeters (mm) unless otherwise noted.
2. This Land Pattern Design is based on IPC-7351 pattern SOIC127P600X173-8AN for Density Level B (Median Land Protrusion).
3. All feature sizes shown are at Maximum Material Condition (MMC), and a card fabrication tolerance of 0.05 mm is assumed.

8.2. SSO-8 Land Pattern

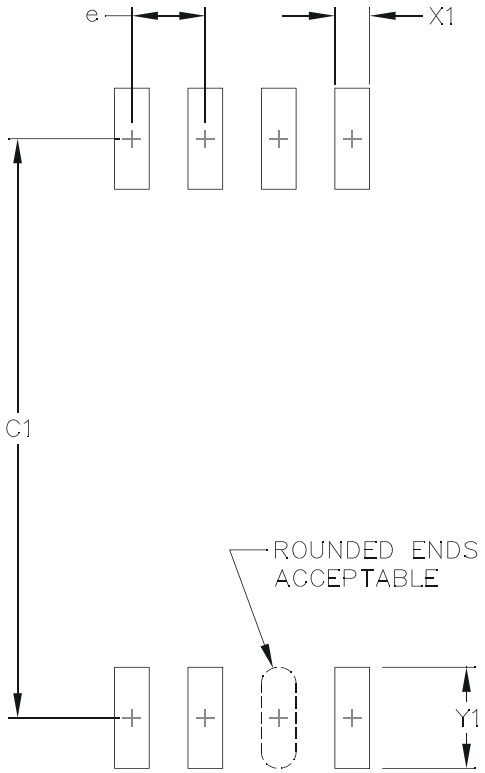


Figure 49. SSO-8 PCB Land Pattern

Table 21. SSO-8 PCB Land Pattern Dimensions[1,2,3]

Dimension	Feature	mm
C1	Pad Column Spacing	10.60
e	Pad Row Pitch	1.27
X1	Pad Width	0.60
Y1	Pad Length	1.85

1. All dimensions shown are in millimeters (mm) unless otherwise noted.
2. This Land Pattern Design is based on IPC-7351 guidelines.
3. All feature sizes shown are at Maximum Material Condition (MMC) and a card fabrication tolerance of 0.05 mm is assumed.

9. Top Markings

9.1. NB SOIC-8 Top Marking

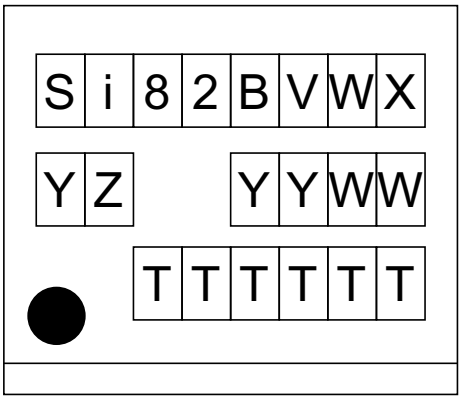


Figure 50. 8-Pin Narrow-Body SOIC Top Marking

Table 22. 8-Pin Narrow-Body SOIC Top Marking Explanation

Line 1 Marking:	Base Part Number Ordering Options (See "10. Ordering Guide" on page 46 for more information)	Si82B = One-channel Value IsoDriver product series V = Input Pinout 2 = VI and DIS inputs 3 = VI and EN inputs 4 = VI+ and VI– inputs W = Output Pinout 0 = Split Source/Sink Driver outputs 1 = Combined Source/Sink Driver and Miller Clamp outputs 8 = Combined Source/Sink Driver output X = Input Configuration A = No deglitch filter B = 30 ns deglitch filter
Line 2 Marking:	Base Part Number Ordering Options (See "10. Ordering Guide" on page 46 for more information)	Y = Output Configuration G = 4 V UVLO B = 8 V UVLO C = 12 V UVLO E = 15 V UVLO Z = Isolation Rating C = 3.75 kV_{RMS}
	YY = Year WW = Workweek	Assigned by the assembly house. Corresponds to the year and workweek of the mold date.
Line 3 Marking:	TTTTTT = Mfg. Trace Code	Manufacturing Traceability Code The Manufacturing Traceability Code represented by "TTTTTT" contains, as its first character, a letter in the range A through M to indicate Industrial-Grade, or a letter in the range N through Z to indicate Automotive-Grade.

9.2. SSO-8 Top Marking

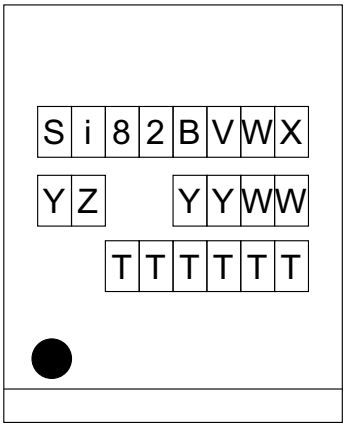


Figure 51. 8-Pin Stretched Small Outline (SSO) Top Marking

Table 23. 8-Pin Stretched Small Outline (SSO) Top Marking Explanation

Line 1 Marking:	Base Part Number Ordering Options (See "10. Ordering Guide" on page 46 for more information)	Si82B = One-channel Value ISOdriver product series V = Input Pinout 3 = VI and EN inputs 4 = VI+ and VI– inputs W = Output Pinout 0 = Split Source/Sink Driver outputs 1 = Combined Source/Sink Driver and Miller Clamp outputs 3 = Split Source/Sink Driver outputs 4 = Combined Source/Sink Driver and Miller Clamp outputs 7 = Combined Source/Sink Driver and Miller Clamp outputs X = Input Configuration A = No deglitch filter B = 30 ns deglitch filter
Line 2 Marking:	Base Part Number Ordering Options (See "10. Ordering Guide" on page 46 for more information)	Y = Output Configuration G = 4 V UVLO B = 8 V UVLO C = 12 V UVLO E = 15 V UVLO Z = Isolation Rating E = 6.0 kV_{RMS}
	YY = Year WW = Workweek	Assigned by the assembly house. Corresponds to the year and workweek of the mold date.
Line 3 Marking:	TTTTTT = Mfg. Trace Code	Manufacturing Traceability Code The Manufacturing Traceability Code represented by "TTTTTT" contains, as its first character, a letter in the range A through M to indicate Industrial-Grade, or a letter in the range N through Z to indicate Automotive-Grade.

10. Ordering Guide

Table 24. Si82Bxx Ordering Guide[1,2,3,4,5,6,7]

Ordering Part Number (OPN)	Automotive OPN	Inputs	Outputs	Enable/ Disable	Deglitch Filter	Undervoltage Lockout (UVLO)	Isolation Rating	Package Type
NB SOIC-8 Package Options								
Si82B28AGC-IS	Si82B28AGC-AS	VI	VO	Disable	NA	4 V	3.75 kV_{RMS}	NB SOIC-8
Si82B28ABC-IS	Si82B28ABC-AS	VI	VO	Disable	NA	8 V	3.75 kV_{RMS}	NB SOIC-8
Si82B28ACC-IS	Si82B28ACC-AS	VI	VO	Disable	NA	12 V	3.75 kV_{RMS}	NB SOIC-8
Si82B30AGC-IS	Si82B30AGC-AS	VI	VO+, VO–	Enable	NA	4 V	3.75 kV_{RMS}	NB SOIC-8
Si82B30ABC-IS	Si82B30ABC-AS	VI	VO+, VO–	Enable	NA	8 V	3.75 kV_{RMS}	NB SOIC-8
Si82B30ACC-IS	Si82B30ACC-AS	VI	VO+, VO–	Enable	NA	12 V	3.75 kV_{RMS}	NB SOIC-8
Si82B30AEC-IS	Si82B30AEC-AS	VI	VO+, VO–	Enable	NA	15 V	3.75 kV_{RMS}	NB SOIC-8
Si82B30BGC-IS	Si82B30BGC-AS	VI	VO+, VO–	Enable	30 ns	4 V	3.75 kV_{RMS}	NB SOIC-8
Si82B30BBC-IS	Si82B30BBC-AS	VI	VO+, VO–	Enable	30 ns	8 V	3.75 kV_{RMS}	NB SOIC-8
Si82B30BCC-IS	Si82B30BCC-AS	VI	VO+, VO–	Enable	30 ns	12 V	3.75 kV_{RMS}	NB SOIC-8
Si82B30BEC-IS	Si82B30BEC-AS	VI	VO+, VO–	Enable	30 ns	15 V	3.75 kV_{RMS}	NB SOIC-8
Si82B40AGC-IS	Si82B40AGC-AS	VI+, VI–	VO+, VO–	NA	NA	4 V	3.75 kV_{RMS}	NB SOIC-8
Si82B40ABC-IS	Si82B40ABC-AS	VI+, VI–	VO+, VO–	NA	NA	8 V	3.75 kV_{RMS}	NB SOIC-8
Si82B40ACC-IS	Si82B40ACC-AS	VI+, VI–	VO+, VO–	NA	NA	12 V	3.75 kV_{RMS}	NB SOIC-8
Si82B40AEC-IS	Si82B40AEC-AS	VI+, VI–	VO+, VO–	NA	NA	15 V	3.75 kV_{RMS}	NB SOIC-8
Si82B40BGC-IS	Si82B40BGC-AS	VI+, VI–	VO+, VO–	NA	30 ns	4 V	3.75 kV_{RMS}	NB SOIC-8
Si82B40BBC-IS	Si82B40BBC-AS	VI+, VI–	VO+, VO–	NA	30 ns	8 V	3.75 kV_{RMS}	NB SOIC-8
Si82B40BCC-IS	Si82B40BCC-AS	VI+, VI–	VO+, VO–	NA	30 ns	12 V	3.75 kV_{RMS}	NB SOIC-8
Si82B40BEC-IS	Si82B40BEC-AS	VI+, VI–	VO+, VO–	NA	30 ns	15 V	3.75 kV_{RMS}	NB SOIC-8
Si82B41ACC-IS	Si82B41ACC-AS	VI+, VI–	VO, MC	NA	NA	12 V	3.75 kV_{RMS}	NB SOIC-8
Si82B41BCC-IS	Si82B41BCC-AS	VI+, VI–	VO, MC	NA	30 ns	12 V	3.75 kV_{RMS}	NB SOIC-8

Table 24. Si82Bxx Ordering Guide[1,2,3,4,5,6,7] (Continued)

Ordering Part Number (OPN)	Automotive OPN	Inputs	Outputs	Enable/ Disable	Deglitch Filter	Undervoltage Lockout (UVLO)	Isolation Rating	Package Type
SSO-8 Package Options								
Si82B30ABE-IS4	Si82B30ABE-AS4	VI	VO+, VO–	Enable	NA	8 V	6 kV_{RMS}	SSO-8
Si82B30ACE-IS4	Si82B30ACE-AS4	VI	VO+, VO–	Enable	NA	12 V	6 kV_{RMS}	SSO-8
Si82B30AEE-IS4	Si82B30AEE-AS4	VI	VO+, VO–	Enable	NA	15 V	6 kV_{RMS}	SSO-8
Si82B30BBE-IS4	Si82B30BBE-AS4	VI	VO+, VO–	Enable	30 ns	8 V	6 kV_{RMS}	SSO-8
Si82B30BCE-IS4	Si82B30BCE-AS4	VI	VO+, VO–	Enable	30 ns	12 V	6 kV_{RMS}	SSO-8
Si82B30BEE-IS4	Si82B30BEE-AS4	VI	VO+, VO–	Enable	30 ns	15 V	6 kV_{RMS}	SSO-8
Si82B40ABE-IS4	Si82B40ABE-AS4	VI+, VI–	VO+, VO–	NA	NA	8 V	6 kV_{RMS}	SSO-8
Si82B40ACE-IS4	Si82B40ACE-AS4	VI+, VI–	VO+, VO–	NA	NA	12 V	6 kV_{RMS}	SSO-8
Si82B40AEE-IS4	Si82B40AEE-AS4	VI+, VI–	VO+, VO–	NA	NA	15 V	6 kV_{RMS}	SSO-8
Si82B40BBE-IS4	Si82B40BBE-AS4	VI+, VI–	VO+, VO–	NA	30 ns	8 V	6 kV_{RMS}	SSO-8
Si82B40BCE-IS4	Si82B40BCE-AS4	VI+, VI–	VO+, VO–	NA	30 ns	12 V	6 kV_{RMS}	SSO-8
Si82B40BEE-IS4	Si82B40BEE-AS4	VI+, VI–	VO+, VO–	NA	30 ns	15 V	6 kV_{RMS}	SSO-8
Si82B41ACE-IS4	Si82B41ACE-AS4	VI+, VI–	VO, MC	NA	NA	12 V	6 kV_{RMS}	SSO-8
Si82B41AEE-IS4	Si82B41AEE-AS4	VI+, VI–	VO, MC	NA	NA	15 V	6 kV_{RMS}	SSO-8
Si82B41BCE-IS4	Si82B41BCE-AS4	VI+, VI–	VO, MC	NA	30 ns	12 V	6 kV_{RMS}	SSO-8
Si82B43ACE-IS4	Si82B43ACE-AS4	VI+, VI–	VO+, VO–	NA	NA	12 V	6 kV_{RMS}	SSO-8
Si82B44ACE-IS4	Si82B44ACE-AS4	VI+, VI–	VO, MC	NA	NA	12 V	6 kV_{RMS}	SSO-8
Si82B47AGE-IS4	Si82B47AGE-AS4	VI+, VI–	VO, MC	NA	NA	4 V	6 kV_{RMS}	SSO-8
Si82B47ABE-IS4	Si82B47ABE-AS4	VI+, VI–	VO, MC	NA	NA	8 V	6 kV_{RMS}	SSO-8
Si82B47ACE-IS4	Si82B47ACE-AS4	VI+, VI–	VO, MC	NA	NA	12 V	6 kV_{RMS}	SSO-8

1. “Si” and “SI” are used interchangeably.
2. An “R” at the end of the Ordering Part Number indicates tape and reel packaging option.
3. All packages are RoHS-compliant with peak reflow temperatures of 260 °C according to the JEDEC industry standard classifications and peak solder temperatures.
4. All devices with VI+ and VI– inputs operate as complementary digital inputs.
5. All devices with VO+ and VO– outputs source current out of the VO+ pin and sink current into the VO– pin.
6. Automotive-Grade devices (with an “-A” suffix) are identical in construction materials and electrical parameters to their Industrial Grade (with an “-I” suffix) version counterparts. Automotive-Grade products are produced utilizing full automotive process flows and additional statistical process controls throughout the manufacturing flow. The Automotive-Grade part number is included on shipping labels.
7. In Top Markings, the Manufacturing Code represented by either “RTTTTT” or “TTTTTT” contains as its first character a letter in the range N through Z to indicate Automotive-Grade.

11. Revision History

Revision	Date	Description
A	January, 2025	Initial release.