DATA SHEET

SKY63101/SKY63102/SKY63103 16-Output, Jitter Attenuators/ Clock Multipliers with Integrated Reference

The SKY63101/02/03 Jitter Attenuators combine sixth-generation DSPLL® and MultiSynth™ technologies with an integrated Skyworks Bulk Acoustic Wave (BAW) oscillator to deliver ultra-low jitter (<45 fs) for high-performance applications like 112G and 224G SerDes and Coherent Optics. They are used in applications that demand the highest level of integration and jitter performance. All PLL components are integrated on-chip, eliminating the risk of noise coupling associated with discrete solutions.
The SKY63101 has a single DSPLL with two MultiSynths; the SKY63102 has two DSPLLs with one MultiSynth, and the SKY63103 has three DSPLLs.
The devices are available with both an integrated Crystal reference and an external XO reference option.

All devices support Free-run, Synchronous and Holdover modes as well as enhanced hitless switching minimizing the phase transients associated when switching between input clocks. These devices are programmable through the primary I^2C or SPI interface with in-circuit programmable non-volatile memory (NVM) to enable powering up with a known frequency configuration.

Programming the SKY63101/02/03 is easy with Skyworks ClockBuilder® Pro (CBPro) software.
The devices can be factory programmed, allowing them to power-up to known frequencies and settings, or shipped as “blank” devices to give more flexibility.

For more information, visit the Skyworks Sales Information page.

Applications

- 56G/112G/224G PAM4 SerDes clocking
- OTN muxponders and transponders
- 100/200/400/600/800G networking line cards
- Synchronous Ethernet
- Datacenter Switches
- Medical imaging
- Test and measurement
- 100G/200G/400G Optical Transceivers

Features

- Integrated Reference (BAW + optional crystal oscillator)
- Sixth-generation DSPLL and MultiSynth technologies
- ANY input to ANY combination of output frequencies up to 3.2 GHz
- Ultra-low phase jitter (<45 fs typical)
- Optional integrated Flash memory for in-field updates
- 1.8 V-only mode for low-power operation
- Enhanced hitless switching minimizes output phase transients (35 ps typ)
- Four differential or six single-ended inputs
- Input frequency range
  - Differential: 8 kHz to 1000 MHz
  - LVCMOS: 8 kHz to 250 MHz
- 16 Outputs
- Output frequency range
  - Differential: 8 kHz to 3.2 GHz
  - LVCMOS: 8 kHz to 250 MHz
- Fixed or user-adjustable output formats
- Simplified JA API interface backwards-compatible with Si5361/62/63 devices
- Full suite of status monitors
- SKY63101: 1 DSPLL, two MultiSynths
- SKY63102: 2 DSPLL, one MultiSynth
- SKY63103: 3 DSPLL, zero MultiSynths
- Pin-compatible with SKY69101/02/NetSync™ network synchronizers
- 64-LGA 9x9 mm
- ClockBuilder Pro Configuration Software
- For RoHS and other product compliance information, see the Skyworks Certificate of Conformance.

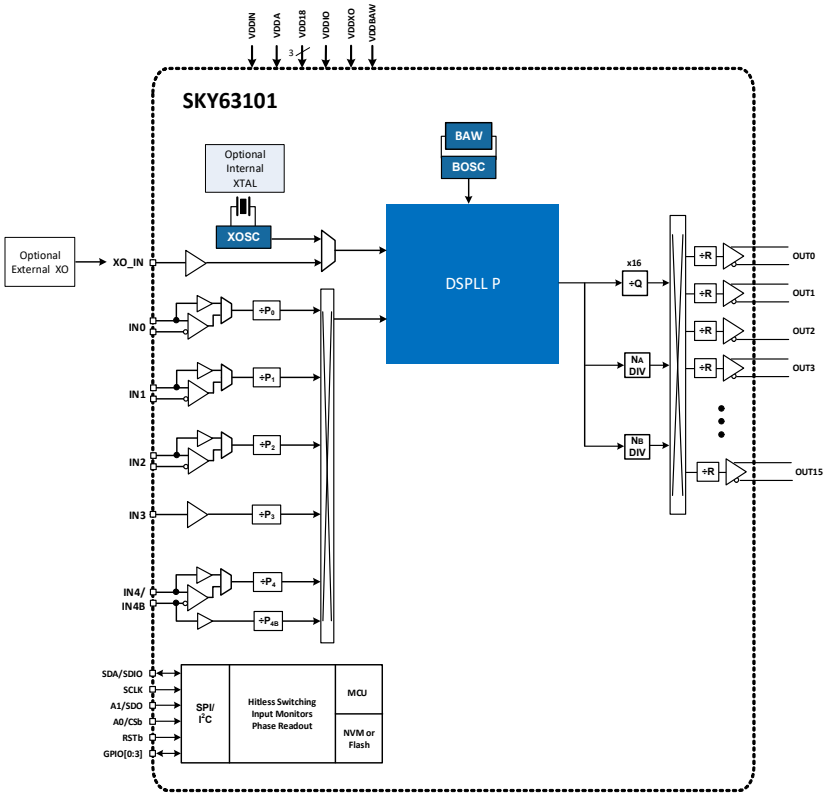


Figure 1. SKY63101 Simplified Block Diagram (1 x DSPLL + 2 x MultiSynth)

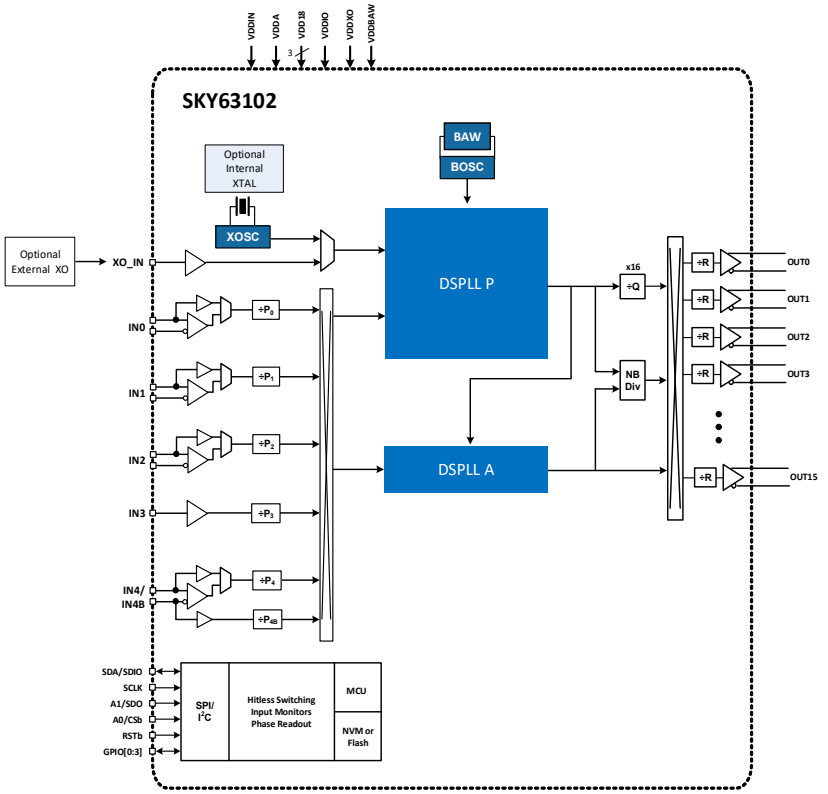


Figure 2. SKY63102 Simplified Block Diagram (2 x DSPLL + 1xMultiSynth)

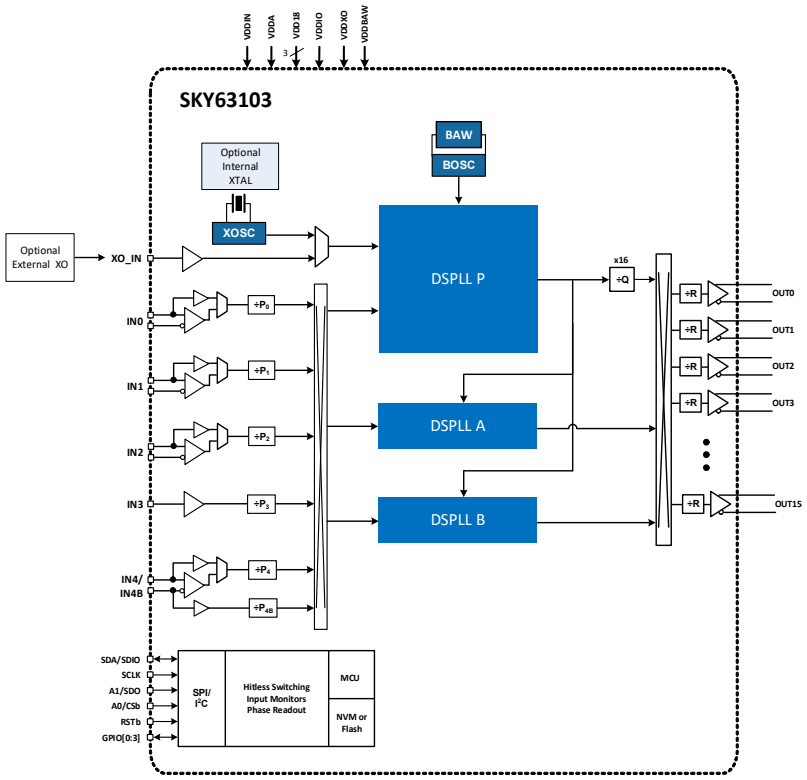


Figure 3. SKY63103 Simplified Block Diagram (3 x DSPLL)

1. Features List

- Integrated BAW and optional crystal oscillators eliminate external XTAL or XO
- Generates any output frequency in any format from any input frequency
- Utilizes sixth-generation DSPLL and MultiSynth technologies
- Ultra-low INTEGER mode jitter performance (DSPLLP+Q):
  - <45 fs RMS typ
- DSPLLA (SKY63102/03 only), DSPLLB (SKY63103 only)
  - Independent synchronization DSPLLs
  - <75 fs RMS typ
- Optional integrated Flash memory supports in-field re-programming of boot-up configuration
- On-chip temperature sensor and die temperature readout
- Programmable loop bandwidth: 20 Hz to 4 kHz
- Hitless input clock switching: automatic or manual with 35 ps typ phase transient
- Four differential inputs or up to six single-ended clock inputs:
  - Differential: 8 kHz to 1 GHz
  - CMOS: 8 kHz to 250 MHz
  - Gapped clock input support
- 16 differential or 32 single-ended clock outputs:
  - Integer Q dividers: 8 kHz to 3.2 GHz
  - Fractional Divider: 8 kHz to 650 MHz
  - CMOS: 8 kHz to 250 MHz
  - PCI-Express Gen 1 through Gen 7 compliant outputs
- User-programmable alarm thresholds
- Highly configurable outputs:
  - Fixed formats LVDS, S-LVDS, LVPECL, LVCMOS, CML, and HCSL
  - User-programmable signal amplitude
- Output-output skew: ±50 ps
- Automatic Free-run, Holdover, and Locked modes
- Zero Delay Mode for all PLLs
- Status monitoring (LOS, OOF, PHMON, FLOL and PLOL)
- Core voltage: 3.3 V, 1.8 V
- Output supply pins: 3.3 V, 2.5 V, 1.8 V
- Serial Interface: I^2C or SPI (3 or 4-wire)
- Frequency-on-the-fly for flexibility of configuration
- ClockBuilder Pro software tool simplifies device configuration
- Package: 64-Lead LGA, 9x9 mm
- Extended temperature range:
  - –40 to +95 °C ambient
  - –40 to +105 °C board
- Pb-free, RoHS compliant

2. Pin Descriptions

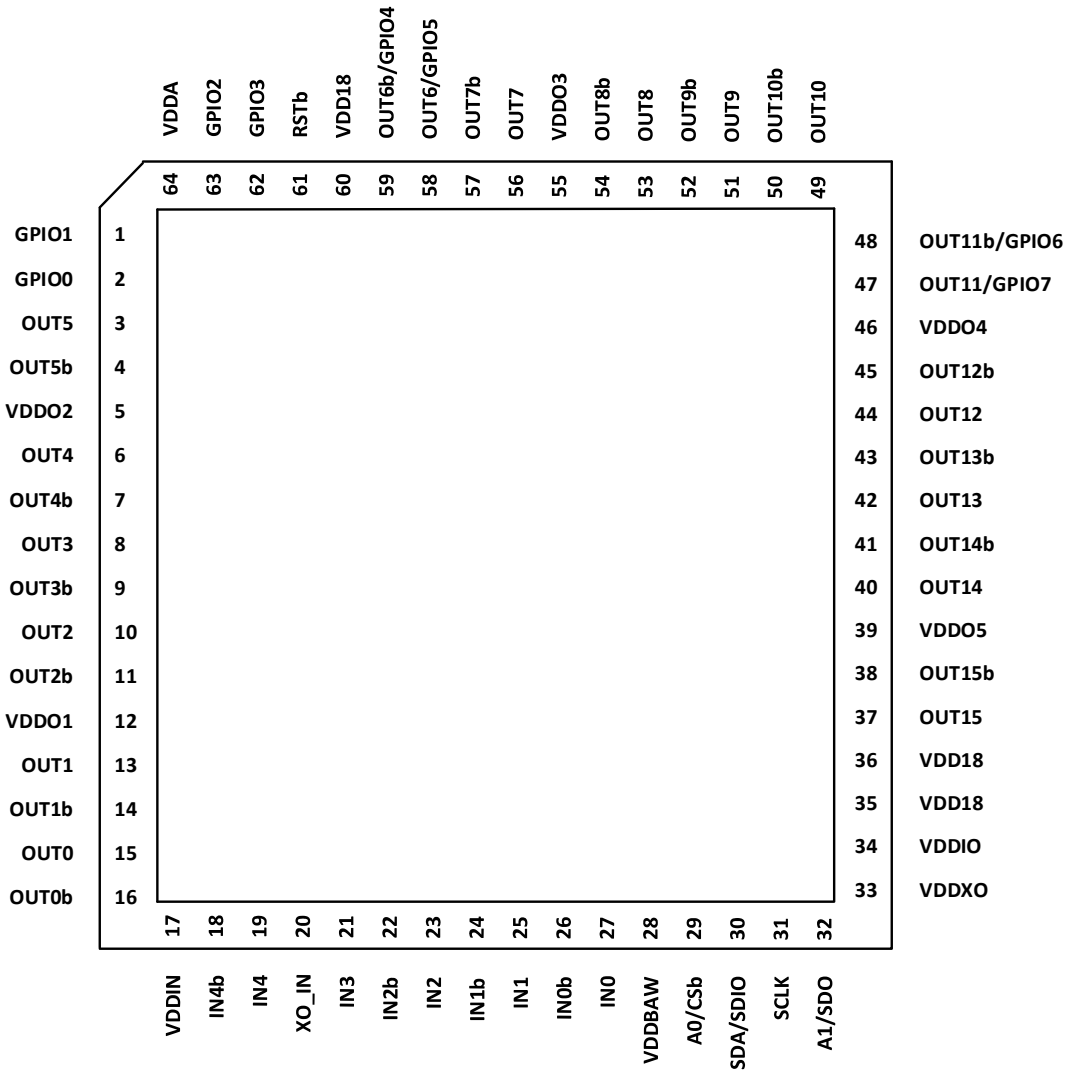


Figure 4. SKY63101/02/03 Pin Descriptions Diagram

Table 1. Pin Descriptions

Pin Name	Pin Number	Pin Type[1]	Function
Inputs			
XO_IN	20	I	**XO Input**: XO_IN is a single-ended input for an external XO. When the integrated crystal (XOSC) is used, leave XO_IN unconnected.
IN3	21	I	**Clock Input**: IN3 is a single-ended input only. IN3 can be disabled in ClockBuilder Pro and the pin left unconnected if unused. Refer to the SKY69101 Reference Manual for input termination options.
IN0	27	I	**Clock Inputs** IN0, IN1, IN2, and IN4 accept an input clock for synchronizing the device. They support both differential and single-ended clock signals. When operating in single-ended mode, input IN4 can provide two SE inputs each for a total of six inputs. Refer to the SKY63101/02/03 Family Reference Manual for input termination options. These pins are high-impedance and must be terminated externally. IN0–IN4 can be disabled in ClockBuilder Pro and the pins left unconnected if unused.
IN0b	26		
IN1	25		
IN1b	24		
IN2	23		
IN2b	22		
IN4	19		
IN4b	18		
Outputs			
OUT0b	16	O	**Output Clocks** The output clocks can be programmed as single-ended CMOS or differential LVDS, S-LVDS, CML, HCSL or ac-coupled LVPECL and support a programmable signal amplitude and common-mode voltage. Desired output signal format is configurable in CBPro. Termination recommendations are provided in the SKY63101/02/03 Reference Manual. Unused outputs should be left unconnected.
OUT0	15		
OUT1b	14		
OUT1	13		
OUT2b	11		
OUT2	10		
OUT3b	9		
OUT3	8		
OUT4b	7		
OUT4	6		
OUT5b	4		
OUT5	3		
OUT6b/GPIO4	59	I or O	**Output Clocks with GPIO Option** Output 6 can alternatively be assigned as two General Purpose Input/Outputs (GPIO4, GPIO5) that can be programmed to have any of the GPIO control functions listed in "5.9. GPIO Pins General Purpose Input or Output" on page 37. Regardless of whether Output 6 is functioning as a clock output or GPIO, the power supply is VDDO3.
OUT6/GPIO5	58		
OUT7b	57	O	**Output Clocks** The output clocks can be programmed as single-ended CMOS or differential LVDS, S-LVDS, CML, HCSL or ac-coupled LVPECL and support a programmable signal amplitude and common-mode voltage. The desired out- put signal format is configurable in CBPro. Termination recommendations are provided in the SKY63101/02/03 Reference Manual. Unused outputs should be left unconnected.
OUT7	56		
OUT8b	54		
OUT8	53		
OUT9b	52		
OUT9	51		
OUT10b	50		
OUT10	49		

Table 1. Pin Descriptions (Continued)

Pin Name	Pin Number	Pin Type[1]	Function
OUT11b/GPIO6	48	I or O	**Output Clocks with GPIO Option** Output 11 can alternatively be assigned as two General Purpose Input/Outputs (GPIO6, GPIO7) that can be programmed to have any of the GPIO control functions listed in "5.9. GPIO Pins General Purpose Input or Output" on page 37. Regardless of whether Output 11 is functioning as a clock output or GPIO, the power supply is VDDO4.
OUT11/GPIO7	47		
OUT12b	45	O	**Output Clocks** The output clocks can be programmed as single-ended CMOS or differential LVDS, S-LVDS, CML, HCSL or ac-coupled LVPECL and support a programmable signal amplitude and common-mode voltage. Desired output signal format is configurable in CBPro. Termination recommendations are provided in the "SKY63101/02/03 Reference Manual". Unused outputs should be left unconnected.
OUT12	44		
OUT13b	43		
OUT13	42		
OUT14b	41		
OUT14	40		
OUT15b	38		
OUT15	37		
Serial Interface			
A0/CSb	29	I	**Address Select 0/Chip Select** This pin functions as the hardware controlled LSB of the device address (A0) in I^2C mode. In SPI mode, this pin functions as the chip select input (active low). This pin is internally pulled-up and can be left floating if unused.
SDA/SDIO	30	I/O	**Serial Data Interface** This is the bidirectional data pin (SDA) for the I^2C mode, or the bidirectional data pin (SDIO) in the 3-wire SPI mode, or the input data pin (SDI) in the 4-wire SPI mode. When in I^2C mode, this pin must be pulled-up using an external resistor of at least 1 kΩ. No pull-up resistor is needed when in SPI mode.
SCLK	31	I	**Serial Clock Input** This pin functions as the serial clock input for both I^2C and SPI modes. When in I^2C mode, this pin must be pulled-up using an external resistor of at least 1 kΩ. No pull-up resistor is needed when in SPI mode.
A1/SDO	32	O	**Address Select 1/Serial Data Output** This input pin operates as the hardware controlled next to LSB portion of the device address (A1) in I^2C mode. In 4-wire SPI mode this pin operates as the serial data output (SDO). In 3-wire SPI mode leave this pin unconnected.

Table 1. Pin Descriptions (Continued)

Pin Name	Pin Number	Pin Type[1]	Function
Control/Status			
GPIO0	2	I or O	**Programmable General Purpose Input or Outputs** These pins can be programmed to the functions defined in GPIO Pin Descriptions. See the "SKY63101/02/03 Reference Manual" for more details.
GPIO1	1		
GPIO2	63		
GPIO3	62		
RSTb	61	I	**Reset Pin** This pin functions as an active-low reset input and is used to generate a device reset when held low for at least the specified Minimum Pulse Width. This resets the device back to a known state and reloads the NVM frequency plan and application. All clocks stop while the RSTb pin is asserted. If there is no frequency plan in NVM, the reset pin returns the device to the bootloader state in which it is waiting for the frequency plan and application to be downloaded by the host controller. This pin accepts a CMOS input and is internally pulled up with a ~20 kΩ resistor to VDDIO. VDDA and VDD18 must be powered up and stable before releasing RSTb. RSTb must not be toggled faster than the maximum update rate (f_{UR}) specification.
Power			
VDDIN	17	P	**Input Clock Supply Voltage** Supply voltage 3.3 V, 2.5 V or 1.8 V for the input clock buffers.
VDDO1	12	P	**Output Clock Supply Voltage 1–5** Supply voltage 3.3 V, 2.5 V, or 1.8 V for outputs. Leave VDDO pins of unused output drivers unconnected. An alternate option is to connect the VDDO pin to a power supply and disable the output driver to minimize current consumption. A 0402 1 µF capacitor should be placed very near each of these pins. The banks of outputs are powered as follows: VDDO1–OUT[0:3] VDDO2–OUT[4:5] VDDO3–OUT[6:9] VDDO4–OUT[10:13] VDDO5–OUT[14:15]
VDDO2	5		
VDDO3	55		
VDDO4	46		
VDDO5	39		
VDDA	64	P	**Core Analog Supply Voltage** This core supply can operate from a 3.3 V, 2.5 V or 1.8 V power supply. A 0402 1 µF capacitor should be placed very near each of these pins.
VDD18	35	P	**Core Supply Voltage 1.8 V** The device core operates from a 1.8 V supply. A 0402 1 µF capacitor should be placed very near each of these pins.
VDD18	36		
VDD18	60		
VDDBAW	28	P	**Reference Supply Voltage** Supply voltage of 3.3 V, 2.5 V or 1.8 V supported for the BAW oscillator reference (BOSC).
VDDXO	33	P	**Reference Supply Voltage** Supply voltage of 3.3 V, 2.5 V or 1.8 V supported for the crystal oscillator (XOSC) reference.
VDDIO	34	P	**Control, Status IO Clock Supply Voltage** Supply voltage 3.3 V, 2.5 V, or 1.8 V for the serial interface, Control, and Status inputs and outputs.
GND PAD	Package Bottom	P	**Exposed Die Attach Pad** The exposed die attach pad (ePAD) on the bottom of the package must be connected to electrical ground.

1. I = Input, O = Output, P = Power, N/C = No Connect.

3. Electrical Specifications

All minimum and maximum specifications are guaranteed and apply across the recommended operating conditions. Typical values apply at nominal supply voltages and an operating temp of 25 °C unless otherwise noted.

Table 2. Absolute Maximum Ratings[1,2,3]

Parameter	Symbol	Test Condition	Value	Unit
DC supply voltage	V_{DDIN}	<10 s	–0.5 to 3.8	V
	V_{DDXO}, V_{DDBAW}	<10 s	–0.5 to 3.8	V
	V_{DD18}	<10 s	–0.5 to 2.4	V
	V_{DDA}	<10 s	–0.5 to 3.8	V
	V_{DDO}	<10 s	–0.5 to 3.8	V
	V_{DDIO}	<10 s	–0.5 to 3.8	V
Input voltage range	V_{I1}	INx/INxb	–0.85 to 3.8	V
	V_{I2}	GPIO0-3, RSTb, SCLK, SDA/SDIO, A0/CSb	–0.5 to 3.8	V
Latch-up tolerance	LU		JESD78 Compliant	
ESD tolerance	HBM	100 pF, 1.5 kΩ	2.0	kV
Storage range	TSTG		–55 to 150	°C
Maximum junction temperature in operation	T_{JCT}		125	°C
Soldering temperature (Pb-free profile)[4]	T_{PEAK}		260	°C
Soldering time at T_{PEAK} (Pb-free profile)[4]	T_P		20 to 40	s

1. Exposure to maximum rating conditions for extended periods may reduce device reliability. Exceeding any of the limits listed here may result in permanent damage to the device.
2. RoHS-6 compliant.
3. For more packaging information, visit the Skyworks environmental compliance page.
4. The device is compliant with JEDEC J-STD-020.

ESD Handling: Industry-standard ESD handling precautions must be adhered to at all times to avoid damage to this device.

Table 3. Thermal Conditions

Parameter	Symbol	Test Condition	Typical Value		Unit
			JEDEC[1]	CEVB[2]	
Thermal resistance junction-to-ambient	θ_{JA}[3]	Still Air	20.7	9.2	°C/W
		1 m/s	14.2	6.6	°C/W
		2 m/s	12.7	6.2	°C/W
Thermal resistance junction-to-board	Ψ_{JB}[4,5]	Still Air	4.6	4.3	°C/W
Thermal resistance junction-to-top-center	Ψ_{JC}	Still Air	1.3	1.0	°C/W

1. Based on PCB dimension: 4" x 4.5", PCB thickness: 1.6 mm, number of Cu Layers: 2.
2. Customer EVB: ten-layer board, board dimensions: 9” x 9", all ten layers are copper-poured.
3. θ_{JA} can be used to calculate the junction temperature based on the ambient temperature and power dissipation for a given frequency plan. $T_J = T_A + (\theta_{JA} \times P_D)$.
4. T_A may not be applicable in applications in which the majority of the heat is dissipated through the PCB. For these applications, it is often preferred to refer to board temperature instead of ambient temperature.
5. Ψ_{JB} can be used to calculate the junction temperature based on the board temperature and power dissipation for a given frequency plan. $T_J = T_B + (\Psi_{JB} \times P_D)$. T_B should be measured as close to the DUT as possible since temperature may vary across the PCB.

Table 4. Recommended Operating Conditions

V_{DD18} = 1.8 V ±5%. All other supplies programmable: 3.3 V ±5%, 2.5 V ±5%, 1.8 V ±5%, T_A = –40 to 95 °C.

Parameter	Symbol	Test Condition	Min	Typ	Max	Unit
Ambient temperature	T_A		–40	25	95	°C
Board temperature	T_B		–40	65	105	°C
Junction temperature	TJ_{MAX}[1]		—	—	125	°C
Core supply voltage	V_{DD18}		1.71	1.80	1.89	V
	V_{DDA}[2,3]		3.14	3.30	3.47	V
		Low-power mode	1.71	1.80	1.89	V
	V_{DDXO}		3.14	3.30	V_{DDA}[2]	V
		Low-power mode	1.71	1.80	1.89	V
Input supply voltage	V_{DDBAW}		3.14	3.30	3.47	V
			2.38	2.50	2.62	V
			1.71	1.80	1.89	V
	V_{DDIN}		3.14	3.30	3.47	V
			2.38	2.50	2.62	V
			1.71	1.80	1.89	V
GPIO supply voltage	V_{DDIO}		3.14	3.30	3.47	V
			2.38	2.50	2.62	V
			1.71	1.80	1.89	V
Clock output driver supply voltage	V_{DDO}		3.14	3.30	3.47	V
			2.38	2.50	2.62	V
			1.71	1.80	1.89	V

1. Ambient temperature of 95 °C may not be possible with all configurations. This is dependent on device configuration. T_j cannot exceed a max of 125 °C.
2. VDDA must be greater than or equal to the highest voltage applied to the device. In Low-Power Mode, all voltage supplies must be set to 1.8 V.
3. In-field flash programming is supported down to VDDA = 1.8 V, but in-field NVM programming is only supported at VDDA = 3.3 V.

Table 5. Performance Characteristics

V_{DD18} = 1.8 V ±5%. All other supplies programmable 3.3 V ±5%, 2.5 V ±5%, 1.8 V ±5%, T_A = –40 to 95 °C.

Parameter	Symbol	Comment	Min	Typ	Max	Unit
Initial start-up time	t_{START}	Time from POR to when the device generates free-running clocks from NVM frequency plan.	—	45	52	ms
	t_{RDY}	POR to API ready	—	25	30	ms
PLL lock time[1]	t_{ACQ}	DSPLLP, IN = 156.25 MHz, BW = 100 Hz FLOL De-assert	—	0.40	0.50	s
		DSPLLP, IN = 156.25 MHz, BW = 100 Hz LOL De-assert	—	0.73	0.75	s
		DSPLLP, IN = 156.25 MHz, BW = 20 Hz FLOL De-assert	—	0.60	0.70	s
		DSPLLP, IN = 156.25MHz, BW = 20 Hz LOL De-assert	—	1.99	2.10	s
		DSPLLA/B, IN = 156.25 MHz, BW = 200 Hz FLOL De-assert	—	0.35	0.40	s
		DSPLLA/B, IN = 156.25 MHz, BW = 200 Hz LOL De-assert	—	0.45	0.50	s
Output delay adjustment	t_{QDIV}	Range[2]	$–T_{VCO}$ x 127	—	$+T_{VCO}$ x 127	ps
		Resolution		T_{VCO}	—	ps
		Resolution (fine delay enabled)	—	$T_{VCO/4}$	—	ps
Jitter peaking	J_{PK}	All PLLs	—	—	0.1	dB
Maximum phase transient during hitless switch[3]	t_{SWITCH}		—	35	150	ps
Pull-in range	ω_P		—	±100	—	ppm
Absolute input-to-output delay + variation[4,5]	t_{ZDELAY}	DSPLLP, DSPLLA, DSPLLB (ZDM)	–100	—	100	ps
	$t_{IODELAY}$	DSPLLP (Non ZDM)	–100	—	160	ps
Input-to-output delay variation[6]	$t_{IODELAY\_VAR}$	DSPLLA, DSPLLB (Non ZDM)	–300	—	79	ps

Table 5. Performance Characteristics (Continued)

V_{DD18} = 1.8 V ±5%. All other supplies programmable 3.3 V ±5%, 2.5 V ±5%, 1.8 V ±5%, T_A = –40 to 95 °C.

Parameter	Symbol	Comment	Min	Typ	Max	Unit
DSPLLP RMS jitter 12 kHz to 20 MHz[7]	Q Div	625 MHz	—	42	62	fs
		390.625 MHz	—	42	63	fs
		312.5 MHz	—	45	64	fs
		156.25 MHz	—	50	74	fs
		125 MHz	—	60	79	fs
	NA/NB Div	125 MHz	—	100	112	fs
		322.265625 MHz	—	74	95	fs
		644.53125 MHz	—	62	86	fs
DSPLLP RMS jitter 12 kHz to 20 MHz (4 MHz high-pass filtered)	Q Div	625 MHz	—	16	27	fs
		390.625 MHz	—	18	26	fs
		312.5 MHz	—	18	30	fs
DSPLLA/B RMS jitter 12 kHz to 20 MHz[7]	NA/NB Div	322.265625 MHz	—	79	107	fs
		155.52 MHz	—	108	138	fs

1. FLOL deasserts once frequency lock is achieved. LOL deasserts once both frequency and phase lock are achieved. Refer to "5.11.2. Lock Acquisition Mode" on page 39 for more details on LOL thresholds.
2. Output delay adjustment range vary depending on frequency plan. Output delay adjustment range (ns) is displayed in the "Output Skew Control" step of the CBPro Wizard. f_{VCO} range is 10.4 to 13.0 GHz.
3. Phase transient specification only applies to clock switches between two synchronous inputs to a DSPLL configured for a phase buildout clock switching mode in CBPro.
4. Input-to-output (IO) delay is measured at the output driver with respect to the input after the output phase has achieved a steady-state value.
5. I/O delay requires clock switching to be configured for Phase Pull-in in CBPro. IO delay is not specified for Phase Buildout (hitless) clock switching mode.
6. Only I/O delay VARIATION is specified for DSPLLA, DSPLLB. Absolute IO delay is dependent on frequency plan.
7. Jitter generation test conditions: f_{VCO} < 11 GHz: f_{OUT} LVDS, DSPLLP BW = 40 Hz.

Table 6. 100 MHz PCIe Jitter Performance Characteristics (without Spread Spectrum)

V_{DD18} = 1.8 V ±5%, V_{DDA} = V_{DDXO} = 3.3 V ±5%; All other supplies programmable 3.3 V ±5%, 2.5 V ±5%, 1.8 V ±5%, T_A = –40 to 95 °C.
Low-Power Mode: V_{DD18} = V_{DDIN} = V_{DDIO} = V_{DDXO} = V_{DDA} = V_{DDO} = 1.8 V ±5%, T_A = –40 to 95 °C.

Parameter	Symbol	Comment	Min	Typ	Max	PCI-SIG Limit[1]	Unit
100 MHz PCIe common clock jitter performance[2]	DSPLLP + Qdiv	Gen 1 (2.5GT/s)	—	14	56	86	ps P-P
		Gen 2 (5GT/s) Low Band	—	2	29	3000	fs_{RMS}
		Gen 2 (5GT/s) High Band	—	86	860	3100	fs_{RMS}
		Gen 3 (8GT/s)	—	24	172	1000	fs_{RMS}
		Gen 4 (16GT/s)	—	23	172	500	fs_{RMS}
		Gen 5 (32GT/s)	—	6	46	150	fs_{RMS}
		Gen 6 (64GT/s)	—	6	40	100	fs_{RMS}
		Gen 7 (128GT/s)	—	4	28	67	fs_{RMS}
	DSPLLP + NA/NB Div DSPLLA DSPLLB	Gen 1 (2.5GT/s)	—	14	57	86	ps P-P
		Gen 2 (5GT/s) Low Band	—	2	30	3000	fs_{RMS}
		Gen 2 (5GT/s) High Band	—	117	901	3100	fs_{RMS}
		Gen 3 (8GT/s)	—	34	182	1000	fs_{RMS}
		Gen 4 (16GT/s)	—	33	182	500	fs_{RMS}
		Gen 5 (32GT/s)	—	12	49	150	fs_{RMS}
		Gen 6 (64GT/s)	—	8	42	100	fs_{RMS}
		Gen 7 (128GT/s)	—	6	29	67	fs_{RMS}
100 MHz PCIe separate reference clock jitter performance[2]	DSPLLP + Qdiv	Gen 2 (5GT/s) Low Band	—	3	5	2120	fs_{RMS}
		Gen 2 (5GT/s) High Band	—	117	646	2190	fs_{RMS}
		Gen 3 (8GT/s)	—	30	129	707	fs_{RMS}
		Gen 4 (16GT/s)	—	30	129	495	fs_{RMS}
		Gen 5 (32GT/s)	—	11	54	177	fs_{RMS}
		Gen 6 (64GT/s)	—	10	54	106	fs_{RMS}
		Gen 7 (128GT/s)	—	7	38	71	fs_{RMS}
	DSPLLP + NA/NB Div DSPLLA DSPLLB	Gen 2 (5GT/s) Low Band	—	3	5	2120	fs_{RMS}
		Gen 2 (5GT/s) High Band	—	142	679	2190	fs_{RMS}
		Gen 3 (8GT/s)	—	37	137	707	fs_{RMS}
		Gen 4 (16GT/s)	—	37	137	495	fs_{RMS}
		Gen 5 (32GT/s)	—	15	57	177	fs_{RMS}
		Gen 6 (64GT/s)	—	12	57	106	fs_{RMS}
		Gen 7 (128GT/s)	—	9	40	71	fs_{RMS}

1. PCI-SIG does not specify a jitter limit for separate reference clock architectures. Instead the PCI-SIG specified simulation limit can be split evenly between transmitter and receiver clocks by dividing by the square root of 2 since their jitter is uncorrelated.
2. Jitter integration as specified by PCI-SIG in the PCI Express® Base Specification Revision 7.0.

Table 7. 100 MHz PCIe Jitter Performance Characteristics (with Spread Spectrum)

V_{DD18} = 1.8 V ±5%, V_{DDA} = V_{DDXO} = 3.3 V ±5%; All other supplies programmable 3.3 V ±5%, 2.5 V ±5%, 1.8 V ±5%, T_A = –40 to 95 °C.
Low-Power Mode: V_{DD18} = V_{DDIN} = V_{DDIO} = V_{DDXO} = V_{DDA} = V_{DDO} = 1.8 V ±5%, T_A = –40 to 95 °C.

Parameter	Symbol	Comment	Min	Typ	Max	PCI-SIG Limit[1]	Unit
100 MHz PCIe common clock jitter performance[2,3]	DSPLLP + NB Div	Gen 1 (2.5GT/s)	—	26	70	86	ps P-P
		Gen 2 (5GT/s) Low Band	—	5	43	3000	fs_{RMS}
		Gen 2 (5GT/s) High Band	—	684	1880	3100	fs_{RMS}
		Gen 3 (8GT/s)	—	272	459	1000	fs_{RMS}
		Gen 4 (16GT/s)	—	191	326	500	fs_{RMS}
		Gen 5 (32GT/s)	—	55	103	150	fs_{RMS}
		Gen 6 (64GT/s)	—	37	72	100	fs_{RMS}
		Gen 7 (128GT/s)	—	26	51	67	fs_{RMS}
100 MHz PCIe separate reference clock jitter performance[2,4]	DSPLLP + NB Div	Gen 2 (5GT/s) High Band	—	838	1047	2190	fs_{RMS}
		Gen 3 (8GT/s)	—	619	656	707	fs_{RMS}
		Gen 4 (16GT/s)	—	394	463	495	fs_{RMS}
		Gen 5 (32GT/s)	—	66	92	177	fs_{RMS}
		Gen 6 (64GT/s)	—	59	82	106	fs_{RMS}
		Gen 7 (128GT/s)	—	42	58	71	fs_{RMS}

1. PCI-SIG does not specify a jitter limit for separate reference clock architectures. Instead the PCI-SIG specified simulation limit can be split evenly between transmitter and receiver clocks by dividing by the square root of 2 since their jitter is uncorrelated.
2. Jitter integration as specified by PCI-SIG in the PCI Express® Base Specification Revision 7.0.
3. Common Clock spread spectrum modulation of –0.4%.
4. Separate Reference spread modulation of –0.4% Gen2 to Gen4, –0.3% Gen5 to Gen6, and –0.15% Gen7.

Table 8. DC Characteristics

V_{DD18} = 1.8 V ±5%. All other supplies programmable 3.3 V ±5%, 2.5 V ±5%, 1.8 V ±5%, T_A = –40 to 95 °C

Parameter	Symbol	Test Condition	Min	Typ	Max	Unit
Core supply current (V_{DD18} + V_{DDA})	I_{DD18}	SKY63101[1,2]	—	400	779	mA
		SKY63102[1,2]		405	786	mA
		SKY63103[1,2]	—	410	792	mA
	I_{DDA}	SKY63101[1,2]	—	200	236	mA
		SKY63102[1,2]	—	200	236	mA
		SKY63103[1,2]	—	200	236	mA
	I_{DD18_PD}	RSTb = 0	—	120	368	mA
	I_{DDA_PD}	RSTb = 0	—	13	15	mA
Peripheral supply current (V_{DDIN} + V_{DDIO} + V_{DDXO})	I_{DDIN} + I_{DDIO}	SKY63101[1,2]	—	43	61	mA
		SKY63102[1,2]	—	51	72	mA
		SKY63103[1,2]	—	60	83	mA
	I_{DDBAW}	SKY63101[1,2]	—	14	18	mA
		SKY63102[1,2]	—	14	18	mA
		SKY63103[1,2]	—	14	18	mA
	I_{DDXO}	SKY63101[1,2]	—	12	15	mA
		SKY63102[1,2]	—	11	15	mA
		SKY63103[1,2]	—	11	15	mA
	I_{DDIN_PD} + I_{DDIO_PD} + I_{DDXO_PD}	RSTb = 0	—	1	5	mA
Output buffer supply current (V_{DDOX})	I_{DDOX} (per output)	LVPECL (2.5 V, 3.3 V) @ 156.25 MHz[3]	—	24	26	mA
		LVDS (2.5 V, 3.3 V) @ 156.25 MHz[3]	—	13	15	mA
		S-LVDS (1.8 V) @ 156.25 MHz[3]	—	12	14	mA
		CML (1.8 V, 2.5 V, 3.3 V) @ 156.25 MHz[3]	—	14	17	mA
		3.3 V LVCMOS @ 156.25 MHz[4]	—	19	22	mA
		2.5 V LVCMOS @ 156.25 MHz[4]	—	15	17	mA
		1.8 V LVCMOS@ 156.25 MHz[4]	—	11	12	mA
		HCSL internal termination (1.8 V, 2.5 V, 3.3 V) @ 156.25 MHz[5]	—	20	23	mA
	I_{DDOX_PD}	RSTb = 0	—	0.23	0.3	mA

Table 8. DC Characteristics (Continued)

V_{DD18} = 1.8 V ±5%. All other supplies programmable 3.3 V ±5%, 2.5 V ±5%, 1.8 V ±5%, T_A = –40 to 95 °C

Parameter	Symbol	Test Condition	Min	Typ	Max	Unit
Total power dissipation	P_D	SKY63101[1]	—	2.10	3.10	W
		SKY63102[1]	—	2.15	3.15	W
		SKY63103[1]	—	2.20	3.20	W
		SKY63101 low-power mode[2]		1.4	2.31	W
		SKY63102 low-power mode[2]		1.4	2.35	W
		SKY63103 low-power mode[2]		1.4	2.40	W
Supply voltage ramp rate	T_{VDD}	Fastest V_{DD} ramp rate allowed on startup	—	—	100	V/ms

1. Typical test configuration: The following frequencies on 12 LVDS outputs: 4–156.25 MHz (Q), 2–312.5 MHz (Q), 1–125 MHz (Q), 1–100 MHz (NB), 1–50 MHz (NB), 2–644.53125 MHz (NA), 1–322.265625 MHz (NA). Excludes power in termination resistors. VDDIN = 1.8 V; VDDO = 3.3 V.
2. Typical test configuration: Same as Note 1, except all supplies set to 1.8 V for Low-Power Mode. Output formats changed to S-LVDS format.
3. Differential outputs terminated into an ac-coupled differential 100 Ω load.
4. LVCMOS outputs measured into a 5-inch, 50 Ω PCB trace with 5 pF load.
5. No external termination; amplitude 800 mVpp_se.

Table 9. Internal Reference Specifications[1,2]

Parameter	Symbol	Test Condition	Min	Typ	Max	Unit
Initial accuracy	—	25 °C	–10	0	+10	ppm
Frequency Stability	—	Over operating temperature range	–40	0	+40	ppm
Total Frequency Accuracy	—	Over operating temperature range (except aging)	–98	0	+98	ppm
Aging	—	10 years at 50 °C	–7	0	+7	ppm

1. These devices with integrated reference have been tuned with an internal 48 MHz reference to deliver optimum performance. It is important to note that connecting an external reference to a device that already has an integrated reference is not allowed. Doing so could lead to internal damage to the circuits.
2. Clocks that feature the integrated crystal may require a slightly longer settling time compared to the external crystal device. See the Reference Manual for more details.

Table 10. Input Specifications

V_{DD18} = 1.8 V ±5%. All other supplies programmable 3.3 V ±5%, 2.5 V ±5%, 1.8 V ±5%, T_A = –40 to 95 °C.

Parameter	Symbol	Test Condition	Min	Typ	Max	Units
Differential (INx/INxb)						
Input frequency range	f_{IN_DIFF}	Differential, ac coupled	0.008	—	1000	MHz
	f_{IN_SE}	Single-ended, ac coupled	0.008	—	250	MHz
Voltage swing	V_{IN_DIFF}	Differential, ac coupled	200	350 (LVDS) 800 (LVPECL)	1800	mVpp_se
	V_{IN_SE}	Single-ended, ac coupled	400	1600	1800	mVpp_se
Slew rate[1,2]	SR		0.4	—	—	V/ns
Duty cycle[3]	DC		40	—	60	%
Capacitance	C_{IN_DIFF}		—	2.5	—	pF
LVCMOS (INx/INxb)						
Input frequency range	f_{IN_LVCMOS}		0.008	—	250	MHz
Slew rate[1,2]	SR		0.2	0.4	—	V/ns
Input voltage	V_{IL}		—	—	V_{DDIN} x 0.3	V
	V_{IH}		V_{DDIN} x 0.7	—	—	V
Input resistance	R_{IN}		—	63	—	kΩ
Duty cycle[3]	DC		40	—	60	%
Capacitance	C_{IN_SE}		—	1.25	—	pF
LVCMOS (XO applied to XO_IN)						
Input frequency range	f_{IN_XO}		30.72	—	250	MHz
Slew rate[1,2]	SR	Single-ended, ac coupled	0.75	—	—	V/ns
Input voltage	V_{IL}		—	—	V_{DDXO} x 0.3	V
	V_{IH}		V_{DDXO} x 0.7	—	—	V
Input resistance	R_{IN}		—	63	—	kΩ
Duty cycle[3]	DC		40	—	60	%
Capacitance	C_{IN_XO}		—	1.25	—	pF
Other Control Input Pins: RSTb, FINC, FDEC, OE, PLLx_FORCE_HO, PLLx_INSEL[#], IN_FAIL[#]						
Update rate	f_{UR}	RSTb[4]	—	—	1	Hz
		FINC, FDEC	—	—	800	kHz
Input voltage	V_{IL}		—	—	V_{DDIO} x 0.3	V
	V_{IH}		V_{DDIO} x 0.7	—	—	V
Minimum pulse width	PW		150	—	—	ns
Programmable internal pullup, pulldown	R_{IN}		—	20	—	kΩ

1. Slew rate can be estimated using the following simplified equation: SR = ((0.8 – 0.2) x $V_{IN\_VPP\_se}$)/t_r.
2. The minimum slew rate on the input clock applied to INx/INxb is recommended to meet the specified input-to-output delay and close-in phase noise (<1 kHz) performance.
3. Applies to clock inputs used for a single frequency only, without PWM encoding.
4. Glitches and toggles on RSTb more frequent than f_{UR} may cause the device to lock up in reset. Power cycle the device to restore operation.

Table 11. Differential Clock Output Specifications

V_{DD18} = 1.8 V ±5%. All other supplies programmable = 3.3 V ±5%, 2.5 V ±5%, 1.8 V ±5%, T_A = –40 to 95 °C.

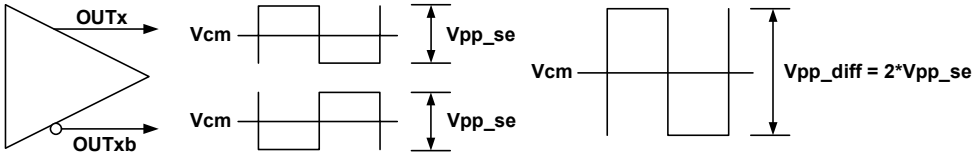
Parameter	Symbol	Test Condition		Min	Typ	Max	Units
Output frequency	f_{OUT}	Q Divider[1] (Grade A/B/C)		0.008	—	3200	MHz
		NA Divider, NB Divider[2]		0.008	—	650	MHz
Duty cycle	DC	f < 400 MHz		49.5	50.0	50.5	%
		400 MHz < f < 3.2 GHz		48.0	50.0	52.0	%
Output-to-output skew	T_{SK}	Q divider outputs, same differential format		–14	—	41	ps
		MultiSynth (NA or NB) outputs, same differential format, same MultiSynth					
OUT-OUTb skew[3]	T_{SK_OUT}	VDDO = 3.3 V	LVPECL, LVDS, CML, custom differential, f ≤160 MHz	1	—	16	ps
		VDDO = 2.5 V		2.2	—	29	ps
		VDDO = 3.3 V/2.5 V	LVPECL, LVDS, CML, custom differential, f > 160 MHz	–7	—	26	ps
		VDDO = 1.8 V	CML, S-LVDS, All frequencies	–5	—	28	ps
Output voltage swing[4]	V_{OUT}	VDDO = 3.3 V/2.5 V	LVDS	330xSF	360xSF	385xSF	mVpp_se
		VDDO = 1.8 V	S-LVDS	350xSF	375xSF	405xSF	mVpp_se
		VDDO = 3.3 V/2.5 V	AC-Coupled LVPECL	760xSF	830xSF	905xSF	mVpp_se
		VDDO = 3.3 V/2.5 V/1.8 V	CML	385xSF	420xSF	455xSF	mVpp_se
		VDDO = 3.3 V/2.5 V	Custom differential, 600 mVpp_se	590xSF	630xSF	680xSF	mVpp_se
Output voltage swing Scaling Factor (SF)	SF	f < 500 MHz		1.00	1.00	1.00	SF
		500 MHz < f < 1 GHz		0.83	1.01	1.10	SF
		1 GHz < f < 1.5 GHz		0.89	0.96	1.01	SF
		1.5 GHz < f < 2.5 GHz		0.64	0.70	0.77	SF
		f > 2.5 GHz		0.49	0.59	0.72	SF
Common mode voltage	V_{CM}	VDDO = 3.3 V/2.5 V	LVDS, AC-Coupled LVPECL, custom differential, CML	1.15	1.20	1.25	V
		VDDO = 1.8 V	S-LVDS, CML	0.85	0.90	0.95	V
Rise and fall times (20% to 80%)	t_r/t_f	VDDO = 3.3 V/2.5 V	AC-coupled LVPECL	—	125	260	ps
		VDDO = 3.3 V/2.5 V, f<100 MHz	LVDS, Custom differential	—	125	240	ps
		VDDO = 3.3 V/2.5 V, f≥100 MHz		—	125	230	ps
		VDDO = 1.8 V, f<500 MHz	S-LVDS	—	150	255	ps
		VDDO = 1.8 V, f≥500 MHz		—	125	230	ps
		VDDO = 3.3 V/2.5 V/1.8 V	CML	—	150	240	ps
Differential output impedance	Z_O	Differential formats		—	100	—	Ω

Table 11. Differential Clock Output Specifications (Continued)

V_{DD18} = 1.8 V ±5%. All other supplies programmable = 3.3 V ±5%, 2.5 V ±5%, 1.8 V ±5%, T_A = –40 to 95 °C.

Parameter	Symbol	Test Condition	Min	Typ	Max	Units
Power supply noise rejection[5]	PSR	25 kHz sinusoidal noise	—	–94	—	dBc
		100 kHz sinusoidal noise	—	–95	—	dBc
		500 kHz sinusoidal noise	—	–91	—	dBc
		1 MHz sinusoidal noise	—	–91	—	dBc
Output-to-output crosstalk[6]	$XTALK_{OUT}$	Differential outputs, same format	—	–95	—	dBc
Input-to-output crosstalk[7]	$XTALK_{IN}$	Differential input and output, same format	—	–90	—	dBc

1. Q dividers support output frequencies within the specified range equal to f_{VCO}/Q, where Q is an integer.
2. NA, NB MultiSynth support any output frequency within the specified range.
3. Skew between positive and negative output pins.
4. Output voltage swing is dependent on frequency range. Scale all values by the Output Voltage Swing Scaling Factor (SF). Voltage swing is specified in mVpp_SE as shown in the following figure.



5. Measured for a 156.25 MHz LVDS output frequency. 100 mVpp sine wave noise added to VDDO = 3.3 V and noise spur amplitude measured.
6. Crosstalk spur measured with the victim running at 156.25 MHz and the aggressor at 155.52 MHz. Victim and aggressor are separated by two unused channels.
7. Crosstalk spur measured with the victim running at 156.25 MHz on OUT0 and the aggressor at 155.52 MHz on IN3.

Table 12. HCSL Clock Output Specifications

V_{DD18} = 1.8 V ±5%. All other supplies programmable = 3.3 V ±5%, 2.5 V ±5%, 1.8 V ±5%, T_A = –40 to 95 °C.

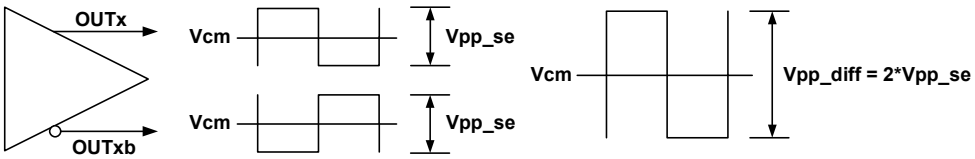
Parameter	Symbol	Test Condition			Min	Typ	Max	Units
Output frequency	f_{OUT}	Q divider, NA divider, NB divider[1]			0.008	—	600	MHz
Duty cycle HCSL Fast, 800 mV or 1200 mV, ext term HCSL Standard, 800 mVpp_se, int	DC	f < 400 MHz			49.5	50	50.5	%
		400 MHz < f < 600 MHz			48	50	52	%
Duty cycle HCSL Standard, 800 mVpp_se, int	DC	f < 400 MHz			48.5	50	51.5	%
		400 MHz < f < 600 MHz			46	50	54	%
Output-to-output skew	T_{SK}	Q divider outputs, same differential format			–14	—	41	ps
		MultiSynth (NA or NB) outputs, same differential format, same MultiSynth			–14	—	41	ps
OUT-OUTb skew[2]	T_{SK_OUT}	Skew between positive and negative output pins	VDDO = 3.3 V	HCSL Standard, 800 mVpp_se, int term	—	—	15	ps
				HCSL Standard, 800 mVpp_se, ext term	—	—	52	ps
				HCSL Fast, 800 mV or 1200 mV, ext term	—	—	29	ps
			VDDO = 2.5 V	HCSL Standard, 800 mVpp_se, int term	—	—	15	ps
				HCSL Standard, 800 mVpp_se, ext term	—	—	60	ps
				HCSL Fast, 800 mV or 1200 mV, ext term	—	—	37	ps
			VDDO = 1.8 V	HCSL Standard, 800 mVpp_se, int term	—	—	25	ps
				HCSL Standard, 800 mVpp_se, ext term	—	—	80	ps
				HCSL Fast, 800 mV, ext term	—	—	53	ps
Output voltage swing[3]	V_{OUT}	VDDO = 3.3 V/ 2.5 V/1.8 V		HCSL Standard, 800 mVpp_se, int term	740xSF	810xSF	960xSF	mVpp_se
		VDDO = 3.3 V/ 2.5 V/1.8 V		HCSL Standard, 800 mVpp_se, ext term	720xSF	800xSF	960xSF	mVpp_se
		VDDO = 3.3 V/2.5 V		HCSL Fast, 800 mVpp_se, ext term	735xSF	810xSF	960xSF	mVpp_se
		VDDO = 3.3 V/2.5 V		HCSL Fast, 1200 mVpp_se, ext term	1085xSF	1175xSF	1270xSF	mVpp_se
Output voltage swing Scaling Factor (SF) standard, 800 mVpp_se, int term	SF	f < 10 MHz			1	1	1	SF
		10 MHz < f < 100 MHz			0.96	0.96	0.98	SF
		100 MHz < f < 200 MHz			0.94	0.94	0.97	SF
		200 MHz < f < 400 MHz			0.90	0.90	0.94	SF
		f > 400 MHz			0.86	0.86	0.90	SF

Table 12. HCSL Clock Output Specifications (Continued)

V_{DD18} = 1.8 V ±5%. All other supplies programmable = 3.3 V ±5%, 2.5 V ±5%, 1.8 V ±5%, T_A = –40 to 95 °C.

Parameter	Symbol	Test Condition		Min	Typ	Max	Units
Output voltage swing Scaling Factor (SF) standard, 800 mVpp_se, ext term	SF	f < 10 MHz		1	1	1	SF
		10 MHz < f < 100 MHz		1.01	1.00	0.99	SF
		100 MHz < f < 200 MHz		0.95	0.96	0.98	SF
		200 MHz < f < 400 MHz		0.91	0.90	0.91	SF
		f > 400 MHz		0.80	0.90	0.96	SF
Output voltage swing Scaling Factor (SF) Fast, 800 or 1200 mVpp_se, ext term	SF	f < 10 MHz		1	1	1	SF
		10 MHz < f < 100 MHz		1.00	0.99	0.99	SF
		100 MHz < f < 200 MHz		0.97	0.98	0.99	SF
		200 MHz < f < 400 MHz		0.96	0.96	0.96	SF
		f > 400 MHz		0.90	0.94	0.98	SF
Common mode voltage	V_{CM}	VDDO = 3.3 V/ 2.5 V/1.8 V	HCSL 800 mVpp_se	0.35	0.425	0.52	V
		VDDO = 3.3 V/2.5 V	HCSL 1200 mVpp_se	0.55	0.6	0.68	V
Rise and fall times (20% to 80%)	t_r/t_f	VDDO=3.3 V/2.5 V/ 1.8 V	HCSL Fast, 800 or 1200 mVpp_se, ext term	—	270	400	ps
		VDDO=3.3 V/2.5 V/ 1.8 V	HCSL Standard, 800 mVpp_se, ext term	—	450	700	ps
		VDDO=3.3 V/2.5 V/ 1.8 V	HCSL Standard, 800 mVpp_se, int term	—	270	—	ps
Differential output impedance	Z_O	HCSL Standard Slew Rate, int term		—	100	—	Ω
		HCSL Standard Slew Rate, ext term		—	Hi-Z	—	Ω
		HCSL Fast Slew Rate, ext term		—	200	—	Ω
Output-to-output crosstalk[4]	$XTALK_{OUT}$	Differential outputs, same format		—	–95	—	dBc
Input-to-output crosstalk[5]	$XTALK_{IN}$	HCSL input and output, same format		—	–90	—	dBc

1. NA, NB MultiSynths support any output frequency within the specified range.
2. Skew between positive and negative output pins.
3. Output voltage swing is dependent on frequency range, HCSL slew rate, and HCSL termination settings. Scale all voltage swing values by the scaling factor (SF). Voltage swing is specified in mVpp_SE as shown in the following figure.



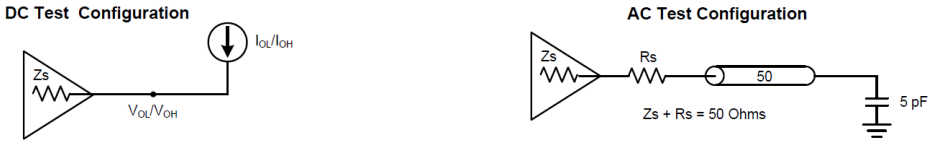
4. Crosstalk spur measured with the victim running at 156.25 MHz and the aggressor at 155.52 MHz. Victim and aggressor are separated by two unused channels.
5. Crosstalk spur measured with the victim running at 156.25 MHz on OUT0 and the aggressor at 155.52 MHz on IN3.

Table 13. LVCMOS Clock Output Specifications

V_{DD18} = 1.8 V ±5%. All other supplies programmable = 3.3 V ±5%, 2.5 V ±5%, 1.8 V ±5%, T_A = –40 to 95 °C

Parameter	Symbol	Test Condition	Min	Typ	Max	Units
Output frequency	f_{OUT}	Q Divider[1]	0.008	—	250	MHz
		NA or NB Divider[2]	0.008	—	250	MHz
Duty cycle	DC	f < 100 MHz	49.5	—	50.5	%
		100 MHz < f < 250 MHz	44	—	56	%
Output voltage high[3]	V_{OH}	VDDO = 3.3 V/2.5 V/1.8 V, I_{OH}= –8/–6/–4 mA, I_{OL} = 8/6/4 mA	V_{DDO} x 0.85	—	—	V
Output voltage low[3]	V_{OL}		—	—	V_{DDO} x 0.15	V
Rise and fall times (20% to 80%)[4,5]	t_r/t_f	LVCMOS	0.39	0.8	1.37	ns

1. Q dividers support output frequencies within the specified range equal to $f_{VCO/Q}$ where Q is an integer.
2. NA, NB MultiSynths support any output frequency within the specified range.
3. V_{OL}/V_{OH} is measured at I_{OL}/I_{OH} as shown in the DC Test Configuration portion of the drawing below.
4. A 15 to 25 Ω series termination resistor (Rs) is recommended to help match the source impedance to a 50 Ω PCB trace. A 5 pF capacitive load is assumed as shown in the AC Test Configuration portion of the drawing below.



5. SRL LVCMOS format clocks are intended only for low frequency clock applications.

Table 14. Output Status Pin Specifications

VDDIO = 3.3 V ±5%, 2.5 V ±5%, 1.8 V ±5%, T_A = –40 to 95 °C. Low-Power Mode: VDDIO = 1.8 V ±5%.

Parameter	Symbol	Test Condition	Min	Typ	Max	Units
Status Output Pins (GPIO, SDA)						
Output voltage high[1]	V_{OH}	I_{OH} = –2 mA	V_{DDIO} x 0.85	—	—	V
Output voltage low	V_{OL}	I_{OL} = 2 mA	—	—	V_{DDIO} x 0.15	V

1. The V_{OH} specification does not apply to the open-drain SDA output when the serial interface is in I^2C mode. V_{OL} remains valid in all cases.

Table 15. I²C Timing Specifications (SCL, SDA)

V_{DD18} = 1.8 V ±5%. All other supplies programmable 3.3 V ±5%, 2.5 V ±5%, 1.8 V ±5%, T_A = –40 to 95 °C.

Parameter	Symbol	Test Condition	Standard Mode 100 kbps		Fast Mode 400 kbps		Unit
			Min	Max	Min	Max	
SCL clock frequency	f_{SCL}		—	100	—	400	kHz
SMBus timeout	—		25	35	25	35	ms
Hold time (repeated) START condition	$t_{HD:STA}$		4.0	—	0.6	—	µs
Low period of the SCL clock	t_{LOW}		4.7	—	1.3	—	µs
HIGH period of the SCL clock	t_{HIGH}		4.0	—	0.6	—	µs
Setup time for a repeated START condition	$t_{SU:STA}$		4.7	—	0.6	—	µs
Data hold time	$t_{HD:DAT}$		100	—	100	—	ns
Data setup time	$t_{SU:DAT}$		250	—	100	—	ns
Rise time of both SDA and SCL signals	t_r		—	1000	20	300	ns
Fall time of both SDA and SCL signals	t_f		—	300	—	300	ns
Setup time for STOP condition	$t_{SU:STO}$		4.0	—	0.6	—	µs
Bus free time between a STOP and START condition	t_{BUF}		4.7	—	1.3	—	µs
Data valid time	$t_{VD:DAT}$		—	3.45	—	0.9	µs
Data valid acknowledge time	$t_{VD:ACK}$		—	3.45	—	0.9	µs

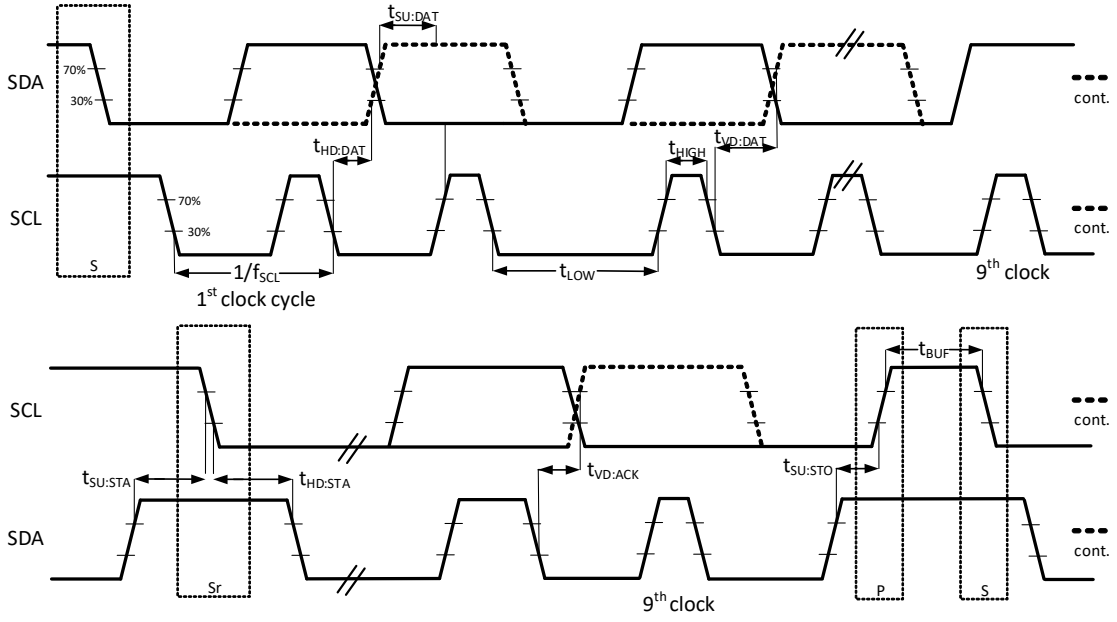


Figure 5. I²C Serial Port Timing Standard and Fast Modes

Table 16. SPI Timing Specifications (Four-Wire)

V_{DD18} = 1.8 V ±5%. All other supplies programmable 3.3 V ±5%, 2.5 V ±5%, 1.8 V ±5%, T_A = –40 to 95 °C

Parameter	Symbol	Min	Typ	Max	Unit
SCLK frequency	f_{SPI}	—	—	30	MHz
SCLK duty cycle	T_{DC}	40	—	60	%
SCLK period	T_C	33.333	—	—	ns
Delay time, SCLK Fall to SDO active	T_{D1}	—	12.5	20	ns
Delay time, SCLK Fall to SDO	T_{D2}	—	10	15	ns
Delay time, CSb rise to SDO tri-state	T_{D3}	—	10	20	ns
Setup time, CSb to SCLK	T_{SU1}	5	—	—	ns
Hold time, SCLK Fall to CSb	T_{H1}	5	—	—	ns
Setup time, SDI to SCLK rise	T_{SU2}	5	—	—	ns
Hold time, SDI to SCLK rise	T_{H2}	5	—	—	ns
Delay time between chip selects (CSb)	T_{CS}	5	—	—	µs

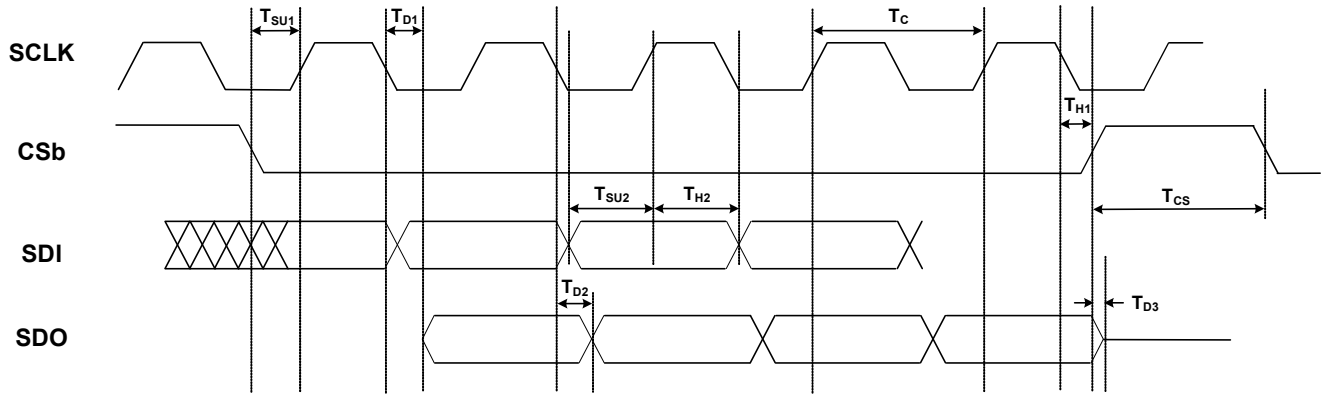


Figure 6. Four-Wire SPI Serial Interface Timing

Table 17. SPI Timing Specifications (Three-Wire)

V_{DD18} = 1.8 V ±5%. All other supplies programmable 3.3 V ±5%, 2.5 V ±5%, 1.8 V ±5%, T_A = –40 to 95 °C

Parameter	Symbol	Min	Typ	Max	Unit
SCLK frequency	f_{SPI}	—	—	30	MHz
SCLK duty cycle	T_{DC}	40	—	60	%
SCLK period	T_C	33.33	—	—	ns
Delay time, SCLK fall to SDIO turn-on	T_{D1}	—	12.5	20	ns
Delay time, SCLK fall to SDIO next-bit	T_{D2}	—	10	15	ns
Delay time, CSb rise to SDIO tri-state	T_{D3}	—	10	20	ns
Setup time, CSb to SCLK	T_{SU1}	5	—	—	ns
Hold time, CSb to SCLK fall	T_{H1}	5	—	—	ns
Setup time, SDI to SCLK rise	T_{SU2}	5	—	—	ns
Hold time, SDI to SCLK rise	T_{H2}	5	—	—	ns
Delay time between chip selects (CSb)	T_{CS}	5	—	—	µs

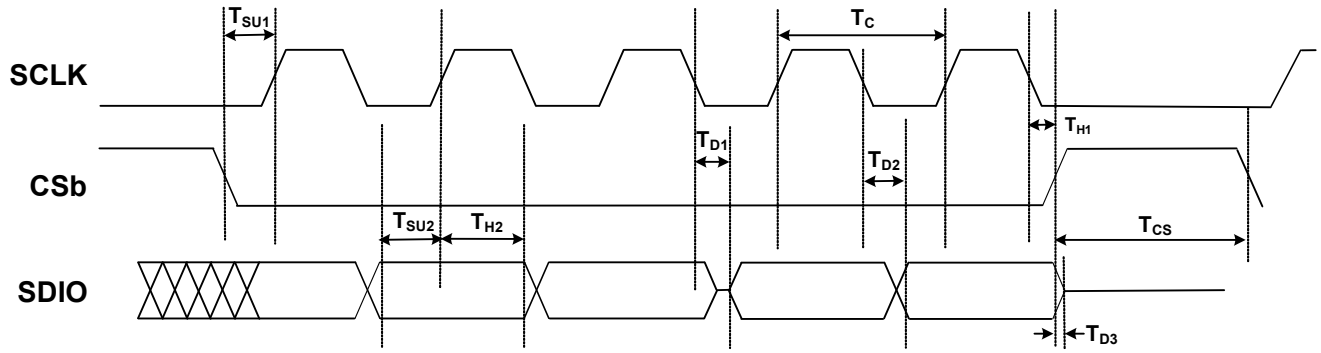


Figure 7. Three-Wire SPI Serial Interface Timing

4. Typical Operating Characteristics

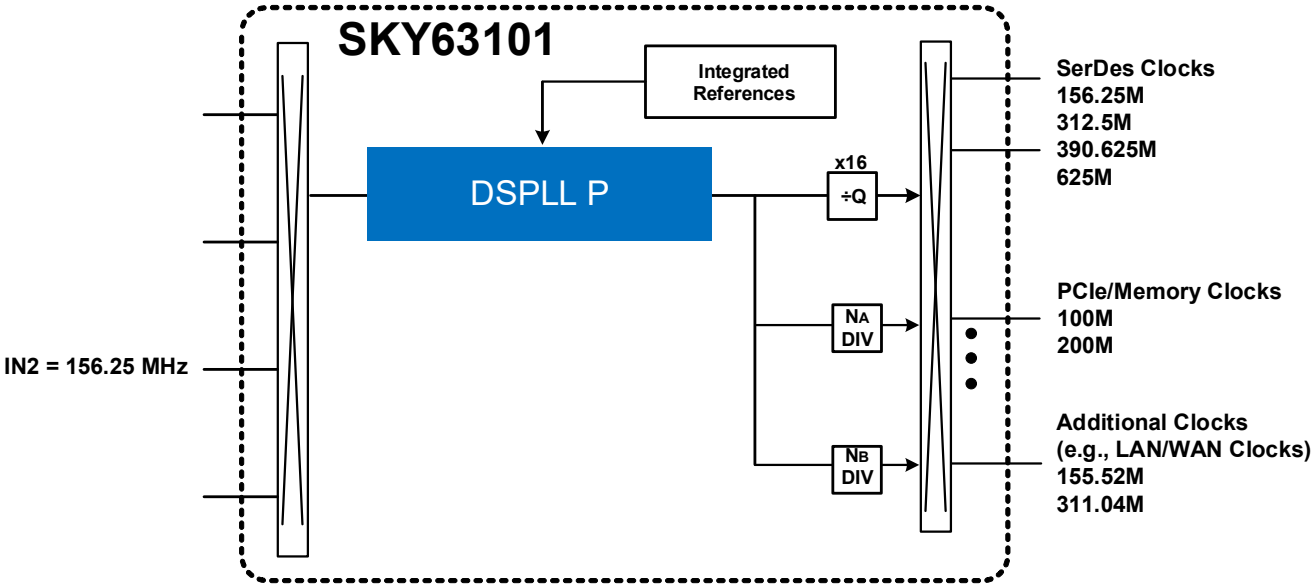


Figure 8. SKY63101 Typical Operating Circuit

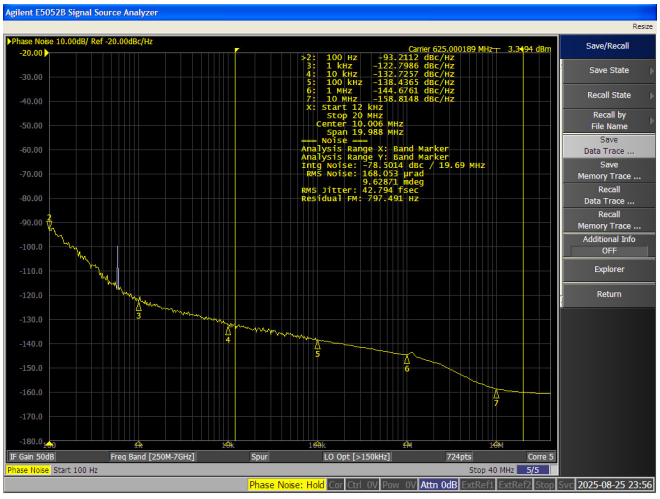


Figure 9. 42 fs RMS Jitter for 625 MHz SerDes Clocks

Figure 10. 43 fs RMS Jitter for 390.625 MHz SerDes Clocks

Figure 11. 45 fs RMS Jitter for 312.5 MHz SerDes Clocks

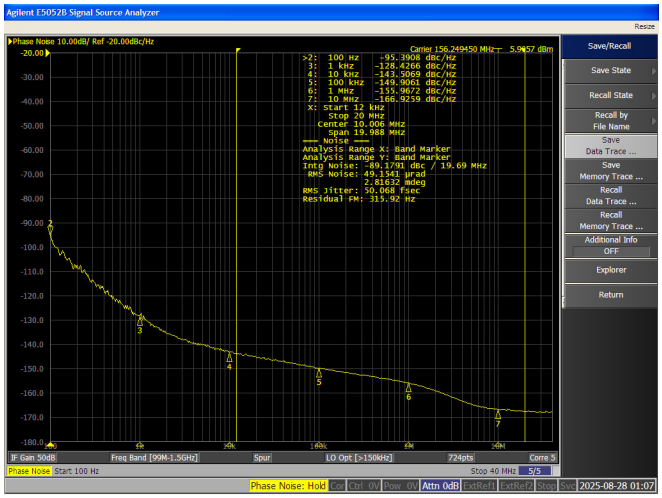


Figure 12. 50 fs RMS Jitter for 156.25 MHz SerDes Clocks

5. Functional Description

The SKY63101/02/03's sixth-generation BAW-based DSPLLs provides jitter attenuation and any-frequency multiplication of the selected input frequency. Fractional input dividers (P) allow the DSPLL to perform hitless switching between input clocks (INx) that are fractionally related. Input switching is controlled manually or automatically using an internal state machine. The integrated BAW oscillator (BOSC) and crystal oscillator (XOSC) provide a low jitter frequency reference which determines output frequency stability and accuracy while the device is in free-run or holdover mode. These devices are available with an integrated XTAL reference for greater space savings or an external XO reference. The high-performance Q dividers generate integer related output frequencies and the MultiSynth dividers (N) generate fractionally related output frequencies. A crosspoint switch connects any of the Q divider or MultiSynth generated frequencies to any of the outputs. Additional integer division (R) determines the final output frequency.

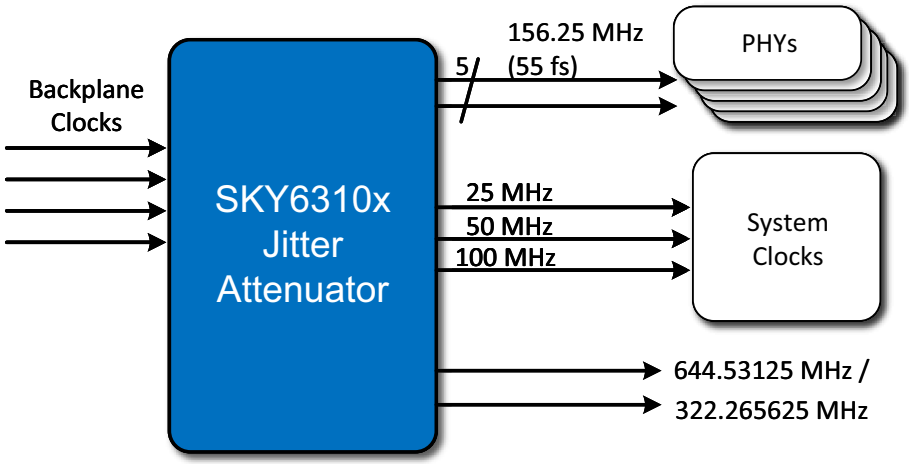


Figure 13. SKY63101/02/03 Typical 56G/112G SerDes Application (Up to Three Domains)

5.1. Frequency Configuration

The frequency configuration of the DSPLL(s) is programmable through the serial interface and can also be stored in non-volatile memory or internal flash depending on the grading option. The combination of input dividers (P), fractional frequency multiplication (M), integer output division (Q), fractional output division (N), and integer output division (R) allows the generation of virtually any output frequency on any of the outputs. All divider values for a specific frequency plan are easily determined using the CBPro utility.

5.2. DSPLL Loop Bandwidth Initial Lock and Fast Lock Settings

The DSPLL loop bandwidth determines the amount of input clock jitter attenuation. Each DSPLL has a configurable loop bandwidth. The DSPLL will always remain stable with low peaking regardless of the loop bandwidth selection.

Each of the DSPLLs, have configurable loop bandwidths. There are three configurations, each has a separate setting for the loop bandwidth:

- **Initial Lock Bandwidth**—The PLL uses this bandwidth when it exits the free-run mode and attempts to lock to a new input clock.
- **Loop Bandwidth**—This sets the bandwidth of the PLL once lock to an input is achieved.
- **Fastlock Bandwidth**—This sets the bandwidth of the PLL when exiting from holdover.

Selecting a low DSPLL loop bandwidth will generally lengthen the lock acquisition time. The fastlock feature allows setting a temporary Fastlock Loop Bandwidth that is used during the lock acquisition process. The DSPLL will revert to its normal loop bandwidth once lock acquisition has completed.

See the Reference Manual and CBPro for more information, recommendations, and limits for setting PLL loop bandwidths for different configurations.

5.3. Inputs

These devices have up to four differential inputs but can also be configured for up to six CMOS inputs, or any combination of differential and CMOS inputs.

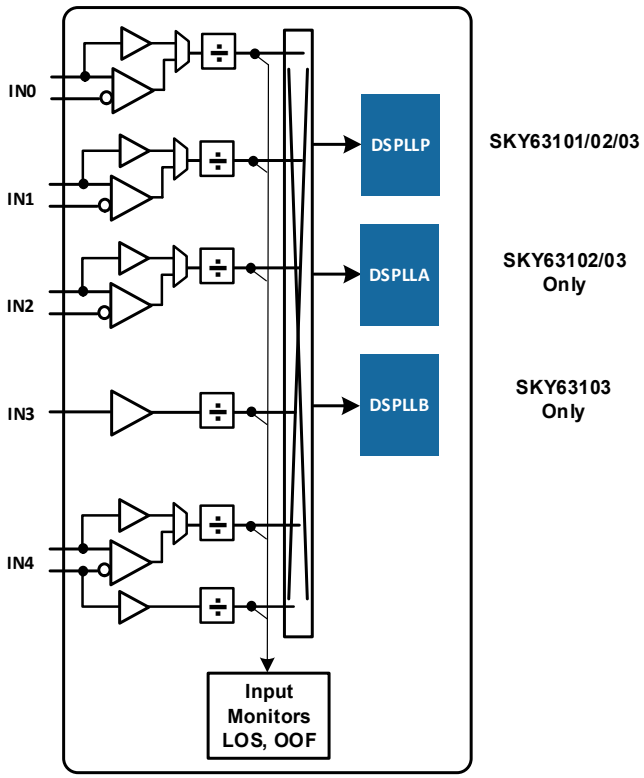


Figure 14. Input Structure

5.3.1. XO_IN

Grading options allow the user to use an integrated XTAL or to connect an external crystal oscillator (XO) directly to the XO_IN pin (Connecting an external XO to a device with a built-in crystal can damage the part). When using an external XO, it's important to select one that meets the jitter performance requirements of the end application. See the SKY63101/02/03 Recommended XTAL, XO, VCXO, TCXO, and OCXO Reference Manual for more details.

5.3.2. Inputs (IN0–IN4)

The SKY63101/02/03 supports up to four differential inputs (IN0, IN1, IN2, IN4). IN3 is a dedicated single-ended input. IN4 can be configured as one differential input or two CMOS inputs (IN4/IN4B). This allows support for up to six CMOS inputs, or any combination of differential and CMOS inputs.

5.3.3. Input Terminations

Refer to the "SKY63101/02/03 Reference Manual" for guidance on input terminations.

5.3.4. Input Selection

Input selection for any of the PLLs can be controlled manually through pin control, API command, or automatically using an internal state machine. Each DSPLL has its own state machine.

5.3.4.1. Input Divider

The device utilizes multiple classes of both fractional and integer frequency dividers. The CBPro software chooses the optimal divide values based on the user-defined frequency plan. Refer to the "SKY63101/02/03 Reference Manual" for guidance on input dividers.

5.3.4.2. Manual Input Selection

In Manual mode, the input selection is made by defining a GPIO pin as an input select pin and changing the input pin voltage level, or by writing an API command. Any of the inputs are available to any of the PLLs through a crosspoint input selection switch. If there is no clock signal on the selected input, or if the input is not valid due to LOS/OOF/PHMON input alarms, the PLL will automatically enter Free-Run/Holdover mode. This applies to all the DSPLLs.

5.3.4.3. Phase Readout PHRD

The Phase Readout Device API can be used to read and measure the phase between multiple input clocks to the SKY63101/02/03. Unused inputs that are not assigned to a DSPLL can also be configured as phase readout (PHRD) or phase readout feedback (PHRD_FB) inputs. These inputs can be used to measure the phase of an output of the SKY63101/02/03 to the input(s) of known phase. PHRD and PHRD_FB inputs use the same alarms (LOS/OOF/PHMON) as the other clock inputs, but they are not assigned to a DSPLL.

5.3.4.4. Automatic Input Selection

When configured in this mode, each of the PLLs automatically selects a valid input that has the highest configured priority. The priority scheme is independently configurable for each PLL and supports revertive or non-revertive selection. All inputs are continuously monitored for loss of signal (LOS), invalid frequency range (OOF), and phase (PHMON). Only valid inputs that have no LOS, OOF or phase monitor (PHMON) alarms can be selected for synchronization by the automatic state machine. The PLL(s) will enter Free-Run or Holdover mode if there are no valid inputs available.

5.3.5. Unused Inputs

Unused inputs should be configured as “Unused (Powered Down)”, and the pins may be left unconnected or ac-coupled to ground. Refer to the “SKY63101/02/03 Reference Manual” for recommendations on how to minimize system noise on any CMOS input or any differential input configured as “Enabled” but not actively being driven by a clock.

5.4. Input Clock Switching

Clock inputs to the SKY63101/02/03 can be either from the same source (0 ppm, same nominal frequency) or different sources (non-0 ppm different nominal frequency). The SKY63101/02/03 automatically determines the optimal switching mode depending on the nominal frequency difference between the clocks at the time of the switch. When switching between 0 ppm inputs, the SKY63101/02/03 performs either a hitless switch with phase buildout (PBO) or a phase pull-in (PPI) switch, depending on the setting in CBPro. When switching between non-0 ppm offset, the SKY63101/02/03 performs a frequency-ramped Input switch with user-programmable frequency ramp rate. Refer to the SKY63101/02/03 Reference Manual for additional guidance on input clock switching modes. All input clock switches are glitchless meaning there will be no runt pulses generated at the output during the transition.

5.4.1. Hitless Input Switching for 0 ppm clocks Phase Buildout PBO

SyncE applications require that transients are kept to a minimum when switching between inputs.
Hitless switching with phase buildout (PBO) is a feature that prevents a phase offset from propagating to the output when switching between two clock inputs that have a fixed phase relationship. A hitless switch can only occur when the two input frequencies are frequency locked, meaning that the nominal frequencies are the same (0 ppm). Due to the nature of hitless switching, the input-to-output delay of the PLL is not preserved. The DSPLL simply absorbs the phase difference between the two input clocks during an input switch. The phase buildout feature supports clock frequencies down to a minimum input frequency of 8 kHz.

5.4.2. Phase Pull-In (PPI) Input Switching for 0 ppm clocks

In some applications, the output phase must track the input phase with minimal delay. When the application requires the input-to-output delay to be preserved after clock switching, the phase pull-in clock switching mode should be selected. In this mode, the output phase will be pulled in at a user-programmable ramp rate referred to as the PPI slope (ns/s). With phase pull-in switching, the output phase always aligns with the newly selected input. PPI is always enabled for zero-delay mode applications.

5.4.3. Ramped Input Switching for non-0 ppm clocks

The ramped switching feature allows the DSPLLs to switch between two input clock frequencies that are non-0 ppm without an abrupt frequency transient at the output. When the two input clock frequencies are not the same nominal frequency, the DSPLL will pull in the frequency difference between inputs at the ramp rate that is programmable in CBPro from ppb/s to ppm/s. The Loss-of-Lock (LOL) and LOOP_FILTER_RAMP_IN_PROGRESS indicators (accessible through the Device API) will assert while the DSPLL is ramping to the new clock frequency.

5.4.4. Gapped Input Clocks

The DSPLL supports locking to an input clock that has missing periods. This is also referred to as a gapped clock. The purpose of gapped clocking is to modulate the frequency of a periodic clock by selectively removing some of its cycles. Gapping a clock severely increases its jitter so a phase-locked loop with high jitter tolerance and low loop bandwidth is required to produce a low-jitter periodic clock. The resulting output will be a periodic non-gapped clock with an average frequency of the input with its missing cycles. Refer to the SKY63101/02/03 Reference Manual for guidance on implementing gapped clocks on this device. For more information on gapped clocks, see “AN561: Introduction to Gapped Clocks and PLLs”.

5.5. Outputs

The SKY63101/02/03 supports 16 differential output drivers with configurable voltage swing and common mode voltage covering a wide variety of differential signal formats. In addition to preset differential levels such as LVPECL, LVDS, S-LVDS, CML and HCSL, the SKY63101/02/03 can also be programmed to a custom differential threshold that allows the signal to be sent directly to chipsets from vendors like Broadcom without complicated termination circuits simplifying the complexity of the board layout.

The outputs can also be configured as single-ended LVCMOS (3.3 V, 2.5 V, or 1.8 V) providing up to 32 single-ended outputs, or any combination of differential and single-ended outputs. The outputs have power supply pins (VDDOx) for output driver groups of 4-2-4-4-2, which can be powered at 3.3 V, 2.5 V, or 1.8 V. The LVCMOS output voltage is set by the VDDOx pin. Refer to "2. Pin Descriptions" on page 5.

5.5.1. Output Crosspoint

A crosspoint allows any of the output drivers to connect with any of the PLLs. A digital output delay adjustment is possible on each of the Q divider outputs to provide output-to-output alignment for the same output source. The crosspoint configuration and delay adjustments are programmable and are stored in NVM so that the desired output configuration is ready at power-up.

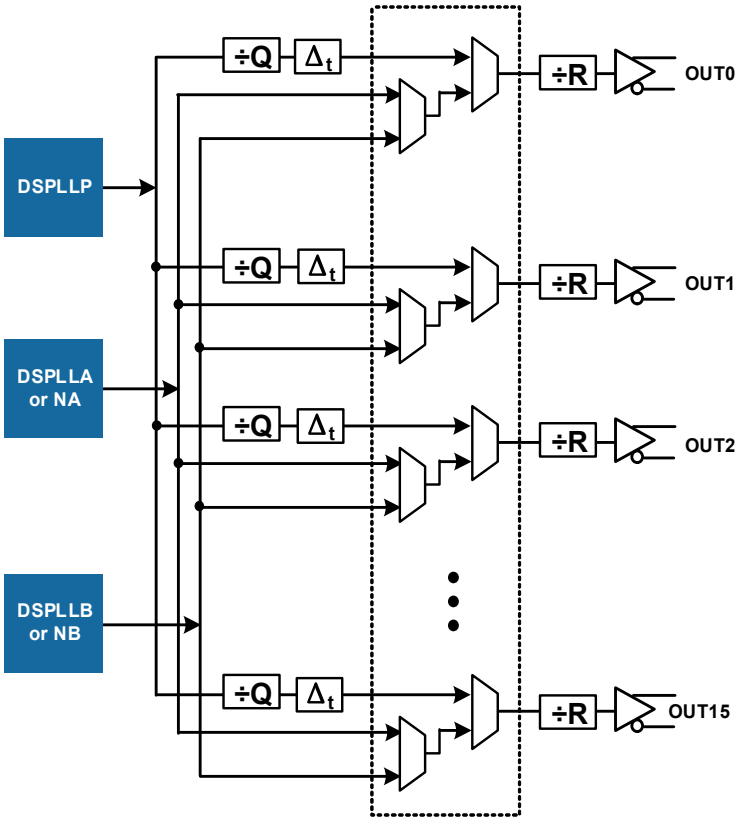


Figure 15. Output Structure

5.5.2. Differential and LVCMOS Output Terminations

Refer to the "SKY63101/02/03 Reference Manual" for guidance on output terminations.

5.5.3. Output Enable Disable

Each output driver may be enabled/disabled through programmable GPIO pins. There are three output enable groups (OE0, OE1, and OE2), which are logically OR'd together to determine which outputs are enabled at any point in time. CBPro allows the control and selection of the GPIO pin mapping to the outputs.

Outputs may also be enabled/disabled using the device API. If an output is assigned as GPIO controlled, the GPIO can be logically ORed or ANDed with the API command. The API controlled output enable allows for more flexibility than the GPIO control as any of the outputs can be individually enabled/disabled via an API command.

5.5.4. State of Disabled Output

The disabled state of an output driver may be configured as stop high, stop low, or Hi-Z. CMOS outputs <2 MHz can also be configured as Hi-Z with weak internal pullup/down.

Differential outputs, when disabled, will maintain the output common-mode voltage even while the output is not toggling. This minimizes disturbances when disabling and enabling clock outputs.

5.5.5. Output Dividers

The device utilizes both integer Q dividers and fractional NA, NB MultiSynth output dividers. The ClockBuilder Pro software chooses the optimal divide values based on the user-defined frequency plan.

A summary of each class of divider is listed below:

1. Output Q Divider: Q0–Q15
   -Integer Only Divide Value
   -Open loop divider taps directly off VCO
2. DSPLLA/B Feedback M Divider: MA, MB
   -Integer or Fractional Divide Value
3. Output N Divider: NA, NB
   -MultiSynth Divider, Integer or Fractional Divide Value
4. Output Divider: R0–R15
   -Integer Only Divide Value
5. Synchronized Dual Outputs
   -If one N divider is used in a closed loop fashion and the other N divider is used in an open loop fashion, the dividers may be cascaded so that the output of each N-divider is derived from the same input clock source and is capable of having a fractional frequency relationship.

5.5.6. Output Skew Control

Output skew control allows outputs that are derived from the Q dividers to be phase adjusted in steps of $1/f_{VCO}$, or $1/(4 \times f_{VCO})$ when the fine adjust is enabled. The exact skew adjustment and step sizes are reported on the Output Skew Control Tab of the CBPro Wizard.

5.5.7. PCIe Outputs

This device supports 100 MHz PCI-Express (Peripheral Component Interconnect Express, PCIe) Gen 1 through Gen 7 compliant outputs.

Compliance to PCIe standards is important to ensure specifications are met as well as to ensure device compatibility and seamless integration across all products. Skyworks “PCIe Clock Jitter Tool” is an easy-to-use GUI that guides users through a step-by-step process to generate compliance analysis results.

Refer to the “SKY63101/02/03 Reference Manual” for more information.

5.6. DSPLLP with Output Q-Divider (High Performance Path)

DSPLLP is the high-performance PLL and is routed through the Integer Q-divider to deliver the best jitter performance. DSPLLP controls the central VCO which provides many of the essential functions for the device such as generating ultra-low phase noise clocks and maintaining free-run accuracy and holdover stability for all PLLs (DSPLLP, DSPLLA, DSPLLB). The phase noise reference for DSPLLP comes from either an integrated XTAL or an external XO. DSPLL locks to a clock input for jitter attenuation. See the SKY63101/02/03 Reference Manual for more information on the configuration modes and CBPro for configuring the modes.

5.7. DSPLLA and DSPLLB with Output Divider NA/NB

In general, both DSPLLA and DSPLLB have identical performance and flexibility and can be independently configured and controlled through the serial interface. Each of the DSPLLs support locked, free-run, and holdover modes of operation. These DSPLLs share the stability from the reference applied to DSPLLP in order to support free-run and holdover modes.

DSPLLA and DSPLLB cannot be routed via the Integer Q divider and instead use N and R dividers to deliver multiple system clocks.

The SKY63101 has one DSPLL (DSPLLP) and two fractional MultiSynth N dividers (NA/NB).

The SKY63102 has two DSPLLs (DSPLLP and DSPLLA) and one fractional MultiSynth N divider (NB).
The NB divider can be connected to either DSPLLP or DSPLLA before being fed to the output R dividers.

The SKY63103 has three DSPLLs (DSPLLP, DSPLLA, and DSPLLB) that are fed directly to the output R dividers.

5.7.1. DCO Mode

The SKY63101/02/03 supports a DCO mode where their output frequencies are adjustable in predefined steps defined by frequency step words (FSW). The frequency adjustments are controlled through the serial interface via the device API or by pin control using frequency increment (FINC) or decrement (FDEC). A FINC will add the frequency step word to the DSPLL output frequency, while a FDEC will decrement it.

5.8. Zero Delay Mode (ZDM)

Zero Delay Mode (ZDM) is a mode of PLL operation in which more accurate input-to-output phase delay can be achieved by providing an external feedback from one of the clock outputs to one of the clock inputs. ZDM is available on each of the three PLLs (DSPLLP, DSPLLA, and DSPLLB). For more details on implementing ZDM, see the "SKY63101/02/03 Reference Manual".

5.9. GPIO Pins General Purpose Input or Output

There are four GPIO pins which have programmable functions. They can be assigned as either an input or an output from one of the functions shown in the table below. OUT6/11 can be repurposed as GPIOs when they are not being used as clock outputs.

The GPI are programmable as either active high or active low via ClockBuilder Pro. Active low GPI are indicated by adding a “b” at the end of the function name for example “OEb” as displayed in ClockBuilder Pro. All GPI pins have a weak pull-up (PU) or pull-down (PD) resistor to set a default state when not externally driven. The default state of the GPI is always deasserted except for OEx, which is asserted by default to enable the outputs. The internal resistance of the PU/PD resistor is 20 kΩ typical.

GPIO selectable status outputs (GPO) are push-pull and do not require any external pull-up or pull-down resistors.

Function	Description
GPIO Selectable Control Inputs (GPI)	
FINC	DCO Frequency Increment.
FDEC	DCO Frequency Decrement.
PLLx_FORCE_HO	Force holdover for DSPLLP, or DSPLL A, or DSPLL B.
PLLx_INSEL[0-2]	Input select pins for DSPLLP, or DSPLL A, or DSPLL B. There are three bits to select from one of six inputs.
IN[0:6]_FAIL	Force input invalid. A low on this pin indicates to the automatic switching state machine that the associated input is not valid for selection. This is useful in applications that use their own input monitoring.
OE0–OE2	Output enable for specific outputs or group of outputs as defined by the grouping assigned in CBPro.
GPIO Selectable Status Outputs (GPO)	
PLLx_LOL	Loss of lock for DSPLLP, DSPLLA, DSPLLB.
INx_LOS	Loss of Signal status indicator for INx.
REF_OOF	Out of Frequency status indicator for the external XO input or the internal XTAL reference to DSPLL P.
INx_OOF	Out of Frequency status indicator for INx.
REF_LOS	Loss of Signal status indicator for the external XO input or the internal XTAL reference to DSPLL P.
PLLx_FORCE_HO	This pin indicates when DSPLLP, DSPLLA, DSPLLB has entered the holdover state.
INTR	Interrupt pin for the device. Programmable Boolean combination of PLLx_LOL, INx_LOS, INx_OOF, PLLx_HO, XO_LOS, XO_OOF.
Serial Interface (I^2C/SPI)	
A1/SDO	A1/SDO of serial interface.
A0/CSb	A0/CSb of serial interface.
SDA/SDIO	SDA/SDIO of serial interface.
SCLK	SCLK of serial interface.

5.10. Device Initialization and Reset

Once power is applied and RSTb is deasserted, the device begins loading preconfigured register values and configuration data from NVM or Flash (depending on grade), and performs other initialization tasks. Communicating with the device through the serial interface is possible once this initialization period is complete (see t_{RDY}). No output clocks will be generated until the initialization is complete, and the device locks to the internal XTAL or external XO reference (see t_{START_XO} and t_{START_XTAL}). A reset, initiated using the RSTb pin or through the Device API RESTART command, restores all registers to the values stored in NVM or Flash, and all circuits, including the serial interface, will be restored to their initial state. All clocks will stop during a hard reset. Other feature-specific resets are also available. See the "SKY63101/02/03 Reference Manual" for more information on different methods of resetting the device.

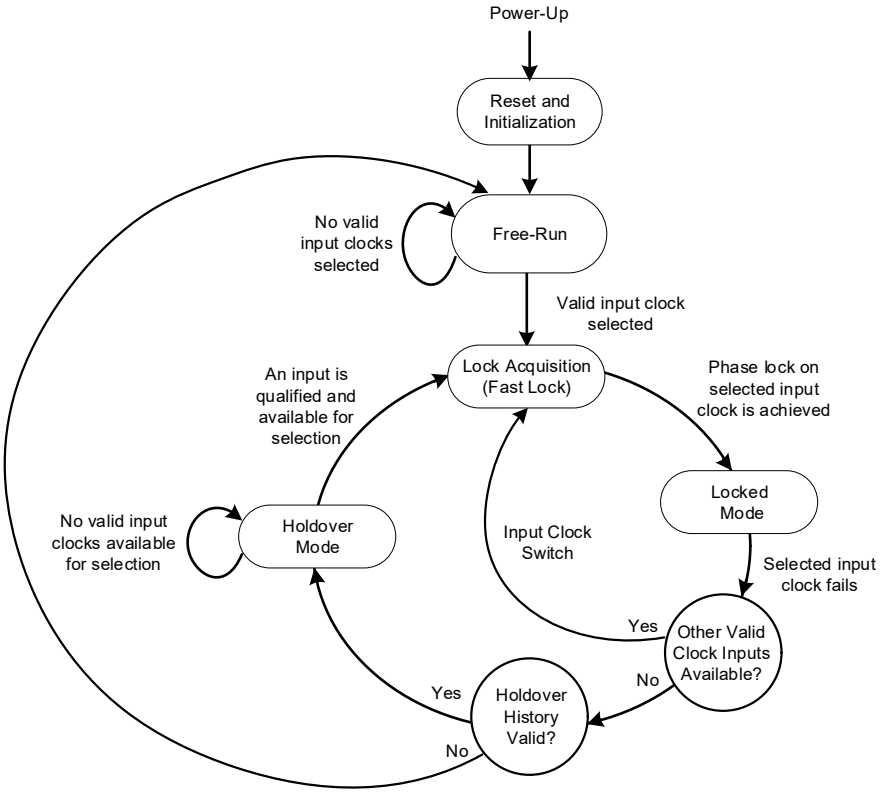


Figure 16. Modes of Operation

5.11. Modes of Operation: DSPLLP, DSPLLA, and DSPLLB

Once initialization is complete, each PLL independently operates in one of four modes: Free-Run, Lock Acquisition, Locked, or Holdover. A state diagram showing the modes of operation is shown in Figure 16 above. The following sections describe each of these modes in greater detail.

5.11.1. Free-Run Mode

The PLLs will automatically enter Free-Run mode once power is applied to the device and initialization is complete. In this mode, the frequency accuracy of the generated output clocks is entirely dependent on the frequency accuracy of the reference clock source. The frequency stability and accuracy of the outputs will be determined by either the internal XTAL or external XO.

For example, if the reference (Internal XTAL or external XO) is operating at –28 ppm, then clock outputs will also be –28 ppm.

5.11.2. Lock Acquisition Mode

Each of the PLLs independently monitors its configured inputs for a valid clock. If at least one valid clock is available for synchronization, a PLL will automatically start the lock acquisition process. If the fast lock feature is enabled, they will acquire lock faster than the PLL Loop Bandwidth would provide and then transition to the normal PLL loop bandwidth. During lock acquisition the outputs will generate a clock that follows the VCO frequency change as it pulls-in to the input clock frequency.

The PLL_STATUS API command reports the lock status of a PLL. When the PLL output frequency is within the threshold defined on the Frequency LOL (FLOL) page in ClockBuilder Pro, the PLL_OUT_OF_FREQUENCY bit deasserts. Some time after that, the PLL will pull in the remaining phase defined on the Phase LOL (PLOL) page in ClockBuilder Pro. Once the PLL is frequency and phase locked, the PLL_LOSS_OF_LOCK (LOL) bit deasserts and the PLL enters locked mode.

5.11.3. Locked Mode

Once locked, the PLL will generate clock outputs that are both frequency and phase locked to their selected input clocks. The PLL loop bandwidths can be independently configured. Any frequency changes (e.g., because of temperature variations) of the reference clock (internal XTAL or external XO) within the PLL loop bandwidth will be corrected by the loop, ensuring 0 ppm lock to its input clock (IN). Any frequency changes of the reference clock beyond the PLL loop bandwidth will pass through to the clock output.

5.11.4. Holdover Mode

Any of the PLLs will automatically enter Holdover mode when the selected input clock becomes invalid, holdover history is valid, and no other valid input clocks are available for selection. Each PLL uses an averaged input clock frequency as its final holdover frequency to minimize the disturbance of the output clock phase and frequency when an input clock suddenly fails. The holdover circuit for each PLL stores historical frequency data while locked to a valid input clock. The final averaged holdover frequency value is calculated from a programmable window within the stored historical frequency data. Both the window size and delay are programmable as shown in Figure 17 on page 40. The window size determines the amount of holdover frequency averaging. The delay value allows ignoring frequency data that may be corrupt just before the input clock failure.

The maximum window size is a function of input frequency and is reported in CBPro for each PLL. Up to 5000 seconds of holdover history can be stored.

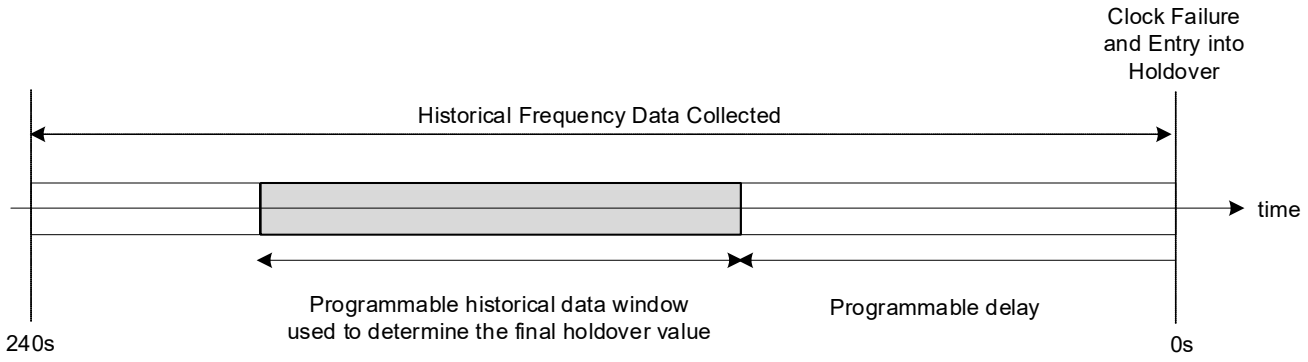


Figure 17. Programmable Holdover Window

When entering holdover, a PLL will pull its output clock frequency to the calculated averaged holdover frequency. While in holdover, the output frequency drift is entirely dependent on the external reference clock connected to the XO_IN input. If the input clock becomes valid, a PLL will automatically exit the holdover mode and re-acquire lock to the new input clock. This process involves pulling the output clock frequency to achieve frequency and phase lock with the input clock. This pull-in process is glitchless.

The PLL output frequency when exiting holdover can be ramped. Just before the exit is initiated, the difference between the current holdover frequency and the new desired frequency is measured. Using the calculated difference and a user-selectable ramp rate, the output is linearly ramped to the new frequency. The PLL loop BW does not limit or affect ramp rate selections (and vice versa). CBPro defaults to ramped exit from holdover and free-run. The ramp rate settings are configurable for initial lock (exit from free-run), exit from holdover, and clock switching.

If ramped holdover exit is disabled, the holdover exit is governed either by (1) the PLL loop BW or (2) the PLL Fastlock bandwidth, when enabled.

5.12. Status and Alarms

The SKY63101/02/03 monitors the input clocks and reference input for status and alarms. These states and alarms provide the internal state machine with real time phase and frequency monitoring used for making decisions, such as switching inputs or entering holdover.

5.12.1. Input Clock Status

All input clocks are continuously monitored for faults using the Loss-of-Signal (LOS), Out-of-Frequency (OOF), and Phase Monitor (PHMON) alarms. When a differential input is configured as a dual CMOS input, then each CMOS input is independently monitored. Any enabled alarms for an input, such as LOS/OOF/PHMON, are logically OR'd together to produce the "Input Invalid" alarm.

Any input clock with an alarm is not valid until all alarms are cleared. If a PLL is locked to an input clock and that input clock becomes invalid, then the PLL may either switch to a valid input or enter holdover mode, depending on how the device is programmed.

API commands can be used to indicate if an alarm is valid, pending short term fault, under validation or invalid.

5.12.1.1. Loss of Signal LOS

The loss of signal alarm measures the period of each input clock cycle to detect phase irregularities or missing clock edges. Each of the input LOS circuits has its own programmable sensitivity, which allows missing edges or intermittent errors to be ignored. Loss of signal sensitivity is configurable using the CBPro utility. The LOS status for each of the monitors is accessible by checking the INPUT_STATUS API.

5.12.1.2. Out of Frequency (OOF) Detection

All inputs are monitored for frequency accuracy with respect to an OOF reference which is selected in ClockBuilder Pro. The OOF reference can be selected as the integrated XTAL or external XO.

The OOF set and clear thresholds must be wider than the combined frequency accuracy of the OOF reference plus the stability of the input clock. A valid input clock frequency is one that remains within the OOF frequency range which is configurable from ±0.1 ppm to ±500 ppm in steps of 0.1 ppm. A configurable amount of hysteresis is also available to prevent the OOF status from toggling at the failure boundary.

An example is shown in the figure below. In this case, the OOF monitor is configured with a valid frequency range of ±15 ppm with 5 ppm of hysteresis.

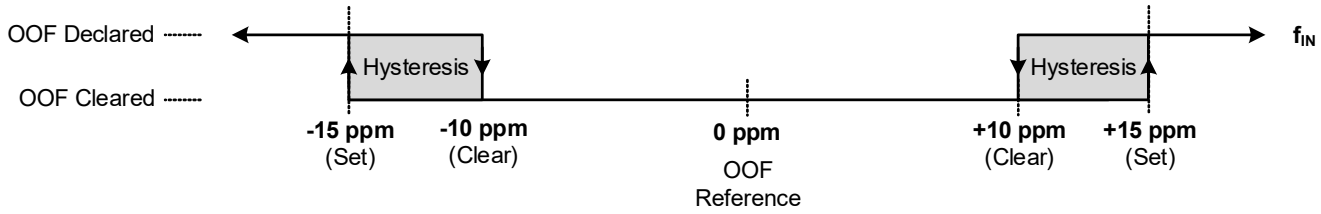


Figure 18. Example of Precise OOF Monitoring Assertion and Deassertion Triggers

5.12.1.3. Phase Monitor (PHMON)

If a clock input undergoes a phase transient, a PLL locked to that input will filter the transient by its loop bandwidth; however, the transient will propagate to the output. Transients that propagate to the output have the potential to negatively impact downstream devices.

Phase Monitor (PHMON) alarm monitors the input clock phase or accumulated phase, and, if the input transient exceeds the programmable threshold, the PHMON alarm will be asserted. PHMON, like the other alarms, is quick to be asserted when the thresholds are violated yet slower to be deasserted to prevent chattering around the threshold.

Each input clock has an independent PHMON alarm. Each alarm can be enabled/disabled individually, and its associated threshold may be independently configured. Note that OOF must be enabled and properly configured for PHMON to operate.

A ZDM input may use the PHMON alarm for monitoring purposes. However, it will have no effect on PLL bandwidth selection and will not cause input switching.

5.12.1.4. Short Term Holdover

The Short-Term Holdover (STHO) feature may be used when the input clock is expected to have a short-term fault and then quickly recover.

If an input clock has STHO enabled, and an LOS/OOF/PHMON alarm is asserted, then a PLL locked to that input will enter holdover and wait for a programmable duration until all alarms on the input clock are deasserted.

If all alarms on the input clock are deasserted before the programmable amount of time has passed, then the PLL will gracefully relock to the same input clock. If all the alarms on the input clock are not deasserted before the programmable amount of time has passed, then the PLL will either switch to the next priority input clock or remain in holdover, depending on the input clock selection settings.

If STHO is disabled, then the PLL will skip the short-term holdover time and immediately switch to the next priority input clock or enter holdover, depending on the input clock selection settings.

STHO may be programmed using Clock Builder Pro to set the duration or to enable or disable the feature for each input clock individually. Note that the STHO setting will affect all PLLs assigned to that input.

5.12.2. PLL Status

DSPLLP, DSPLLA, and DSPLLB are continuously monitored for Loss-of-Lock (LOL). The final LOL status indicator is the logical OR of the Frequency Loss-of-Lock and Phase Loss-of-Lock statuses. See the Reference Manual for more information.

5.12.2.1. Loss of Lock (LOL)

There is a loss of lock (LOL) monitor for each of the PLLs (DSPLLP, DSPLLA, and DSPLLB). The LOL monitor asserts when a PLL has lost synchronization with its selected input clock. Any of the GPIOs can be programmed as a dedicated loss-of-lock pin that reflects the loss-of-lock condition for each of the PLLs. The LOL monitor measures both the frequency and phase difference between the input and feedback clocks of the phase detector.
The frequency monitor gives frequency lock detection (FLOL) while the phase monitor indicates true phase lock PLOL by detecting one or more single slips. Both the phase and frequency LOL monitors have clear and set thresholds and a timer to prevent LOL assertion from toggling or chattering as the DSPLL completes lock acquisition. The cycle slip detector also has configurable sensitivity.

5.12.2.2. Frequency Loss of Lock (FLOL)

The Frequency Loss-of-Lock (FLOL) monitor measures the frequency difference between the input clock and the feedback clock. The upper and lower LOL thresholds are programmable, which dictates when the alarm will be asserted or deasserted. It is recommended to program the clear threshold to be less than the set threshold to allow for hysteresis in the FLOL set/clear behavior. This prevents the FLOL alarm from chattering or causing multiple interrupts. FLOL, like the other alarms, is quick to be asserted when the threshold is violated yet slower to be deasserted. The alarm validates that the frequency difference between the input and feedback clocks has truly settled to within the LOL clear threshold before the FLOL alarm is deasserted. The time required to validate the frequency difference increases as the loop bandwidth of the PLL decreases.

5.12.2.3. Status Bits

There are four Status Bits that serve as four additional Frequency LOL thresholds. The Status Bit is asserted if the frequency difference between the input clock and feedback clock exceeds the programmable STB threshold. The assertion or deassertion of an STB does not contribute to the FLOL or LOL status. Rather, they serve as a way to track the lock acquisition process for DSPLL's with a loop bandwidth of ~20 Hz. The status bits may be read via the API. In the lock acquisition process, the deassertion of a STB does not indicate that the PLL is frequency locked. This is because the frequency may chatter around the STB threshold. On the other hand, the deassertion of FLOL requires the frequency difference to truly settle below the LOL clear threshold.

5.12.2.4. Phase Loss of Lock (PLOL)

The Phase Loss-of-Lock (PLOL) alarm measures the phase difference between the input clock and feedback clock. The PLOL set threshold is programmable so the alarm will assert or deassert depending on phase difference between the input and feedback clocks relative to the threshold setting. It is recommended to set the clear threshold below the set threshold to allow for hysteresis. This prevents the alarm from chattering or causing multiple interrupts. During the lock acquisition process the input clock and feedback clock will likely have a significant frequency mismatch so the PLOL is asserted until FLOL is deasserted. Once FLOL has been deasserted, the two frequencies are stable with respect to each other. Then the feedback clock phase can be pulled in to within the PLOL clear threshold.

5.12.2.5. Cycle Slip Detection

DSPLLP, DSPLLA, and DSPLLB may be monitored for cycle slips. Like the PLOL alarm, cycle slip detection is not enabled until FLOL is deasserted. Additionally, PLOL must be enabled for cycle slip detection to be enabled. Cycle slips both in the positive and negative direction are monitored. The API can be used to read the total count of positive cycle slips, negative cycle slips and the total count or both positive and negative slips.

5.12.3. External Reference Status

If an external XO reference grade is selected, the XO must always be connected to the device. The SKY63101/02/03 will monitor the external reference input for LOS, OOF, LOL. If a fault is detected on the external reference, then the outputs will be disabled. Any external reference faults may be read via the API.

5.12.4. Interrupt Status

The interrupt flag is asserted when any of the status indicators of the device changes state. The interrupt status may be assigned a GPIO pin, or it may be checked using an API command to show which status indicator caused the interrupt to be asserted.

The Interrupt Pin page in CBPro lists all the status indicators that can be programmed to activate the interrupt pin.

The status indicators that are enabled are logically OR'd together so that the assertion of any of these status indicators will cause the interrupt pin to assert. The interrupt pin status depends on the sticky versions of the individual status indicators, so the interrupt pin will stay asserted until the sticky status indicators are cleared.

5.13. Serial Interface

Configuration and operation of the SKY63101/02/03 is controlled by reading and writing API commands using the I^2C or SPI interface. The SPI mode operates in either four-wire or three- wire modes. The following table defines the GPIO pins assigned to the SPI port. For more information, see the "SKY63101/02/03 Reference Manual".

Table 18. Serial Interface Pins

Pin Number	3-Wire SPI	4-Wire SPI	I^2C
29	CSb	CSb	A0
30	SDIO	SDI	SDA
31	SCLK	SCLK	SCK
32	Unused	SDO	A1

5.14. NVM/Flash Programming and Startup

At power-up, the device downloads its boot-up configuration and settings from either internal non-volatile memory (NVM) or internal Flash memory depending on the selected device grade. The device can be ordered as a blank part with no configuration, or a boot-up configuration can be preprogrammed at the factory with a custom frequency plan such that the device starts generating clocks on its first power-up.

For devices with non-volatile memory (NVM), the boot-up configuration is stored in the NVM. At power-up, the device downloads its default configuration and settings from internal NVM. The NVM can be preprogrammed at the factory with a custom frequency plan such that the device starts generating clocks on its first power-up, or the NVM can be programmed in the field (up to eight times) using the API command set. NVM programming must be done with VDDA set to 3.3 V. For more details on NVM programming, see the "SKY63101/02/03 Reference Manual".

For devices with internal Flash memory, the boot-up configuration can be reprogrammed as many times as necessary. During re-programming of the Flash memory, the device maintains the existing frequency configuration and continues generating clocks. After the flash has been reprogrammed, on the next power-on reset cycle, the device will download the new boot-up configuration.

5.15. Application Programming Interface (API)

Communication between the customer's host processor and the SKY63101/02/03 internal microcontroller (MCU) is accomplished through the serial interface. The SKY63101/02/03 MCU contains API firmware that allows users simple command level access to the device's registers. For more details on the Device API and for instructions on programming the clock device, see the "SKY63101/02/03 Reference Manual".

5.16. Power Supplies

The SKY63101/02/03 has 13 power supply pins. The separate power supplies are used for different functions, providing power locally where it is needed on the die to improve isolation. When no outputs are enabled for a particular VDDOx, that supply pin may be left unconnected. Please refer to the "SKY63101/02/03 Reference Manual" for more details on power management and filtering recommendations.

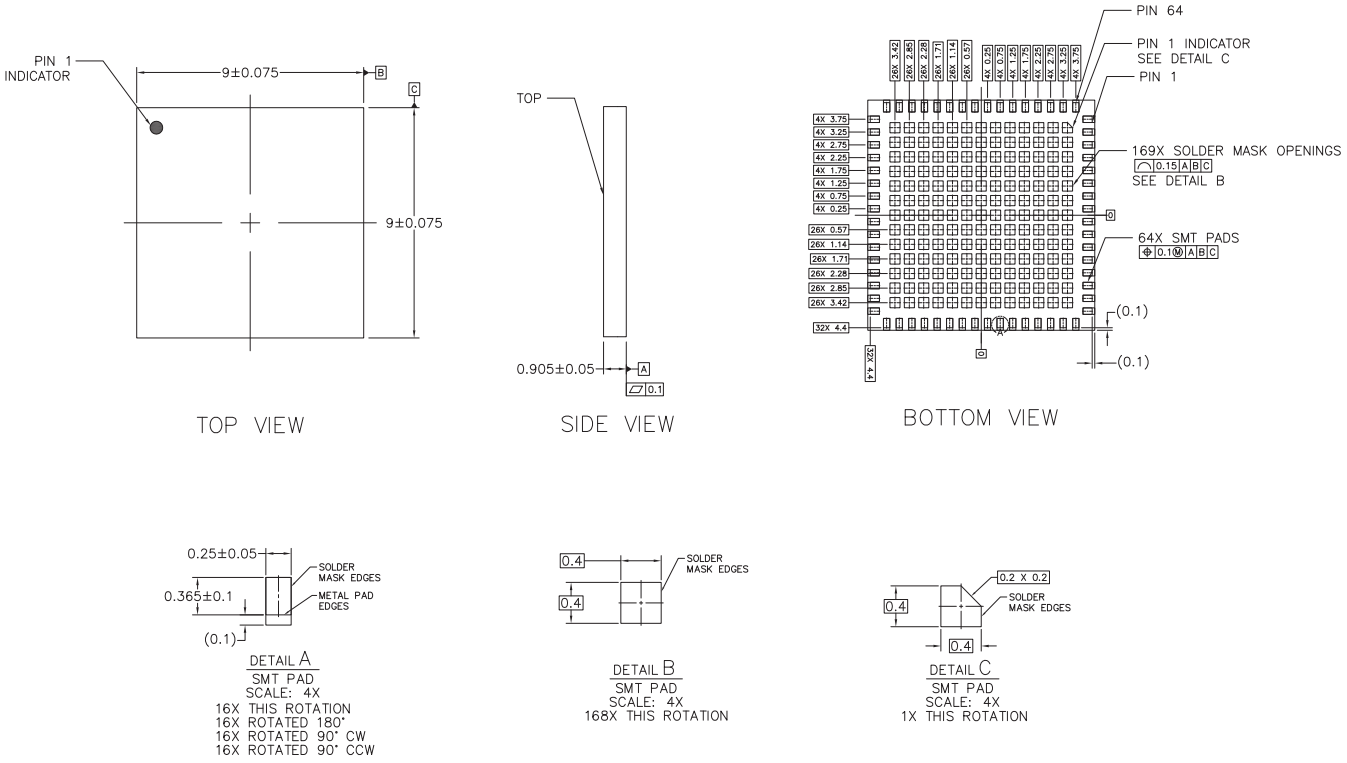
5.16.1. Power Supply Sequencing

There are no power sequencing requirements between supplies. VDDA, VDDIN, and VDD18 should be powered up before releasing RSTb.

5.16.2. Power Supply Ramp Rate

Power supply ramp times must stay within the maximum supply voltage ramp rate as defined in Table 8, "DC Characteristics," on page 15.

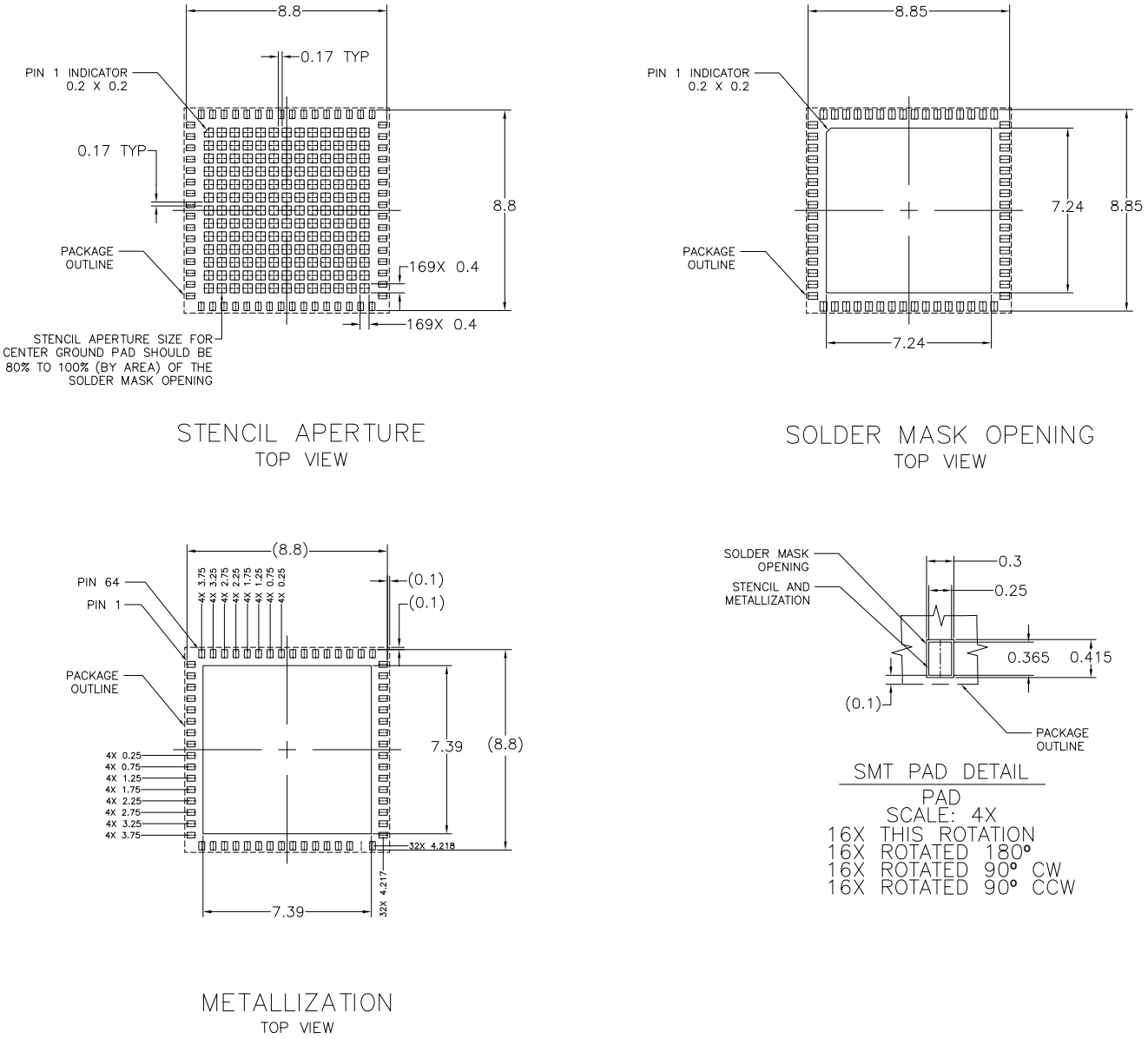
6. Package Outline



NOTES: UNLESS OTHERWISE SPECIFIED.
1. DIMENSIONING AND TOLERANCING IN ACCORDANCE WITH ASME Y14.5M–1994.
2. DIMENSIONS ARE IN MILLIMETERS
3. PAD DEFINITIONS PER DETAILS ON DRAWING.

Figure 19. 64-LGA Package Diagram

7. PCB Land Pattern



NOTES:
1. DIMENSIONS ARE IN MILLIMETERS, UNLESS OTHERWISE SPECIFIED.
2. THERMAL VIAS SHOULD BE RESIN FILLED AND CAPPED IN ACCORDANCE WITH IPC–4761 TYPE VII VIAS. 30–35UM Cu THICKNESS IS RECOMMENDED.

Figure 20. PCB Land Pattern

8. Top Marking

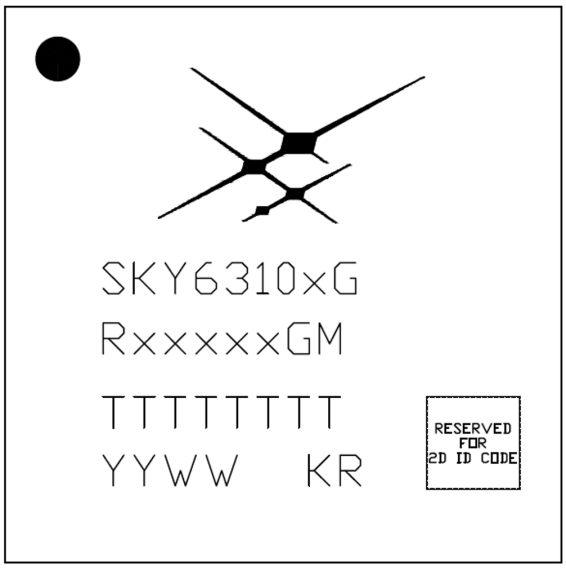


Figure 21. SKY63101/02/03 Top Marking

Table 19. Top Marking Explanation

Line	Characters	Description
1	Circle w/ 0.6 mm (64-LGA) diameter	Pin 1 indicator; left-justified
	SKY6310xG	Base part number and Device Grade: G = Device Grade. (Refer to 9. Ordering Guide for latest device grade information).
2	RxxxxxGM	R = Product revision. (Refer to 9. Ordering Guide for latest revision). xxxxx = Customer specific sequence number. Optional boot-configuration code as- signed for custom, factory preprogrammed devices. Characters are not included for standard, factory default configured devices. See 9. Ordering Guide for more information. GM = Package (LGA) and temperature range (–40 to +95 °C)
3	TTTTTTTT	TTTTTTTT = Manufacturing trace code.
4	YYWW	YYWW = Characters correspond to the year (YY) and work week (WW) of package assembly.
	KR	KR = Korea; Country of Origin (ISO Abbreviation)

9. Ordering Guide

Table 20. SKY63101 Ordering Guide

Ordering Part Number (OPN)[1]	DSPLLs	MultiSynths	Maximum Output Frequency	Internal Memory Flash/NVM	Internal Reference	Package
SKY63101A-A-GM/R	1	2	3.2 GHz	Flash	Yes	64-Lead LGA 9x9 mm
SKY63101AAxxxxxGM/R	1	2	3.2 GHz	Flash	Yes	64-Lead LGA 9x9 mm
SKY63101BAxxxxxGM/R	1	1	3.2 GHz	Flash	Yes	64-Lead LGA 9x9 mm
SKY63101CAxxxxxGM/R	1	0	3.2 GHz	Flash	Yes	64-Lead LGA 9x9 mm
SKY63101D-A-GM/R	1	2	3.2 GHz	NVM	Yes	64-Lead LGA 9x9 mm
SKY63101DAxxxxxGM/R	1	2	3.2 GHz	NVM	Yes	64-Lead LGA 9x9 mm
SKY63101EAxxxxxGM/R	1	1	3.2 GHz	NVM	Yes	64-Lead LGA 9x9 mm
SKY63101FAxxxxxGM/R	1	0	3.2 GHz	NVM	Yes	64-Lead LGA 9x9 mm
SKY63101P-A-GM/R	1	2	3.2 GHz	Flash	No	64-Lead LGA 9x9 mm
SKY63101PAxxxxxGM/R	1	2	3.2 GHz	Flash	No	64-Lead LGA 9x9 mm
SKY63101QAxxxxxGM/R	1	1	3.2 GHz	Flash	No	64-Lead LGA 9x9 mm
SKY63101RAxxxxxGM/R	1	0	3.2 GHz	Flash	No	64-Lead LGA 9x9 mm
SKY63101S-A-GM/R	1	2	3.2 GHz	NVM	No	64-Lead LGA 9x9 mm
SKY63101SAxxxxxGM/R	1	2	3.2 GHz	NVM	No	64-Lead LGA 9x9 mm
SKY63101TAxxxxxGM/R	1	1	3.2 GHz	NVM	No	64-Lead LGA 9x9 mm
SKY63101UAxxxxxGM/R	1	0	3.2 GHz	NVM	No	64-Lead LGA 9x9 mm
SKY63101AA-EVB[2]	—	—	3.2 GHz	Flash	Yes	Evaluation board

1. The blank parts, SKY63101AA-A-GM and SKY63101PA-A-GM, are configured to be a 4-Wire interface. For Factory programmed plans and blank parts requiring other interface standards like I^2C and 3-Wire, custom part numbers (Axxxxx) are created using CBPro.
2. The SKY63101AA-EVB is supported by the Saturn evaluation platform. See the Saturn evaluation platform user guide for more information.

Table 21. SKY63102 Ordering Guide

Ordering Part Number (OPN)[1]	DSPLLs	Multisynths	Maximum Output Frequency	Internal Memory Flash/ NVM	Internal Reference	Package
SKY63102A-A-GM/R	2	1	3.2 GHz	Flash	Yes	64-Lead LGA 9x9 mm
SKY63102AAxxxxxGM/R	2	1	3.2 GHz	Flash	Yes	64-Lead LGA 9x9 mm
SKY63102BAxxxxxGM/R	2	0	3.2 GHz	Flash	Yes	64-Lead LGA 9x9 mm
SKY63102D-A-GM/R	2	1	3.2 GHz	NVM	Yes	64-Lead LGA 9x9 mm
SKY63102DAxxxxxGM/R	2	1	3.2 GHz	NVM	Yes	64-Lead LGA 9x9 mm
SKY63102EAxxxxxGM/R	2	0	3.2 GHz	NVM	Yes	64-Lead LGA 9x9 mm
SKY63102P-A-GM	2	1	3.2 GHz	Flash	No	64-Lead LGA 9x9 mm
SKY63102PAxxxxxGM/R	2	1	3.2 GHz	Flash	No	64-Lead LGA 9x9 mm
SKY63102QAxxxxxGM/R	2	0	3.2 GHz	Flash	No	64-Lead LGA 9x9 mm
SKY63102S-A-GM	2	1	3.2 GHz	NVM	No	64-Lead LGA 9x9 mm
SKY63102SAxxxxxGM/R	2	1	3.2 GHz	NVM	No	64-Lead LGA 9x9 mm
SKY63102TAxxxxxGM/R	2	0	3.2 GHz	NVM	No	64-Lead LGA 9x9 mm
SKY63102AA-EVB[2]	—	—	3.2 GHz	Flash	Yes	Evaluation board

1. The blank parts, SKY63102AA-A-GM and SKY63102PA-A-GM, are preconfigured to be a 4-Wire interface. For Factory programmed plans and blank parts requiring other interface standards like I^2C and 3-Wire, custom part numbers (Axxxxx) are created using CBPro.
2. The SKY63102AA-EVB is supported by the Saturn evaluation platform. See the Saturn evaluation platform user guide for more information.

Table 22. SKY63103 Ordering Guide

Ordering Part Number (OPN)[1]	DSPLLs	Multisynths	Maximum Output Frequency	Internal Memory Flash/ NVM	Internal Reference	Package
SKY63103A-A-GM/R	3	0	3.2 GHz	Flash	Yes	64-Lead LGA 9x9 mm
SKY63103AAxxxxxGM/R	3	0	3.2 GHz	Flash	Yes	64-Lead LGA 9x9 mm
SKY63103D-A-GM/R	3	0	3.2 GHz	NVM	Yes	64-Lead LGA 9x9 mm
SKY63103DAxxxxxGM/R	3	0	3.2 GHz	NVM	Yes	64-Lead LGA 9x9 mm
SKY63103P-A-GM/R	3	0	3.2 GHz	Flash	No	64-Lead LGA 9x9 mm
SKY63103PAxxxxxGM/R	3	0	3.2 GHz	Flash	No	64-Lead LGA 9x9 mm
SKY63103S-A-GM/R	3	0	3.2 GHz	NVM	No	64-Lead LGA 9x9 mm
SKY63103SAxxxxxGM/R	3	0	3.2 GHz	NVM	No	64-Lead LGA 9x9 mm
SKY63103AA-EVB[2]	—	—	3.2 GHz	Flash	Yes	Evaluation board

1. The blank parts, SKY63103AA-A-GM and SKY63103PA-A-GM, are preconfigured to be a 4-Wire interface. For Factory programmed plans and blank parts requiring other interface standards like I^2C and 3-Wire, custom part numbers (Axxxxx) are created using CBPro.
2. The SKY63103AA-EVB is supported by the Saturn evaluation platform. See the Saturn evaluation platform user guide for more information.

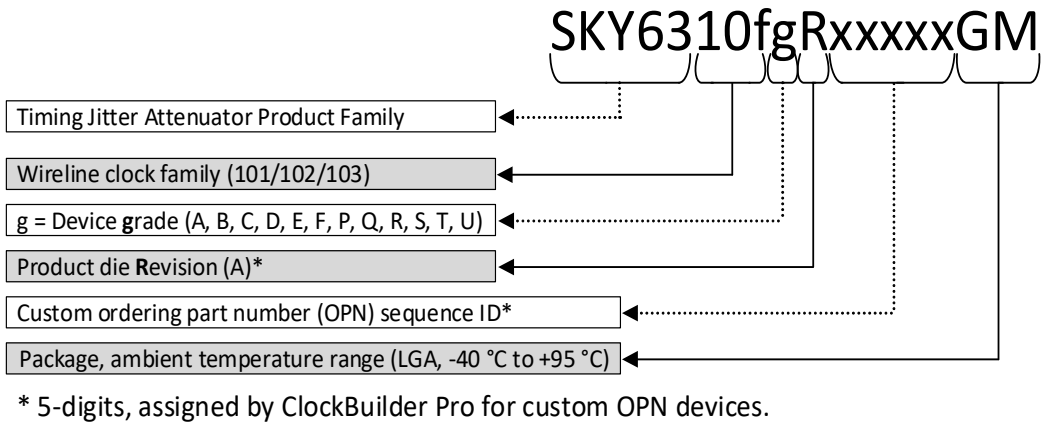


Figure 22. Ordering Guide

10. Revision History

Revision	Date	Description
D	November, 2025	• Updated Table 3. Thermal Conditions. • Clarified specs in Table 9. Internal Reference Specifications.
C	October, 2025	• Added “Gapped clock input support” and “PCI-Express Gen 1 through Gen 7 compliant outputs” to 1. Features List. • Added 5.4.4. Gapped Input Clocks. • Updated 5.5.3. Output Enable Disable. • Added 5.5.7. PCIe Outputs. • Updated 5.6. DSPLLP with Output Q-Divider (High Performance Path) • Updated 5.7.1. DCO Mode. • Corrected SPI pins in Table 18. Serial Interface Pins. • Corrected minor typos.
B	September, 2025	• Updated Electrical specifications tables with latest characterization data. • PCI specs updated to include spread spectrum (Table 6 and 7). • Updated package diagram side view dimension. • Table 1 updated description to reflect GPIO pins as inputs and outputs. - OUT6b/GPIO4 - OUT6/GPIO5 - OUT11b/GPIO6 - OUT11/GPIO7
A	March, 2025	Initial release.