DATA SHEET

SKY62101 12-Output, Any-Frequency, Any-Output Clock Generator with Ultra-Low Jitter

The SKY62101 clock generator combines Fifth-generation DSPLL® and MultiSynth™ technologies with an ultra-low jitter VCO to deliver ultra-low jitter (<55 fs) in PCIe Gen 1/2/3/4/5/6/7 compliant high-performance applications. The device is used in applications like 112G/224G SerDes, coherent optics, and data center equipment that demand the highest level of integration and jitter performance. All PLL components are integrated on-chip, eliminating the risk of noise coupling associated with discrete solutions.

The SKY62101 supports free-run and synchronous operation by locking to an external crystal or oscillator. The SKY62101 is quickly and easily configured using Skyworks ClockBuilder® Pro (CBPro) software. ClockBuilder Pro assigns a custom part number for each unique configuration.

Devices ordered with custom part numbers are factory-programmed, making it easy to get a custom clock configuration uniquely tailored for each application. Custom part numbers that are factory-programmed will power up with a known frequency configuration. The device may also be user-configured at power-up or internally configured in non-volatile memory (NVM) using the CBPro Field Programmer via the serial interface. For more information, visit the Skyworks Sales Information page.

Applications

- 56G/112G/224G PAM4 serializer/deserializer (SerDes) clocking
- OTN muxponders and transponders
- 100/200/400/600/800G networking line cards
- Synchronous Ethernet
- Data center switches
- 100G/200G/400G optical transceivers
- Medical imaging
- Test and measurement

Key Features

- Utilizes Fifth-generation DSPLL and MultiSynth technologies:
  - One DSPLL, two MultiSynth
- Frequencies up to 3.2 GHz
- Ultra-low phase jitter:
  - <55 fs RMS typ (integer mode)
  - 100 fs RMS typ (fractional mode)
- PCIe Gen 1/2/3/4/5/6/7 compliant
- 12 outputs
- Output frequency range:
  - Differential: 8 kHz to 3.2 GHz
  - LVCMOS: 8 kHz to 250 MHz
- Fixed or user-adjustable output formats
- Programmable delay at each output
- External flash or internal NVM options
- Simplified API interface
- Pin-compatible with SKY63104/05/06 jitter attenuators and SKY63001/69003/69102 IEEE 1588 PTP network synchronizers
- 56-QFN, 8 x 8 mm
- ClockBuilder Pro Configuration Software
- For RoHS and other product compliance information, see the Skyworks Certificate of Conformance.

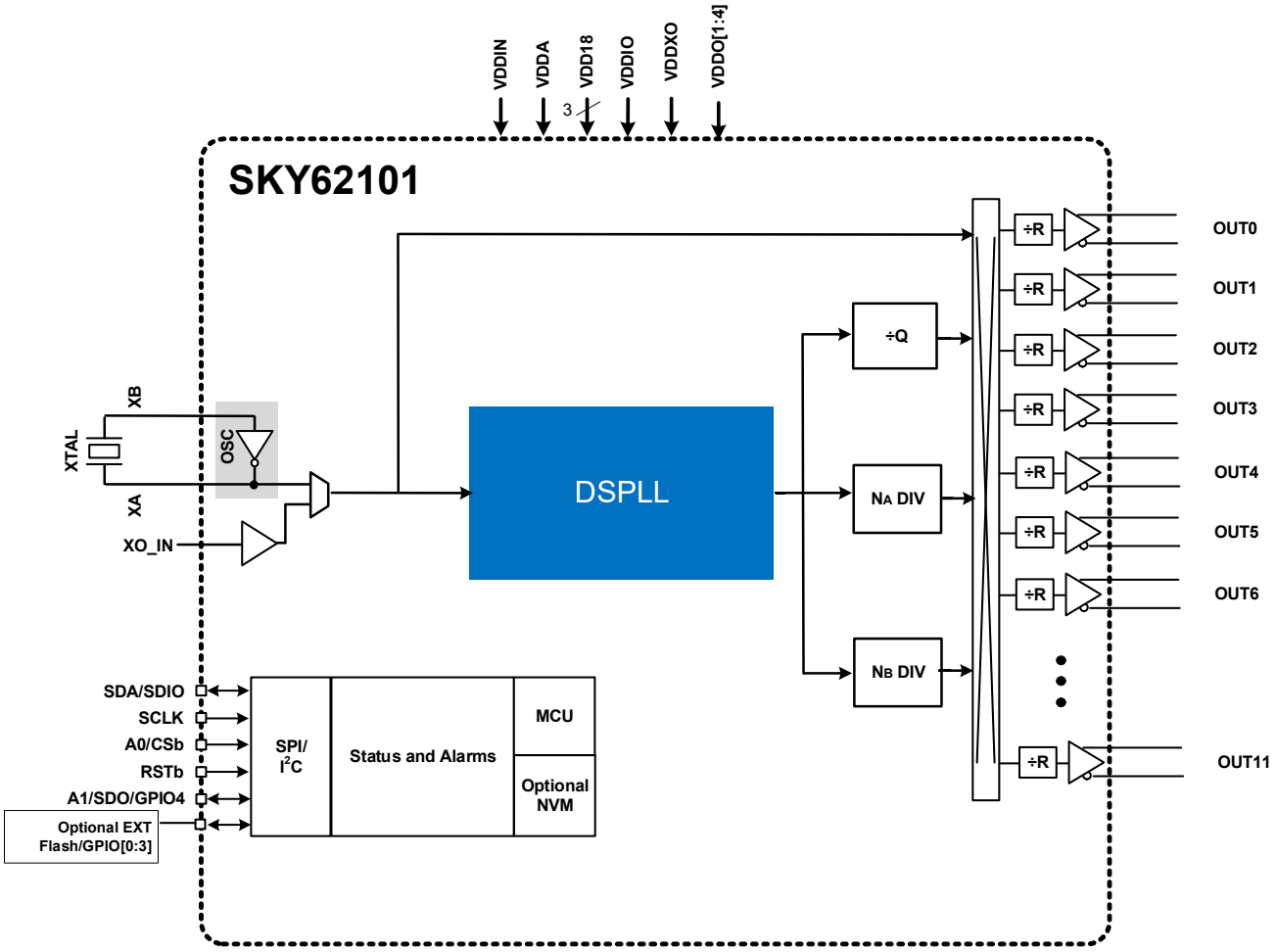


Figure 1. Functional Block Diagram

1. Features List

Specifications on this page are for reference only. Refer to 3. "Electrical and Mechanical Specifications" for device performance.

- Generates any output frequency in any format
- Ultra-low jitter performance
  - <55 fs RMS typ. in integer mode
  - 100 fs RMS typ. in fractional mode
- External crystal: 48 MHz to 61.44 MHz
- Up to 12 programmable clock outputs
- Integer divider
  - Differential: 8 kHz to 3.2 GHz
  - CMOS: 8 kHz to 250 MHz
- Fractional divider
  - Differential: 8 kHz to 650 MHz
  - CMOS: 8 kHz to 250 MHz
- Highly configurable outputs:
  - Fixed formats LVDS, S-LVDS, LVPECL, LVCMOS, CML, and HCSL
  - User-programmable signal amplitude
  - Configurable GPIO pins
- PCIe Gen 1/2/3/4/5/6/7 compliant
- PCIe spread spectrum support
  - Programmable down and center spread spectrum
- Glitchless on-the-fly output frequency changes
- DCO Mode: as low as 0.001 ppb steps
- Core voltage: 3.3 V, 1.8 V
- Output supply pins: 3.3 V, 2.5 V, 1.8 V
- Serial Interface: I^2C or SPI (3- or 4-wire)
- ClockBuilder Pro software tool simplifies device configuration
- External Flash support
- Package: 56-lead QFN, 8x8 mm
- Extended temperature range
  - –40 to +95 °C ambient
  - –40 to +105 °C board
- Pb-free, RoHS compliant

2. Pin Descriptions

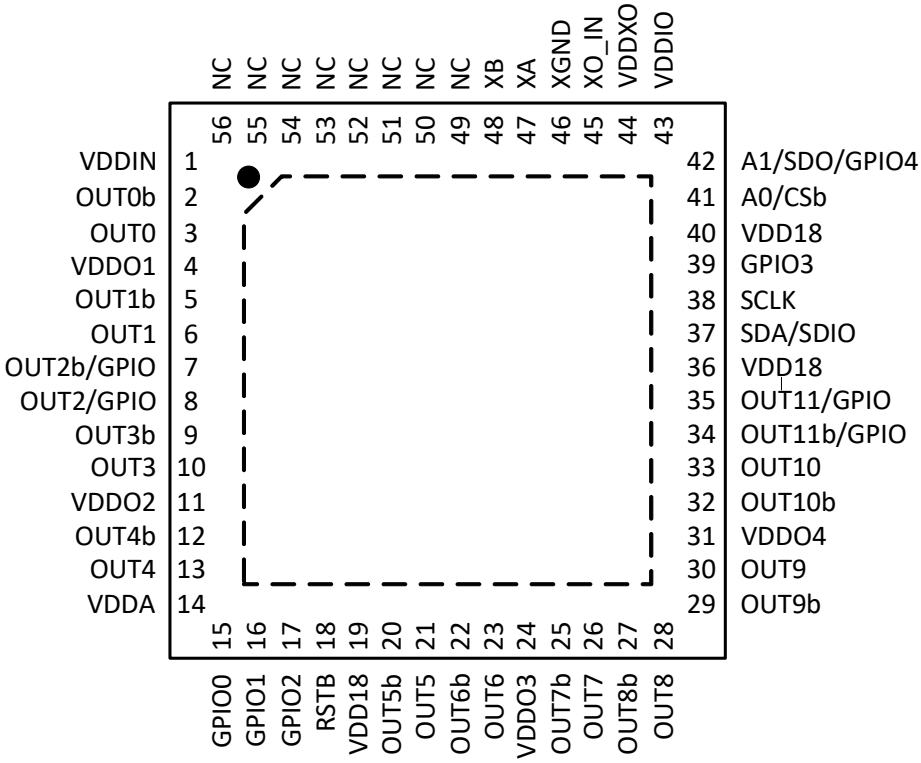


Figure 2. Pinout Top View

Table 1. Pin Descriptions

Pin Name	Pin Number	Pin Type[1]	Function
Inputs			
XO_IN	45	I	**Input for low phase noise (XO)**
XGND	46	I	**XTAL Shield** Connect this pin directly to the XTAL and capacitor ground pins. Do not ground the XV pin. XV should be isolated from the PCB ground plane. Refer to the "Fifth Generation DSPLL Clock Generator Reference Manual" for layout guidelines.
XA	47	I	**Crystal Input** Input pins for external crystal (XTAL). XA and XB pins can be left unconnected when not in use.
XB	48		

Table 1. Pin Descriptions (Continued)

Pin Name	Pin Number	Pin Type[1]	Function
NC	49	NC	**No Connect** Leave these pins floating.
NC	50		
NC	51		
NC	52		
NC	53		
NC	54		
NC	55		
NC	56		
Outputs			
OUT0b	2	O	**Output Clocks** The output clocks can be programmed as single-ended CMOS or differential LVDS, S-LVDS, CML, HCSL or ac-coupled LVPECL and support a programmable signal amplitude and common-mode voltage. Desired output signal format is configurable in CBPro. Termination recommendations are provided in the "Fifth Generation DSPLL Clock Generator Reference Manual". Unused outputs should be left unconnected.
OUT0	3		
OUT1b	5		
OUT1	6		
OUT2b/GPIO	7	I or O	**Output Clocks with General-Purpose Input or Output Option** Output 2 can alternatively be assigned as two General-Purpose Inputs or Outputs (GPIO0, GPIO1) that can be programmed to have any of the input or output control functions listed in "5.6. GPIO Pins General Purpose Input or Output" on page 29. Regardless of whether Output 2 is functioning as a clock output or GPIO, the power supply will be VDDO1.
OUT2/GPIO	8		
OUT3b	9	O	**Output Clocks** The output clocks can be programmed as single-ended CMOS or differential LVDS, S-LVDS, CML, HCSL, or ac-coupled LVPECL and support a programmable signal amplitude and common-mode voltage. The desired output signal format is configurable in CBPro. Termination recommendations are provided in the "Fifth Generation DSPLL Clock Generator Reference Manual". Unused outputs should be left unconnected.
OUT3	10		
OUT4b	12		
OUT4	13		
OUT5b	20		
OUT5	21		
OUT6b	22		
OUT6	23		
OUT7b	25		
OUT7	26		
OUT8b	27		
OUT8	28		
OUT9b	29		
OUT9	30		
OUT10b	32		
OUT10	33		
OUT11b/GPIO	34	I or O	**Output Clocks with General-Purpose Input or Output Option** Output 11 can alternatively be assigned as two General Purpose Inputs or Outputs (GPIO2, GPIO3) that can be programmed to have any of the input or output control functions listed in "5.6. GPIO Pins General Purpose Input or Output" on page 29. Regardless of whether Output 11 is functioning as a clock output or GPIO, the power supply will be VDDO4.
OUT11/GPIO	35		

Table 1. Pin Descriptions (Continued)

Pin Name	Pin Number	Pin Type[1]	Function
Serial Interface			
SDA/SDIO	37	I/O	**Serial Data Interface** This is the bidirectional data pin (SDA) for the I^2C mode, or the bidirectional data pin (SDIO) in the 3-wire SPI mode, or the input data pin (SDI) in the 4-wire SPI mode. When in I^2C mode, this pin must be pulled-up using an external resistor of at least 1 kΩ. No pull-up resistor is needed when in SPI mode.
SCLK	38	I	**Serial Clock Input Interface** This is the bidirectional I^2C clock pin. Clock stretching (i.e., driving SCL low to insert wait-states) will be utilized when operating at rates greater than 100 kHz. This pin must be pulled up to V_{DDIO} using an external resistor of at least 1 kΩ.
A0/CSb	41	I	**Address Select 0/Chip Select** This pin functions as the hardware-controlled LSB of the device address (A0) in I^2C mode. In SPI mode, this pin functions as the chip select input (active low). This pin is internally pulled up and can be left floating if unused.
A1/SDO/GPIO4	42	O	**Address Select 1/Serial Data Output/GPIO4** This input pin operates as the hardware-controlled next to LSB portion of the device address (A1) in I^2C mode. In 4-wire SPI mode, this pin operates as the Serial Data Output (SDO). In 3-wire SPI mode, this pin can function as an additional GPIO pin (GPIO4).
Control/Status			
GPIO0	15	I or O	**Programmable General Purpose Input or Outputs** These pins can be programmed to the functions defined in "5.6. GPIO Pins General Purpose Input or Output" on page 29. See the "Fifth Generation DSPLL Clock Generator Reference Manual" for more details.
GPIO1	16		
GPIO2	17		
GPIO3	39		
RSTb	18	I	**Device Reset** This pin functions as an active-low reset input and is used to generate a device reset when held low for at least the specified minimum pulse width. This resets the device back to a known state and reloads the NVM frequency plan and application. All clocks will stop while the RSTb pin is asserted. If there is no frequency plan in NVM, the reset pin will return the device to the bootloader state in which it is waiting for the frequency plan and application to be downloaded by the host controller. This pin accepts a CMOS input and is internally pulled up with a ~20 kΩ resistor to VDDIO. VDDA and VDD18 must be powered up and stable before releasing RSTb. RSTb must not be toggled faster than the maximum update rate (f_{UR}) specification. For more details on RSTb pin circuitry, refer to the "Fifth Generation DSPLL Clock Generator Reference Manual".
Power			
VDDIN	1	P	**Input Clock Supply Voltage** Supply voltage 3.3 V, 2.5 V or 1.8 V for the input clock buffers.
VDDO1	4	P	**Output Clock Supply VDDO1 to VDDO4** Supply voltage 3.3 V, 2.5 V, or 1.8 V for outputs. Leave VDDO pins of unused output drivers unconnected. An alternate option is to connect the VDDO pin to a power supply and disable the output driver to minimize current consumption. A 0402 1 µF capacitor should be placed very near each of these pins. VDDO may not exceed VDDA. The banks of outputs are powered as follows: VDDO1 – OUT[0:2] VDDO2 – OUT[3:4] VDDO3 – OUT[5:8] VDDO4 – OUT[9:11] Data sheet jitter performance requires all outputs in a given bank to operate at a single frequency.
VDDO2	11		
VDDO3	24		
VDDO4	31		

Table 1. Pin Descriptions (Continued)

Pin Name	Pin Number	Pin Type[1]	Function
VDDA	14	P	**Core Analog Supply Voltage** This core supply can operate from a 3.3 V or 1.8 V power supply for low-power mode. Note that all other supply voltages must be equal or lower voltage than the VDDA pin, so in low-power mode, no other supply can exceed 1.8 V. See the "Fifth Generation DSPLL Clock Generator Reference Manual" for power supply filtering recommendations. A 0402 1 µF capacitor should be placed very near each of these pins.
VDD18	19	P	**Core Supply Voltage 1.8 V** The device core operates from a 1.8 V supply. See the "Fifth Generation DSPLL Clock Generator Reference Manual" for power supply filtering recommendations. A 0402 1 µF capacitor should be placed very near each of these pins.
VDD18	36		
VDD18	40		
VDDIO	43	P	**Control, Status IO Clock Supply Voltage** Supply voltage 3.3 V, 2.5 V, or 1.8 V for the serial interface, control, and status inputs and outputs.
VDDXO	44	P	**Reference Supply Voltage** Supply voltage of 3.3 V or 1.8 V supported for the reference. For best performance, VDDXO should be the same voltage as the VDD_XO.
GND PAD	Package Bottom	P	**Exposed Die Attach Pad** The exposed die attach pad (ePAD) on the bottom of the package must be connected to electrical ground.

1. I = Input, O = Output, P = Power, NC = No Connect.

3. Electrical and Mechanical Specifications

All minimum and maximum specifications are assured and apply across the recommended operating conditions. Typical values apply at nominal supply voltages and an operating temperature of 25 °C unless otherwise noted.

Table 2. Absolute Maximum Ratings[1,2,3]

Parameter	Symbol	Test Condition	Value	Unit
DC supply voltage	V_{DDIN}		–0.5 to 3.8	V
	V_{DDXO}		–0.5 to 3.8	V
	V_{DD18}	<10 s	–0.5 to 2.4	V
	V_{DDA}	<10 s	–0.5 to 3.8	V
	V_{DDO}	<10 s	–0.5 to 3.8	V
	V_{DDIO}	<10 s	–0.5 to 3.8	V
Input voltage range	V_{I1}	XO_IN/XO_INb	–0.85 to 3.8	V
	V_{I2}	GPIO0-3, RSTb, SCLK, SDA/SDIO, A0/CSb	–0.5 to 3.8	V
	V_{I3}	XA/XB	–0.5 to 2.7	V
Latch-up tolerance	LU		JESD78 compliant	
ESD tolerance	HBM	100 pF, 1.5 kΩ	2.0	kV
Storage range	TSTG		–55 to 150	°C
Maximum junction temperature in operation	T_{JCT}		125	°C
Soldering temperature (Pb-free profile)[4]	T_{PEAK}		235 to 245	°C
Soldering time at T_{PEAK} (Pb-free profile)[4]	T_P		30 to 40	s

1. Permanent device damage may occur if the absolute maximum ratings are exceeded. Functional operation should be restricted to the conditions as specified in the operational sections of this data sheet. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.
2. RoHS-6 compliant.
3. For more packaging information, visit the Skyworks environmental compliance page.
4. The device is compliant with JEDEC J-STD-020.

ESD Handling: Industry-standard ESD handling precautions must be adhered to at all times to avoid damage to this device.

Table 3. Thermal Conditions

Parameter	Symbol	Test Condition	Typical Value		Unit
			JEDEC[1]	CEVB[2]	
Thermal resistance, junction-to-ambient	θ_{JA}	Still air	23.27	9.89	°C/W
		1 m/s	19.44	8.60	°C/W
		2 m/s	18.65	8.52	°C/W
Thermal resistance, junction-to-board	Ψ_{JB}[3]	Still air	10.21	3.85	°C/W
Thermal resistance, junction-to-top-center	Ψ_{JC}	Still air	0.4	0.6	°C/W

1. Based on PCB dimension: 4" x 4.5", PCB thickness: 1.6 mm, number of Cu Layers: 2.
2. Customer EVB: eight-layer board, board dimensions: ~9”x 9”, all eight layers are copper-poured.
3. Ψ_{JB} can be used to calculate the junction temperature based on the board temperature and power dissipation for a given frequency plan, $T_j = T_{PCB} + \Psi_{JB} \times P_D$. T_{PCB} should be measured as close to the SKY62101 DUT as possible since temperature may vary across the PCB.

Table 4. Recommended Operating Conditions

V_{DD18} = 1.8 V ±5%, $V_{DDXO} = V_{DDA}$ = 3.3 V ±5%, All other supplies programmable 3.3 V ±5%, 2.5 V ±5%, 1.8 V ±5%, T_A = –40 to 95 °C.
Low Power Mode: $V_{DD18} = V_{DDIN} = V_{DDIO} = V_{DDXO} = V_{DDA} = V_{DDO}$ = 1.8 V ±5%, T_A = –40 to 95 °C.

Parameter	Symbol	Test Condition	Min	Typ	Max	Unit
Ambient temperature	T_A		–40	25	95	°C
Board temperature	T_B		–40	65	105	°C
Junction temperature	TJ_{MAX}[1]		—	—	125	°C
Core supply voltage	V_{DD18}		1.71	1.80	1.89	V
	V_{DDA}[2]		3.14	3.30	3.47	V
		Low-power mode	1.71	1.80	1.89	V
	V_{DDXO}		3.14	3.30	V_{DDA}[2]	V
		Low-power mode	1.71	1.80	1.89	V
Input supply voltage	V_{DDIN}		3.14	3.30	V_{DDA}[2]	V
			2.38	2.50	2.62	V
			1.71	1.80	1.89	V
GPIO supply voltage	V_{DDIO}		3.14	3.30	V_{DDA}[2]	V
			2.38	2.50	2.62	V
			1.71	1.80	1.89	V
Clock output driver supply voltage	V_{DDO}		3.14	3.30	V_{DDA}[2]	V
			2.38	2.50	2.62	V
			1.71	1.80	1.89	V

1. Ambient temperature of 95 °C may not be possible with all configurations. This is dependent on device configuration. T_j cannot exceed a max of 125 °C.
2. VDDA must be greater than or equal to the highest voltage applied to the device. In Low-Power Mode, all voltage supplies must be set to 1.8 V.

Table 5. Performance Characteristics

V_{DD18} = 1.8 V ±5%, V_{DDA} = V_{DDXO} = 3.3 V ±5%; All other supplies programmable 3.3 V ±5%, 2.5 V ±5%, 1.8 V ±5%, T_A = –40 to 95 °C.
Low-Power Mode: V_{DD18} = V_{DDIN} = V_{DDIO} = V_{DDXO} = V_{DDA} = V_{DDO} = 1.8 V ±5%, T_A = –40 to 95 °C.

Parameter	Symbol	Comment	Min	Typ	Max	Unit
Initial start-up time	t_{START}[1]	Time from POR to when the device generates output clocks from NVM frequency plan.	—	25	40	ms
	t_{RDY}	POR to API ready	—	25	30	ms
Output delay adjustment (typical T_{VCO} = 90 ps)	t_{QDIV}	Range[2]	$-T_{VCO}$ x 127	—	$+T_{VCO}$ x 127	ps
		Resolution		T_{VCO}	—	ps
		Resolution (fine delay enabled)		$T_{VCO/4}$	—	ps
Pull-in range	ω_P		—	±100	—	ppm
RMS jitter crystal reference[3,4]	Q Div	644.53125 MHz	—	52	70	fs
		625 MHz	—	53	82	fs
		390.625 MHz	—	52	70	fs
		322.265625 MHz	—	52	70	fs
		312.5 MHz	—	54	70	fs
		156.25 MHz		55	74	fs
		125 MHz		60	80	fs
		100 MHz		65	85	fs
	MultiSynth NA/NB Div	644.53125 MHz	—	57	75	fs
		322.265625 MHz	—	58	80	fs
		156.25 MHz	—	64	85	fs
		125 MHz	—	70	96	fs
		100 MHz	—	112	130	fs
Buffered output jitter performance, 12 kHz to 20 MHz.		Crystal mode	—	78	—	fs
		XO_IN additive jitter	—	39	—	fs

1. Assumes crystal or XO is available at power up.
2. Output delay adjustment range will vary depending on frequency plan. Output delay adjustment range (ns) is displayed in the “Output Skew Control” step of the CBPro Wizard. f_{VCO} range is 10.4 to 13.0 GHz.
3. Added jitter and spurs due to crosstalk is frequency plan dependent and can be determined using the ClockBuilder Pro Spur Analysis tool.
4. Jitter generation test conditions: XTAL = 54 MHz TXC 7M54070001, f_{VCO} < 11 GHz; f_{OUT} LVDS, DSPLL BW = 40 Hz.

Table 6. 100 MHz PCIe Jitter Performance Characteristics (without Spread Spectrum)

V_{DD18} = 1.8 V ±5%, V_{DDA} = V_{DDXO} = 3.3 V ±5%; All other supplies programmable 3.3 V ±5%, 2.5 V ±5%, 1.8 V ±5%, T_A = –40 to 95 °C.
Low-Power Mode: V_{DD18} = V_{DDIN} = V_{DDIO} = V_{DDXO} = V_{DDA} = V_{DDO} = 1.8 V ±5%, T_A = –40 to 95 °C.

Parameter	Symbol	Comment	Min	Typ	Max	PCI-SIG Limit[1]	Unit
100 MHz PCIe common clock jitter performance[2]	DSPLL + Qdiv	Gen 1 (2.5GT/s)	—	14	56	86	ps_{p-p}
		Gen 2 (5GT/s) Low Band	—	2	29	3000	fs_{RMS}
		Gen 2 (5GT/s) High Band	—	86	860	3100	fs_{RMS}
		Gen 3 (8GT/s)	—	24	172	1000	fs_{RMS}
		Gen 4 (16GT/s)	—	23	172	500	fs_{RMS}
		Gen 5 (32GT/s)	—	6	46	150	fs_{RMS}
		Gen 6 (64GT/s)	—	6	40	100	fs_{RMS}
		Gen 7 (128GT/s)	—	4	28	67	fs_{RMS}
	DSPLL + NA/NB Div	Gen 1 (2.5GT/s)	—	14	57	86	ps_{p-p}
		Gen 2 (5GT/s) Low Band	—	2	30	3000	fs_{RMS}
		Gen 2 (5GT/s) High Band	—	117	901	3100	fs_{RMS}
		Gen 3 (8GT/s)	—	34	182	1000	fs_{RMS}
		Gen 4 (16GT/s)	—	33	182	500	fs_{RMS}
		Gen 5 (32GT/s)	—	12	49	150	fs_{RMS}
		Gen 6 (64GT/s)	—	8	42	100	fs_{RMS}
		Gen 7 (128GT/s)	—	6	29	67	fs_{RMS}
100 MHz PCIe separate reference clock jitter performance[2]	DSPLL + Qdiv	Gen 2 (5GT/s) Low Band	—	3	5	2120	fs_{RMS}
		Gen 2 (5GT/s) High Band	—	117	646	2190	fs_{RMS}
		Gen 3 (8GT/s)	—	30	129	707	fs_{RMS}
		Gen 4 (16GT/s)	—	30	129	495	fs_{RMS}
		Gen 5 (32GT/s)	—	11	54	177	fs_{RMS}
		Gen 6 (64GT/s)	—	10	54	106	fs_{RMS}
		Gen 7 (128GT/s)	—	7	38	71	fs_{RMS}
	DSPLL + NA/NB Div	Gen 2 (5GT/s) Low Band	—	3	5	2120	fs_{RMS}
		Gen 2 (5GT/s) High Band	—	142	679	2190	fs_{RMS}
		Gen 3 (8GT/s)	—	37	137	707	fs_{RMS}
		Gen 4 (16GT/s)	—	37	137	495	fs_{RMS}
		Gen 5 (32GT/s)	—	15	57	177	fs_{RMS}
		Gen 6 (64GT/s)	—	12	57	106	fs_{RMS}
		Gen 7 (128GT/s)	—	9	40	71	fs_{RMS}

1. PCI-SIG does not specify a jitter limit for separate reference clock architectures. Instead the PCI-SIG specified simulation limit can be split evenly between transmitter and receiver clocks by dividing by the square root of 2 since their jitter is uncorrelated.
2. Jitter integration as specified by PCI-SIG in the PCI Express® Base Specification Revision 7.0.

Table 7. 100 MHz PCIe Jitter Performance Characteristics (with Spread Spectrum)

V_{DD18} = 1.8 V ±5%, V_{DDA} = V_{DDXO} = 3.3 V ±5%; All other supplies programmable 3.3 V ±5%, 2.5 V ±5%, 1.8 V ±5%, T_A = –40 to 95 °C.
Low-Power Mode: V_{DD18} = V_{DDIN} = V_{DDIO} = V_{DDXO} = V_{DDA} = V_{DDO} = 1.8 V ±5%, T_A = –40 to 95 °C.

Parameter	Symbol	Comment	Min	Typ	Max	PCI-SIG Limit[1]	Unit
100 MHz PCIe common clock jitter performance[2,3]	DSPLL + NB Div	Gen 1 (2.5GT/s)	—	26	70	86	ps P-P
		Gen 2 (5GT/s) Low Band	—	5	43	3000	fs_{RMS}
		Gen 2 (5GT/s) High Band	—	684	1880	3100	fs_{RMS}
		Gen 3 (8GT/s)	—	272	459	1000	fs_{RMS}
		Gen 4 (16GT/s)	—	191	326	500	fs_{RMS}
		Gen 5 (32GT/s)	—	55	103	150	fs_{RMS}
		Gen 6 (64GT/s)	—	37	72	100	fs_{RMS}
		Gen 7 (128GT/s)	—	26	51	67	fs_{RMS}
100 MHz PCIe separate reference clock jitter performance[2,4]	DSPLL + NB Div	Gen 2 (5GT/s) High Band	—	838	1047	2190	fs_{RMS}
		Gen 3 (8GT/s)	—	619	656	707	fs_{RMS}
		Gen 4 (16GT/s)	—	394	463	495	fs_{RMS}
		Gen 5 (32GT/s)	—	66	92	177	fs_{RMS}
		Gen 6 (64GT/s)	—	59	82	106	fs_{RMS}
		Gen 7 (128GT/s)	—	42	58	71	fs_{RMS}

1. PCI-SIG does not specify a jitter limit for separate reference clock architectures. Instead the PCI-SIG specified simulation limit can be split evenly between transmitter and receiver clocks by dividing by the square root of 2 since their jitter is uncorrelated.
2. Jitter integration as specified by PCI-SIG in the PCI Express® Base Specification Revision 7.0.
3. Common clock spread spectrum modulation of –0.4%.
4. Separate reference spread modulation of –0.4% Gen2 to Gen4, –0.3% Gen5 to Gen6, and –0.15% Gen7.

Table 8. DC Characteristics

V_{DD18} = 1.8 V ±5%, V_{DDXO} = V_{DDA} = 3.3 V ±5%, All other supplies programmable 3.3 V ±5%, 2.5 V ±5%, 1.8 V ±5%, T_A = –40 to 95 °C.
Low Power Mode: V_{DD18} = V_{DDIN} = V_{DDIO} = V_{DDXO} = V_{DDA} = V_{DDO} = 1.8 V ±5%, T_A = –40 to 95 °C.

Parameter	Symbol	Test Condition	Min	Typ	Max	Unit
Core supply current (V_{DD12} + V_{DDA})	I_{DD18}	SKY62101[1,2]	—	400	650	mA
	I_{DDA}	SKY62101[1,2]		190	230	mA
	I_{DD18_PD}	RSTb = 0	—	120	300	mA
	I_{DDA_PD}	RSTb = 0	—	15	16	mA
Peripheral supply current (VDDIN + VDDIO + VDDXO)	I_{DDIN} + I_{DDIO}	SKY62101[1,2]	—	32	50	mA
	I_{DDXO}	SKY62101[1,2]	—	12	15	mA
	I_{DDIN_PD} + I_{DDIO_PD} + I_{DDXO_PD}	RSTb = 0	—	2	3	mA
Output buffer supply current (V_{DDOX})	I_{DDOX} (per output)	LVPECL (2.5 V, 3.3 V) @ 156.25 MHz[3]	—	24	26	mA
		LVDS (2.5 V, 3.3 V) @ 156.25 MHz[3]	—	13	15	mA
		S-LVDS (1.8 V) @ 156.25 MHz[3]	—	12	14	mA
		CML (1.8 V, 2.5 V, 3.3 V) @ 156.25 MHz[3]	—	14	17	mA
		3.3 V LVCMOS @ 156.25 MHz[4]	—	19	22	mA
		2.5 V LVCMOS @ 156.25 MHz[4]	—	15	17	mA
		1.8 V LVCMOS @ 156.25 MHz[4]	—	11	22	mA
		HCSL internal termination (1.8 V, 2.5 V, 3.3 V) @ 156.25 MHz[5]	—	20	23	mA
	I_{DDOX_PD}	RSTb = 0	—	0.2	0.3	mA
Total power dissipation	P_D	SKY62101[1]	—	2.0	2.8	W
		SKY62101 low-power mode[1]	—	1.4	2.0	W
Supply voltage ramp rate	T_{VDD}	Fastest V_{DD} ramp rate allowed on startup	—	—	100	V/ms

1. Typical test configuration: The following frequencies on 12 LVDS outputs: 4–156.25 MHz (Q), 2–312.5 MHz (Q), 1–125 MHz (Q), 1–100 MHz (NB), 1–50 MHz (NB), 2–644.53125 MHz (NA), 1–322.265625 MHz (NA). Excludes power in termination resistors. VDDIN = 1.8 V; VDDO = 3.3 V.
2. Typical test configuration: Same as Note 1, except all supplies set to 1.8 V for Low-Power Mode. Output formats changed to S-LVDS format.
3. Differential outputs terminated into an ac-coupled differential 100 Ω load.
4. LVCMOS outputs measured into a 5-inch, 50 Ω PCB trace with 5 pF load.
5. No external termination; amplitude 800 mVpp_se.

Table 9. Input Specifications

V_{DD18} = 1.8 V ±5%, V_{DDXO} = V_{DDA} = 3.3 V ±5%, All other supplies programmable 3.3 V ±5%, 2.5 V ±5%, 1.8 V ±5%, T_A = –40 to 95 °C.
Low Power Mode: V_{DD18} = V_{DDIN} = V_{DDIO} = V_{DDXO} = V_{DDA} = V_{DDO} = 1.8 V ±5%, T_A = –40 to 95 °C.

Parameter	Symbol	Test Conditions	Min	Typ	Max	Units
LVCMOS (XO Applied to XO_IN)						
Input frequency range	f_{IN_CMOS}		30.72	—	250	MHz
Slew rate[1,2,3]	SR		0.75	—	—	V/ns
Input voltage	V_{IL}		—	—	V_{DDXO} x 0.3	V
	V_{IH}		V_{DDXO} x 0.7	—	—	V
Input resistance	R_{IN}		—	63	—	kΩ
Duty cycle	DC		40	—	60	%
Capacitance	C_{IN_SE}		—	1.25	—	pF
Crystal (Connected to XA/XB Pins)[4]						
Frequency range	f_{IN_XTAL}		48	—	61.44	MHz
Load capacitance	C_L		—	8	—	pF
Crystal drive level	d_L		—	—	200	µW
Equivalent series resistance	RESR		Refer to the Recommended XTAL, XO, VCXO, TCXO, and OCXO Reference Manual to determine ESR and shunt capacitance values.			
Shunt capacitance	C0					
Other Control Input Pins: RSTb, FINC, FDEC, OE[5]						
Update rate	f_{UR}	RSTb	—	—	1	Hz
		FINC, FDEC	—	—	800	kHz
Input voltage	V_{IL}		—	—	V_{DDIO} x 0.3	V
	V_{IH}		V_{DDIO} x 0.7	—	—	V
Minimum pulse width	PW		150	—	—	ns
Programmable internal pullup, pulldown	R_{IN}		—	20	—	kΩ

1. The minimum slew rate on the XO applied to XO_IN is recommended to meet the specified jitter performance.
2. To achieve this slew rate and voltage swing, use one of the XOs from the Recommended XTAL, XO, VCXO, TCXO, and OCXO Reference Manual placed as close as possible to the XO_IN pins.
3. Slew rate can be estimated using the following simplified equation: SR = ((0.8 – 0.2) x $V_{IN\_VPP\_SE}$)/t_r.
4. To meet specified jitter performance use one of the XTALs from the "Recommended XTAL, XO, VCXO, TCXO, and OCXO Reference Manual.
5. Glitches and toggles on RSTb more frequent than f_{UR} may cause the device to lock up in reset. Power cycle the device to restore operation.

Table 10. Differential Clock Output Specifications

V_{DD18} = 1.8 V ±5%, V_{DDXO} = V_{DDA} = 3.3 V ±5%, All other supplies programmable = 3.3 V ±5%, 2.5 V ±5%, 1.8 V ±5%, T_A = –40 to 95 °C.
Low Power Mode: V_{DD18} = V_{DDIN} = V_{DDIO} = V_{DDXO} = V_{DDA} = V_{DDO} = 1.8 V ±5%, T_A = –40 to 95 °C.

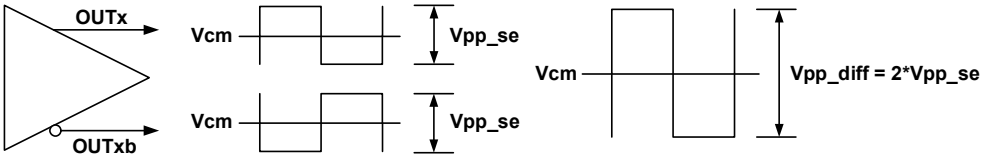
Parameter	Symbol	Test Condition		Min	Typ	Max	Units
Output frequency[1]	f_{OUT}	Q divider (Grade A/C)[2]		0.008	—	3200	MHz
		Q divider (Grade B/D)[2]		0.008	—	650	MHz
		NA divider, NB divider (Grade A)[3]		0.008	—	650	MHz
		NA divider, NB divider (Grade B)[3]		0.008	—	350	MHz
Duty cycle	DC	f < 400 MHz		49.5	50.0	50.5	%
		400 MHz < f < 3.2 GHz		48.0	50.0	52.0	%
Output-to-output skew	T_{SK}	Q divider outputs, same differential format		–50	—	50	ps
		MultiSynth (NA or NB) outputs, same differential format, same MultiSynth					
OUT-OUTb skew[4]	T_{SK_OUT}	VDDO = 3.3 V	LVPECL, LVDS, CML, custom diff f ≤ 160 MHz	–6	—	6	ps
		VDDO = 2.5 V	LVPECL, LVDS, CML, custom diff f ≤ 160 MHz	–5	—	25	ps
		VDDO = 3.3 V/2.5 V	LVPECL, LVDS, CML, custom diff f > 160 MHz	–10	—	15	ps
		VDDO = 1.8 V	CML, S-LVDS, and custom diff all frequencies	–10	—	30	ps
Output voltage swing[5]	V_{OUT}	VDDO = 3.3 V/2.5 V	LVDS	330xSF	360xSF	380xSF	mVpp_se
		VDDO = 1.8 V	S-LVDS	350xSF	370xSF	410xSF	mVpp_se
		VDDO = 3.3 V/2.5 V	AC-coupled LVPECL	780xSF	840xSF	910xSF	mVpp_se
		VDDO = 3.3 V/2.5 V/1.8 V	CML	390xSF	420xSF	460xSF	mVpp_se
		VDDO = 3.3 V/2.5 V	Custom differential, 600 mVpp_se	560xSF	630xSF	710xSF	mVpp_se
Output voltage swing scaling factor (SF)	SF	f < 500 MHz		0.9	1.00	1.00	SF
		500 MHz < f < 1 GHz		0.8	1.00	0.95	SF
		1 GHz < f < 1.3 GHz		0.5	0.6	0.75	SF
Common mode voltage	V_{CM}	VDDO = 3.3 V/2.5 V	LVDS, custom differential, CML, ac-coupled LVPECL	1.15	1.20	1.25	V
		VDDO = 1.8 V	S-LVDS, CML	0.85	0.90	0.95	V
Rise and fall times (20% to 80%)	t_r/t_f	VDDO = 3.3 V/2.5 V	AC-coupled LVPECL	—	125	260	ps
		VDDO = 3.3 V/2.5 V, f<100 MHz	LVDS, custom differential	—	125	260	ps
		VDDO = 3.3 V/2.5 V, f≥100 MHz		—	125	200	ps
		VDDO = 1.8 V, f<500 MHz	S-LVDS	—	150	250	ps
		VDDO = 1.8 V, f≥500 MHz		—	125	200	ps
		VDDO = 3.3 V/2.5 V/1.8 V	CML	—	150	280	ps
Differential output impedance	Z_O	Differential formats		—	100	—	Ω

Table 10. Differential Clock Output Specifications (Continued)

V_{DD18} = 1.8 V ±5%, V_{DDXO} = V_{DDA} = 3.3 V ±5%, All other supplies programmable = 3.3 V ±5%, 2.5 V ±5%, 1.8 V ±5%, T_A = –40 to 95 °C.
Low Power Mode: V_{DD18} = V_{DDIN} = V_{DDIO} = V_{DDXO} = V_{DDA} = V_{DDO} = 1.8 V ±5%, T_A = –40 to 95 °C.

Parameter	Symbol	Test Condition	Min	Typ	Max	Units
Power supply noise rejection[6]	PSR	25 kHz sinusoidal noise	—	–94	—	dBc
		100 kHz sinusoidal noise	—	–95	—	dBc
		500 kHz sinusoidal noise	—	–91	—	dBc
		1 MHz sinusoidal noise	—	–91	—	dBc
Output-to-output crosstalk[7]	$XTALK_{OUT}$	Differential outputs, same format	—	–95	—	dBc

1. HCSL output format is not supported for f_{OUT} > 400 MHz.
2. Q dividers support output frequencies within the specified range equal to f_{VCO}/Q, where Q is an integer.
3. NA, NB MultiSynths support any output frequency within the specified range.
4. Skew between positive and negative output pins.
5. Output voltage swing is dependent on frequency range. Scale all values by the Output Voltage Swing Scaling Factor (SF). Voltage swing is specified in mVpp_SE as shown in the following figure.



6. Measured for a 156.25 MHz LVDS output frequency. 100 mVpp sine wave noise added to VDDO = 3.3 V and noise spur amplitude measured.
7. Crosstalk spur measured with the victim running at 156.25 MHz and the aggressor at 155.52 MHz. Victim and aggressor are separated by two unused channels.

Table 11. HCSL Clock Output Specifications

V_{DD18} = 1.8 V ±5%, V_{DDIN} = V_{DDIO} = 3.3 V ±5%, 1.8 V ±5%, V_{DDREF} = V_{DDA} = 3.3 V ±5%, V_{DDO} = 3.3 V ±5%, 2.5 V ±5%, 1.8 V ±5%, T_A = –40 to 95 °C; Low Power Mode: V_{DD18} = V_{DDIN} = V_{DDIO} = V_{DDREF} = V_{DDA} = V_{DDO} = 1.8 V ±5%, T_A = –40 to 95 °C.

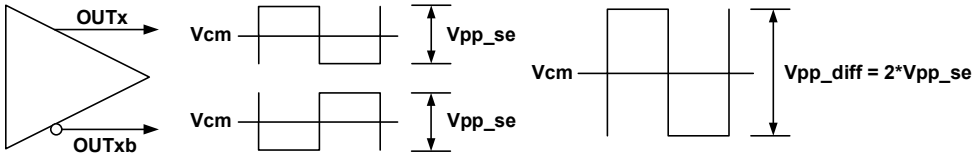
Parameter	Symbol	Test Condition			Min	Typ	Max	Units
Output frequency	f_{OUT}	Q divider, NA divider, NB divider[1]			0.008	—	500	MHz
Duty cycle	DC	f < 400 MHz			49.5	50.0	50.5	%
		400 MHz < f < 500 MHz			48.0	50.0	52.0	%
Output-to-output skew	T_{SK}	Q divider outputs, same differential format			–50	—	50	ps
		MultiSynth (NA or NB) outputs, same differential format, same MultiSynth			–50	—	50	ps
OUT-OUTb skew[2]	T_{SK_OUT}	Skew between positive and negative output pins	VDDO = 3.3 V	HCSL standard, 800 mVpp_se, internal termination	—	—	15	ps
				HCSL standard, 800 mVpp_se, external termination	—	—	25	ps
				HCSL fast, 800 mV or 1200 mV, external termination	—	—	10	ps
			VDDO = 2.5 V	HCSL standard, 800 mVpp_se, internal termination	—	—	15	ps
				HCSL standard, 800 mVpp_se, external termination	—	—	30	ps
				HCSL fast, 800 mV or 1200 mV, external termination	—	—	20	ps
			VDDO = 1.8 V	HCSL standard, 800 mVpp_se, internal termination	—	—	22	ps
				HCSL standard, 800 mVpp_se, external termination	—	—	70	ps
				HCSL fast, 800 mV, external termination	—	—	36	ps
Output voltage swing[3]	V_{OUT}	VDDO = 3.3 V/2.5 V/1.8 V		HCSL standard, 800 mVpp_se, internal termination	740xSF	810xSF	1000xSF	mVpp_se
		VDDO = 3.3 V/2.5 V/1.8 V		HCSL standard, 800 mVpp_se, external termination	730xSF	810xSF	1000xSF	mVpp_se
		VDDO = 3.3 V/2.5 V		HCSL fast, 800 mVpp_se, external termination	730xSF	810xSF	1000xSF	mVpp_se
		VDDO = 3.3 V/2.5 V		HCSL fast, 1200 mVpp_se, external termination	1100xSF	1175xSF	1260xSF	mVpp_se
Output voltage swing Scaling Factor (SF) standard, 800 mVpp_se, internal termination	SF	f < 8 kHz			1	1	1	SF
		8 kHz < f < 100 MHz			0.91	0.94	0.96	SF
		100 MHz < f < 200 MHz			0.89	0.91	0.93	SF
		200 MHz < f < 400 MHz			0.83	0.85	0.92	SF
		f > 400 MHz			0.74	0.78	0.89	SF
Output voltage swing Scaling Factor (SF) standard, 800 mVpp_se, external termination	SF	f < 8 kHz			1	1	1	SF
		8 kHz < f < 100 MHz			0.97	0.96	0.96	SF
		100 MHz < f < 200 MHz			0.94	0.93	0.95	SF
		200 MHz < f < 400 MHz			0.91	0.90	0.88	SF
		f > 400 MHz			0.68	0.71	0.75	SF

Table 11. HCSL Clock Output Specifications (Continued)

V_{DD18} = 1.8 V ±5%, V_{DDIN} = V_{DDIO} = 3.3 V ±5%, 1.8 V ±5%, V_{DDREF} = V_{DDA} = 3.3 V ±5%, V_{DDO} = 3.3 V ±5%, 2.5 V ±5%, 1.8 V ±5%, T_A = –40 to 95 °C; Low Power Mode: V_{DD18} = V_{DDIN} = V_{DDIO} = V_{DDREF} = V_{DDA} = V_{DDO} = 1.8 V ±5%, T_A = –40 to 95 °C.

Parameter	Symbol	Test Condition		Min	Typ	Max	Units
Output voltage swing Scaling Factor (SF) Fast, 800 or 1200 mVpp_se, external termination	SF	f < 8 kHz		1	1	1	SF
		8 kHz < f < 100 MHz		0.98	0.99	0.99	SF
		100 MHz < f < 200 MHz		0.94	0.94	0.95	SF
		200 MHz < f < 400 MHz		0.94	0.95	0.94	SF
		f > 400 MHz		0.89	0.92	0.91	SF
Common mode voltage	V_{CM}	VDDO = 3.3 V/2.5 V/1.8 V	HCSL 800 mVpp_se	0.35	0.425	0.52	V
		VDDO = 3.3 V/2.5 V	HCSL 1200 mVpp_se	0.55	0.6	0.68	V
Rise and fall times (20% to 80%)	t_r/t_f	VDDO = 3.3 V/2.5 V/1.8 V	HCSL fast, 800 or 1200 mVpp_se, external termination	—	270	360	ps
		VDDO = 3.3 V/2.5 V/1.8 V	HCSL standard, 800 mVpp_se, external termination	—	450	700	ps
		VDDO = 3.3 V/2.5 V/1.8 V	HCSL standard, 800 mVpp_se, internal termination	—	270	420	ps
Differential output impedance	Z_O	HCSL standard slew rate, internal termination		—	100	—	Ω
		HCSL standard slew rate, external termination		—	Hi-Z	—	Ω
		HCSL fast slew rate, external termination		—	200	—	Ω
Output-to-output crosstalk[4]	$XTALK_{OUT}$	Differential outputs, same format		—	–95	—	dBc
Input-to-output crosstalk[5]	$XTALK_{IN}$	HCSL input and output, same format		—	–90	—	dBc

1. NA, NB MultiSynths support any output frequency within the specified range.
2. Skew between positive and negative output pins.
3. Output voltage swing is dependent on frequency range, HCSL slew rate, and HCSL termination settings. Scale all voltage swing values by the scaling factor (SF). Voltage swing is specified in mVpp_SE as shown in the following figure.



4. Crosstalk spur measured with the victim running at 156.25 MHz and the aggressor at 155.52 MHz. Victim and aggressor are separated by two unused channels.
5. Crosstalk spur measured with the victim running at 156.25 MHz on OUT0 and the aggressor at 155.52 MHz on IN3.

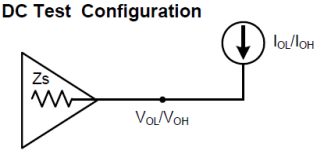
Table 12. LVCMOS Clock Output Specifications

V_{DD18} = 1.8 V ±5%, V_{DDXO} = V_{DDA} = 3.3 V ±5%, All other supplies programmable = 3.3 V ±5%, 2.5 V ±5%, 1.8 V ±5%, T_A = –40 to 95 °C.
Low Power Mode: V_{DD18} = V_{DDIN} = V_{DDIO} = V_{DDXO} = V_{DDA} = V_{DDO} = 1.8 V ±5%, T_A = –40 to 95 °C.

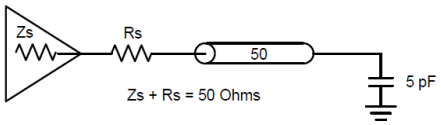
Parameter	Symbol	Test Condition	Min	Typ	Max	Units
Output frequency	f_{OUT}	Q divider[1]	0.008	—	250	MHz
		NA or NB divider[2]	0.008	—	250	MHz
Duty cycle	DC	f < 100 MHz	49.5	—	50.5	%
		100 MHz < f < 250 MHz	45	—	55	%
Output voltage high[3]	V_{OH}	VDDO = 3.3 V/2.5 V/1.8 V	V_{DDO} x 0.85	—	—	V
Output voltage low[3]	V_{OL}	I_{OH} = –8/–6/–4 mA, I_{OL} = 8/6/4 mA	—	—	V_{DDO} x 0.15	V
Rise and fall times (20% to 80%)[4,5]	t_r/t_f	LVCMOS	0.35	0.8	1.35	ns

1. Q dividers support output frequencies within the specified range equal to $f_{VCO/Q}$ where Q is an integer.
2. NA, NB MultiSynths support any output frequency within the specified range.
3. V_{OL}/V_{OH} is measured at I_{OL}/I_{OH} as shown in the "DC Test Configuration" portion of the drawing below.
4. A 15 to 25 Ω series termination resistor (Rs) is recommended to help match the source impedance to a 50 Ω PCB trace. A 5 pF capacitive load is assumed as shown in the "AC Test Configuration" portion of the drawing below.

DC Test Configuration



AC Test Configuration



5. Slew rate limited (SRL) LVCMOS format clocks are intended only for low-frequency clock applications.

Table 13. Output Status Pin Specifications

VDDIO = 3.3 V ±5%, 2.5 V ±5%, 1.8 V ±5%, T_A = –40 to 95 °C, Low-Power Mode: V_{DDIO} = 1.8 V ±5%.

Parameter	Symbol	Test Condition	Min	Typ	Max	Units
Status Output Pins (GPIO, SDA)						
Output voltage high[1]	V_{OH}	I_{OH} = –2 mA	V_{DDIO} x 0.85	—	—	V
Output voltage low	V_{OL}	I_{OL} = 2 mA	—	—	V_{DDIO} x 0.15	V

1. The V_{OH} specification does not apply to the open-drain SDA output when the serial interface is in I^2C mode. V_{OL} remains valid in all cases.

Table 14. I²C Timing Specifications (SCL, SDA)

V_{DD18} = 1.8 V ±5%, V_{DDXO} = V_{DDA} = 3.3 V ±5%; All other supplies programmable 3.3 V ±5%, 2.5 V ±5%, 1.8 V ±5%, T_A = –40 to 95 °C.
Low Power Mode: V_{DD18} = V_{DDIN} = V_{DDIO} = V_{DDXO} = V_{DDA} = V_{DDO} = 1.8 V ±5%, T_A = –40 to 95 °C.

Parameter	Symbol	Standard Mode 100 kbps		Fast Mode 400 kbps		Unit
		Min	Max	Min	Max	
SCL clock frequency	f_{SCL}	—	100	—	400	kHz
SMBus timeout	—	25	35	25	35	ms
Hold time (repeated) START condition	$t_{HD:STA}$	4.0	—	0.6	—	µs
Low period of the SCL clock	t_{LOW}	4.7	—	1.3	—	µs
HIGH period of the SCL clock	t_{HIGH}	4.0	—	0.6	—	µs
Setup time for a repeated START condition	$t_{SU:STA}$	4.7	—	0.6	—	µs
Data hold time	$t_{HD:DAT}$	100	—	100	—	ns
Data setup time	$t_{SU:DAT}$	250	—	100	—	ns
Rise time of both SDA and SCL signals	t_r	—	1000	20	300	ns
Fall time of both SDA and SCL signals	t_f	—	300	—	300	ns
Setup time for STOP condition	$t_{SU:STO}$	4.0	—	0.6	—	µs
Bus free time between a STOP and START condition	t_{BUF}	4.7	—	1.3	—	µs
Data valid time	$t_{VD:DAT}$	—	3.45	—	0.9	µs
Data valid acknowledge time	$t_{VD:ACK}$	—	3.45	—	0.9	µs

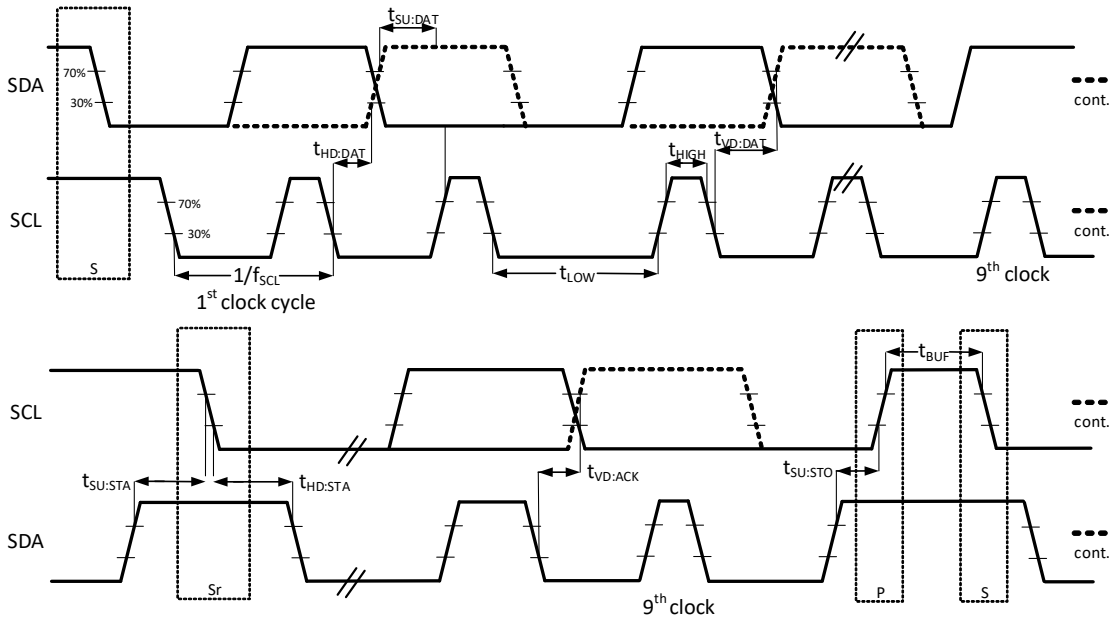


Figure 3. I²C Serial Port Timing Standard and Fast Modes

Table 15. SPI Timing Specifications (4-Wire)

V_{DD18} = 1.8 V ±5%, V_{DDXO} = V_{DDA} = 3.3 V ±5%, All other supplies programmable 3.3 V ±5%, 2.5 V ±5%, 1.8 V ±5%, T_A = –40 to 95 °C.
Low Power Mode: V_{DD18} = V_{DDIN} = V_{DDIO} = V_{DDXO} = V_{DDA} = V_{DDO} = 1.8 V ±5%, T_A = –40 to 95 °C.

Parameter	Symbol	Min	Typ	Max	Unit
SCLK frequency	f_{SPI}	—	—	30	MHz
SCLK duty cycle	T_{DC}	40	—	60	%
SCLK period	T_C	33.333	—	—	ns
Delay time, SCLK fall to SDO active	T_{D1}	—	12.5	20	ns
Delay time, SCLK fall to SDO	T_{D2}	—	10	15	ns
Delay time, CSb rise to SDO tri-state	T_{D3}	—	10	20	ns
Setup time, CSb to SCLK	T_{SU1}	5	—	—	ns
Hold time, SCLK fall to CSb	T_{H1}	5	—	—	ns
Setup time, SDI to SCLK rise	T_{SU2}	5	—	—	ns
Hold time, SDI to SCLK rise	T_{H2}	5	—	—	ns
Delay time between chip selects (CSb)	T_{CS}	5	—	—	µs

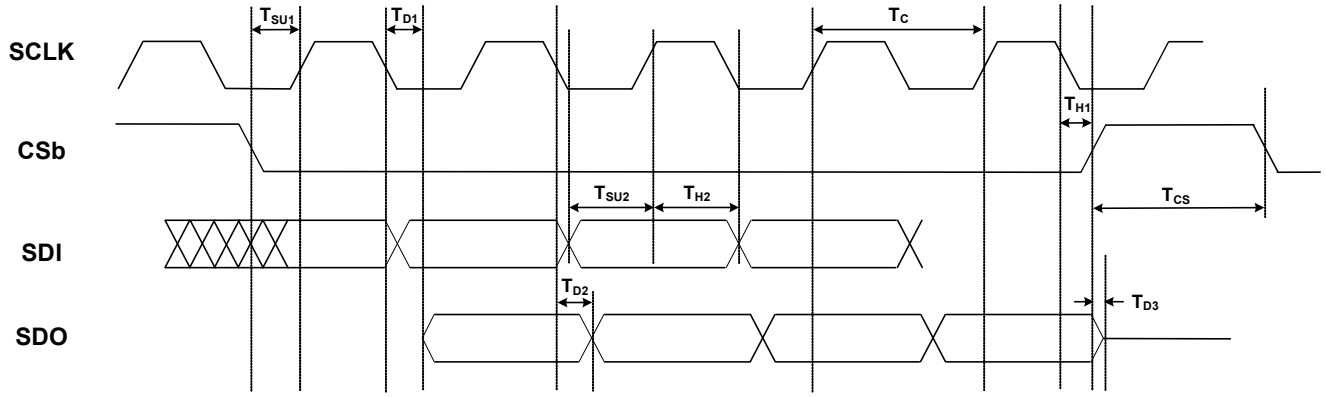


Figure 4. SPI Serial Interface Timing (4-Wire)

Table 16. SPI Timing Specifications (3-Wire)

V_{DD18} = 1.8 V ±5%, V_{DDXO} = V_{DDA} = 3.3 V ±5%, All other supplies programmable 3.3 V ±5%, 2.5 V ±5%, 1.8 V ±5%, T_A = –40 to 95 °C.
Low Power Mode: V_{DD18} = V_{DDIN} = V_{DDIO} = V_{DDXO} = V_{DDA} = V_{DDO} = 1.8 V ±5%, T_A = –40 to 95 °C.

Parameter	Symbol	Min	Typ	Max	Unit
SCLK frequency	f_{SPI}	—	—	30	MHz
SCLK duty cycle	T_{DC}	40	—	60	%
SCLK period	T_C	33.33	—	—	ns
Delay time, SCLK fall to SDIO turn-on	T_{D1}	—	12.5	20	ns
Delay time, SCLK fall to SDIO next-bit	T_{D2}	—	10	15	ns
Delay time, CSb rise to SDIO tri-state	T_{D3}	—	10	20	ns
Setup time, CSb to SCLK	T_{SU1}	5	—	—	ns
Hold time, CSb to SCLK fall	T_{H1}	5	—	—	ns
Setup time, SDI to SCLK rise	T_{SU2}	5	—	—	ns
Hold time, SDI to SCLK rise	T_{H2}	5	—	—	ns
Delay time between chip selects (CSb)	T_{CS}	5	—	—	µs

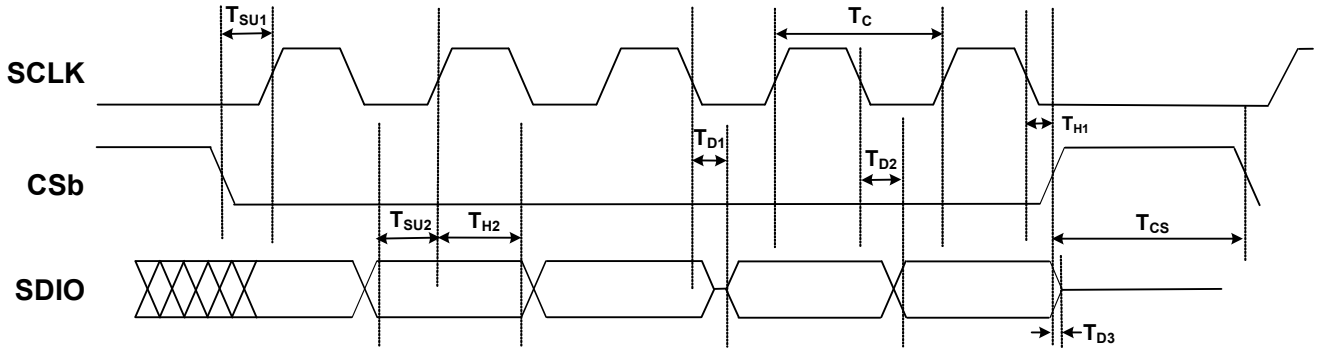


Figure 5. SPI Serial Interface Timing (3-Wire)

4. Typical Operating Characteristics

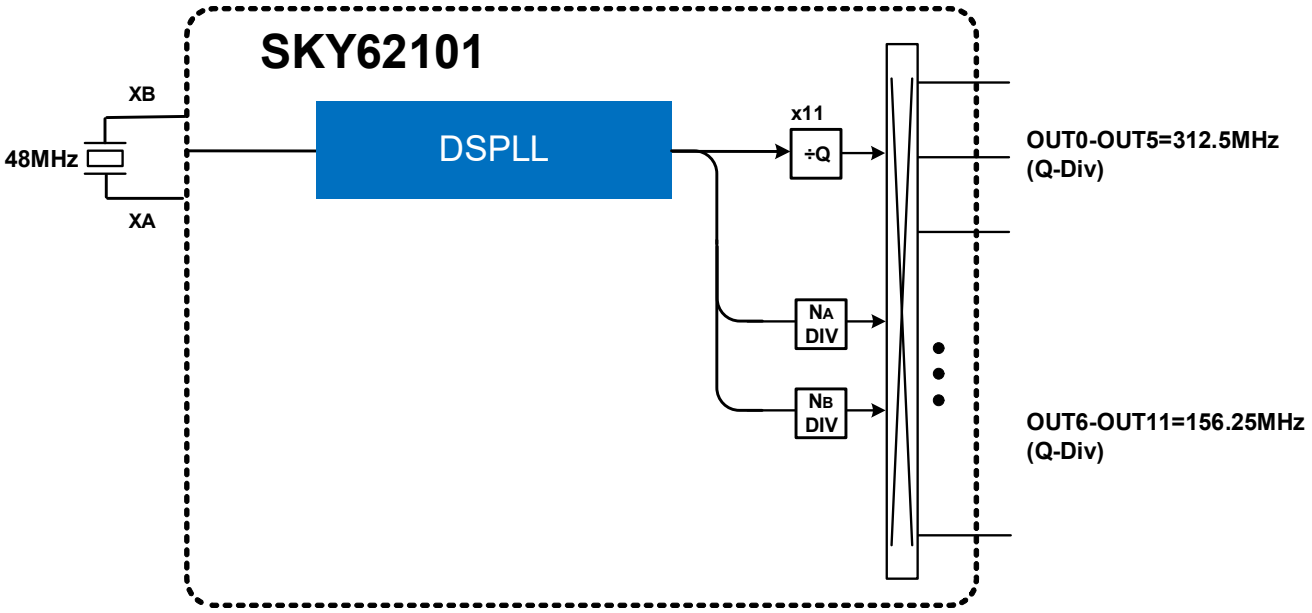


Figure 6. Typical Operating Circuit

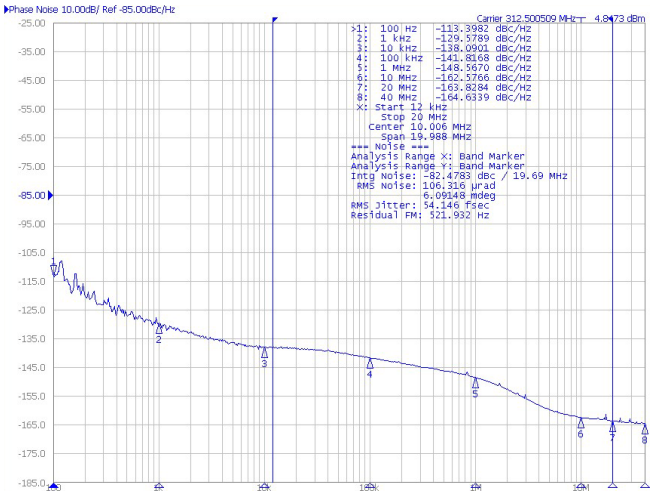


Figure 7. 54.1 fs RMS Jitter for SyncE 312.5 MHz

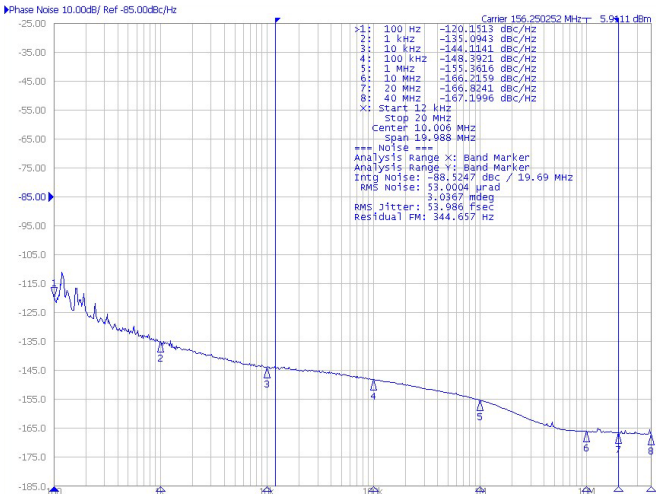


Figure 8. 53.9 fs RMS Jitter for SyncE 156.25 MHz

5. Functional Description

The SKY62101 Fifth-generation DSPLL provides any-frequency multiplication of the reference or selected input frequency. Input switching is controlled manually via API command. The output frequency stability and accuracy is determined by the crystal and oscillator circuit (OSC) or the selected input reference. The integer dividers (Q) and MultiSynth dividers generate integer or fractionally related output frequencies for the output stage.

A cross point switch connects any of the integer dividers (Q) and MultiSynth-generated frequencies to any of the outputs. Additional integer (R) determines the final output frequency for the MultiSynth generated outputs. Integer divider (R) is not used for integer (Q). For best jitter performance, the integer Q divider is preferred.

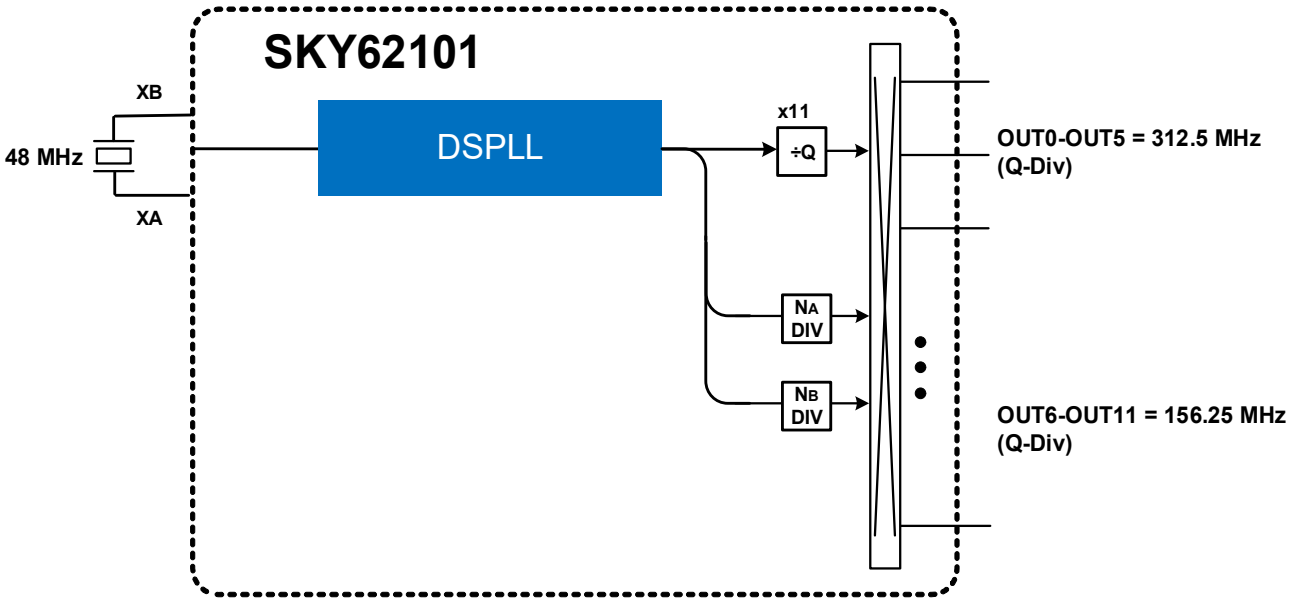


Figure 9. Typical 56G/112G/224G SerDes Application (Up to Three Domains)

5.1. Frequency Configuration

The frequency configuration of the DSPLL is programmable through the serial interface and can also be stored in non-volatile memory. The combination of input dividers, fractional frequency multiplication, integer output division (Q), fractional output division (N), and integer output division (R) allows the generation of virtually any output frequency on any of the outputs. All divider values for a specific frequency plan are easily determined using the CBPro utility.

5.2. Inputs

5.2.1. XA/XB Crystal Inputs

An internal crystal oscillator exists between pins XA and XB. When this oscillator is enabled, an external crystal connected across these pins will oscillate and provide a clock input to the PLL. A crystal frequency of 48 MHz can be used although crystals in the frequency range of 48 MHz to 54 MHz are recommended for best jitter performance. The device includes internal XTAL loading capacitors, which eliminates the need for external capacitors and also has the benefit of reduced noise coupling from external sources.

The "Fifth Generation DSPLL Clock Generator Reference Manual" provides additional information on PCB layout recommendations for the crystal to ensure optimum jitter performance. Refer to the Recommended XTAL, XO, VCXO, TCXO, and OCXO Reference Manual for crystal specifications and recommended crystals.

To achieve optimal jitter performance and minimize BOM cost, a crystal is recommended on the XA/XB crystal input. A clock (e.g., XO) may be used through the XO_IN input but may result in higher output jitter unless the phase noise of the XO is extremely low. When using an external XO, it is important to select one that meets the jitter performance requirements of the end application.

5.2.2. XO_IN Inputs

An alternative to using an external XTAL is to connect a crystal oscillator (XO) directly to the XO_IN input. The XO_IN inputs accommodate single-ended CMOS input. Note that XO phase noise below the PLL loop bandwidth of approximately 1 MHz passes through to the output. In addition to selecting XOs with appropriate noise in this frequency band, be sure to filter the VDD supplying power to the XO since many XOs have poor supply rejection.

5.3. Outputs

The SKY62101 supports 12 differential output drivers with configurable voltage swing and common-mode voltage covering a wide variety of differential signal formats. In addition to preset differential levels, such as LVPECL, LVDS, S-LVDS, CML, and HCSL, the SKY62101 can also be programmed to a custom differential threshold that allows the signal to be sent directly to other chipsets without complicated termination circuits, reducing the complexity of board layout.

The outputs can also be configured as single-ended LVCMOS (3.3 V, 2.5 V, or 1.8 V) providing up to 24 single-ended outputs or any combination of differential and single-ended outputs. The outputs have power supply pins (VDDOx) for output driver groups of 3-2-4-3, which can be powered at 3.3 V, 2.5 V, or 1.8 V. The LVCMOS output voltage is set by the VDDOx pin. Refer to Table 1, “Pin Descriptions,” on page 4.

5.3.1. Output Crosspoint

A crosspoint allows any of the output drivers to connect with the PLL, reference input, or any NA/NB MultiSynth output. A digital output delay adjustment is possible on each of the Q divider outputs to provide output-to-output alignment for the same output source. The crosspoint configuration and delay adjustments are programmable and are stored in NVM so that the desired output configuration is ready at power-up.

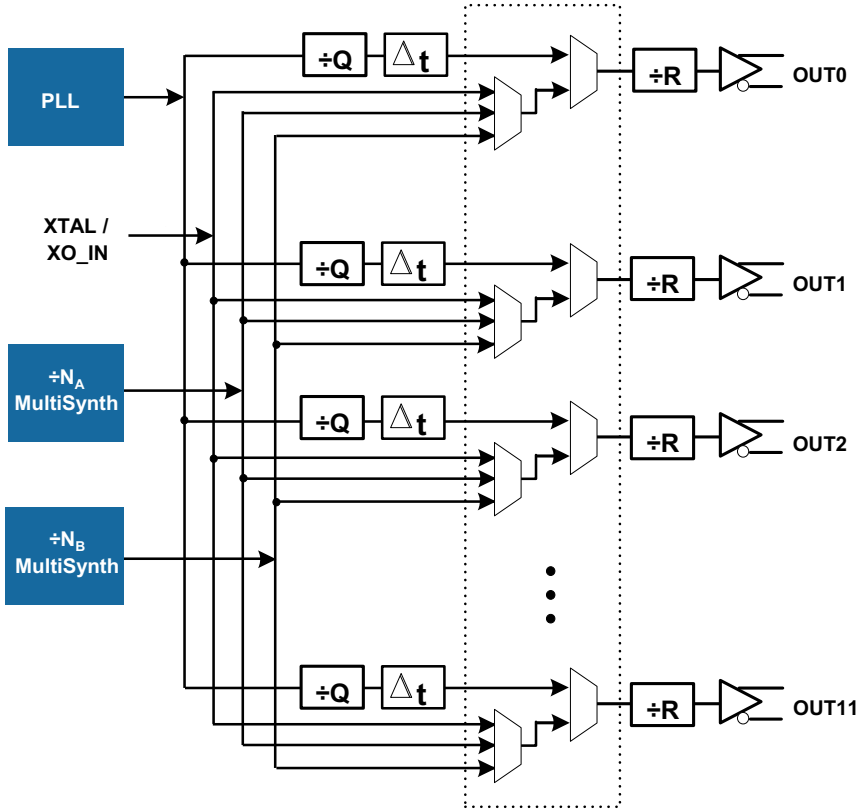


Figure 10. Output Structure

5.3.2. Differential and LVCMOS Output Terminations

Refer to the "Fifth Generation DSPLL Clock Generator Reference Manual" for guidance on output terminations.

5.3.3. Output Enable/Disable

Each output driver may be enabled/disabled through programmable GPIO pins. There are two output enable groups, OE0 and OE1, which are logically ORed together to determine which outputs are enabled at any point in time. CBPro allows the control and selection of the GPIO pin mapping to the outputs.

Outputs may also be enabled/disabled using the device API. For more details on controlling the output enable/disable, please refer to the "Fifth Generation DSPLL Clock Generator Reference Manual".

5.3.4. State of Disabled Output

The disabled state of an output driver may be configured as stop high, stop low, or Hi-Z. CMOS outputs <2 MHz can also be configured as Hi-Z with weak internal pull-up/down.

When disabled, differential outputs maintain the output common-mode voltage even while the output is not toggling. This minimizes disturbances when disabling and enabling clock outputs.

5.3.5. Output Dividers

The device utilizes both integer Q dividers and fractional NA, NB MultiSynth output dividers. The ClockBuilder Pro software chooses the optimal divide values based on the user-defined frequency plan.

A summary of each class of divider is listed below:

1. Output Q divider: Q0 to Q11
   a. Integer-only Divide Value
2. Output N divider: NA, NB
   a. MultiSynth divider, Integer or Fractional divide value
3. Output divider: R0–R11
   a. Integer-only divide value

5.3.6. Output Skew Control

Output skew control allows outputs that are derived from the Q dividers to be phase-adjusted in steps of 1/fvco or 1/(4 x fvco) when the fine adjust is enabled. The exact skew adjustment and step sizes are reported on the Output Skew Control tab of the CBPro Wizard.

5.3.7. Dynamic Phase Adjust

Output skew can also be controlled dynamically by API command during operation using OUTPUT_PHINC and OUTPUT_PHDEC. The parameter settings for API control can be found on the ClockBuilder Pro tab of Dynamic Phase Adjust (DPA) Outputs.

5.4. DSPLL®

The DSPLL controls the central VCO, which provides many of the essential functions for the device, such as generating ultra-low phase noise clocks and maintaining frequency accuracy. It operates by referencing one of many external frequency sources. In crystal mode, a simple low-cost, fixed-frequency crystal (XTAL) may provide the low phase noise reference. The option of using a crystal oscillator (XO) is also available.

5.5. MultiSynthA (NA) and MultiSynthB (NB)

In general, both MultiSynthA and MultiSynthB have identical performance and flexibility and can be independently configured and controlled through the serial interface. Each of the MultiSynths support an optional DCO mode.

5.5.1. DCO Mode

The DCO in the DSPLL can be frequency controlled in predefined steps ranging from <1 ppt to several ppm. The DCO can be controlled when the DSPLL is locked to an external input. The frequency adjustments are controlled through the serial interface by triggering a Device API command or by pin control using frequency increments (FINC) or frequency decrements (FDEC). Both the FINC and FDEC pins are available through the configurable GPIO pins. The DSPLL can be assigned to the FINC and FDEC pins. A FINC adds the frequency step word to the DSPLL output frequency, while an FDEC decrements it.

The PLL feedback divider may also use FINC/FDEC DCO, adjusting all output frequencies simultaneously. This mode is only available using API commands.

5.6. GPIO Pins General Purpose Input or Output

There are four GPIO pins with programmable functions. They can be assigned as either an input or an output from one of the functions shown in Table 17 below. OUT2/11 can be repurposed as GPIOs, for both the internal NVM and external flash variants, when they are not being used as clock outputs.

The GPIOs are programmable as either active-high or active-low via ClockBuilder Pro. Active-low GPIs are indicated by adding a “b” at the end of the function name, for example, “OEb” as displayed in ClockBuilder Pro. All GPI pins have a weak pull-up (PU) or pull-down (PD) resistor to set a default state when not externally driven. The default state of the GPI is always deasserted except for OEx, which is asserted by default to enable the outputs. The internal resistance of the PU/PD resistor is 20 kΩ typical.

GPIO selectable status outputs (GPO) are push-pull and do not require any external pull-up or pull-down resistors. Additional details are available in the “Fifth Generation DSPLL Clock Generator Reference Manual”.

Table 17. General Purpose Input or Output

Function	Description
GPIO Selectable Control Inputs (GPI)	
FINC	DCO frequency increment.
FDEC	DCO frequency decrement.
OE0-OE1	Output enable for specific outputs or group of outputs as defined by the grouping assigned in CBPro.
GPIO Selectable Status Outputs (GPO)	
REF_LOS	Loss of signal at XA/XB or XO_IN pins.
INTR	Interrupt pin for the device. Programmable Boolean combination of PLL_LOL, REF_LOS
Serial Interface (I^2C/SPI)	
A1/SDO	A1/SDO of serial interface. Assignable to GPIO3 only.
A0/CSb	A0/CSb of serial interface.
SDA/SDIO	SDA/SDIO of serial interface.
SCLK	SCLK of serial interface.

Table 18. GPIO Functions for External Flash

Pin	Name	SPI for Flash Control
15	GPIO0	FSDI – Data in from Flash
16	GPIO1	FSDO – Data out to Flash
17	GPIO2	FSCLK – Clock output to Flash
39	GPIO3	FCSB – Chip select

5.6.1. Device Initialization and Reset

Once power is applied, the device begins an initialization period where it downloads preconfigured register values and configuration data from NVM and performs other initialization tasks. Communication with the device through the serial interface is possible once this initialization period is complete. A hard reset is functionally similar to a device power-up. All registers will be restored to the values stored in NVM, and all circuits will be restored to their initial state including the serial interface. A hard reset is initiated using the RSTb pin or by API command. The global soft reset API restarts all PLLs without updating register values. Output clocks do not toggle in either type of reset.

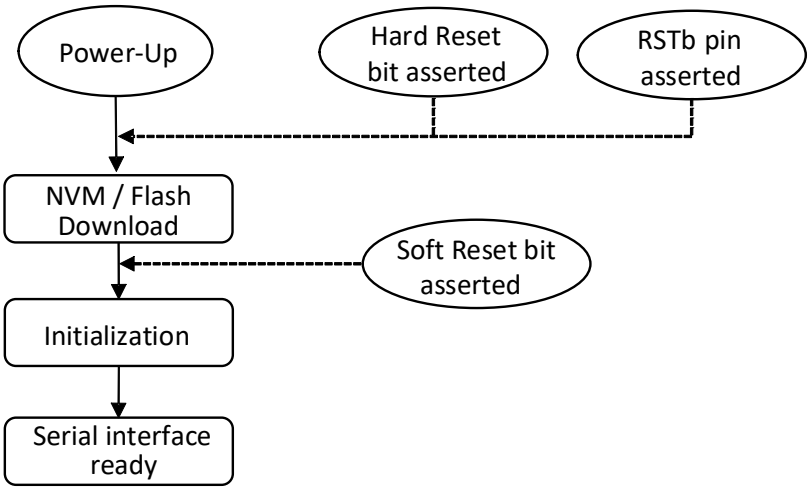


Figure 11. Modes of Operation

5.6.2. Locked Mode

Once locked, the PLL generates clock outputs that are frequency- and phase-locked to the input. Any frequency or phase variation on the input also appears on the outputs. This includes thermal drift of XO or XTAL inputs.

5.7. Status and Alarms

The SKY62101 has monitors for the PLL and input/output clocks. See the "Fifth Generation DSPLL Clock Generator Reference Manual" for more information.

5.7.1. Interrupt Status

The interrupt flag is asserted when any of the status indicators of the device changes state. The interrupt status may be assigned a GPIO pin, or it may be checked using an API command to show which status indicator caused the interrupt to be asserted.

The Interrupt Pin page in CBPro lists all the status indicators that can be programmed to activate the interrupt pin.

The status indicators that are enabled are logically ORed together so that the assertion of any of these status indicators cause the interrupt pin to assert. The interrupt pin status depends on the sticky versions of the individual status indicators, so the interrupt pin stays asserted until the sticky status indicators are cleared.

5.8. Serial Interface

Configuration and operation of the SKY62101 is controlled by reading and writing API commands using the I^2C or SPI interface. The SPI mode operates in either 4- or 3-wire mode. Table 19 below defines the GPIO pins assigned to the SPI port. For more information, see "AN1360: Serial Communications and API Programming Guide for Si536x, Si540x, and Si55xx Devices".

Table 19. Serial Interface Pins

Pin Number	3-Wire SPI	4-Wire SPI	I^2C
41	CSb	CSb	A0
37	SDIO	SDI	SDA
38	SCLK	SCLK	SCK
42	Unused	SDO	A1

5.9. NVM Programming and External Flash Support

Upon power-up, the device downloads its default configuration and settings either from an internal non-volatile memory (NVM) or from external Flash. This option is settable during device configuration in CBPro.

If the NVM option is selected, the internal NVM can be preprogrammed at the factory with a custom frequency plan such that the device starts generating clocks on its first power-up. The NVM can also be programmed in the field using the API command set. NVM programming must be done with VDDA set to 3.3 V.

If the Flash option is selected, the device starts with the frequency plan stored externally. This option is useful for customers who want the flexibility to modify the boot-up configuration in the field. For more details on NVM or Flash programming, refer to "AN1360: Serial Communications and API Programming Guide for Si536x, Si540x, and Si55xx Devices" and the "Fifth Generation DSPLL Clock Generator Reference Manual".

5.10. Application Programming Interface API

Communication between the customer's host processor and the SKY62101 internal microcontroller (MCU) is accomplished through the serial interface. The SKY62101 MCU contains API firmware that allows users simple command-level access to the device registers. For more details on the Device API and for instructions on programming the clock device, see "AN1360: Serial Communications and API Programming Guide for Si536x, Si540x, and Si55xx Devices" and the "Fifth Generation DSPLL Clock Generator Reference Manual".

5.11. Power Supplies

The SKY62101 has 11 power supply pins. The separate power supplies are used for different functions, providing power locally where it is needed on the die to improve isolation. When no outputs are enabled for a particular VDDOx, that supply pin may be left unconnected. For more details on power management and filtering recommendations, refer to the "Fifth Generation DSPLL Clock Generator Reference Manual".

5.11.1. Power Supply Sequencing

There are no power sequencing requirements between supplies. VDDA and VDD18 should be powered up before releasing RSTb. VDDA must be equal to the highest voltage supply.

5.11.2. Power Supply Ramp Rate

Power supply ramp times must stay within the maximum supply voltage ramp rate as defined in Table 8, "DC Characteristics," on page 13.

5.11.3. Low-Power Mode

In Low-Power Mode, the analog core supply voltage (VDDA) of the SKY62101 is set to 1.8 V in order to reduce power consumption. Since VDDA must be equal to the highest voltage applied to the SKY62101, in Low-Power Mode, all voltage supplies including VDDO must be 1.8 V. A 1.8 V VDDO restricts the output format to S-LVDS, LVCMOS, or HCSL. If standard LVPECL / LVDS common-mode voltages are required, Low-Power Mode cannot be used.

NVM programming in the field is not supported in Low-Power Mode since NVM programming requires VDDA to be 3.3 V. Refer to the "Fifth Generation DSPLL Clock Generator Reference Manual" for VDDXO and XO/XTAL connections and terminations for Low-Power Mode.

6. Package Handling Information

Since the device package is sensitive to moisture absorption, it is baked and vacuum packed before shipping. Instructions on the shipping container label regarding exposure to moisture after the container seal is broken must be followed. Otherwise, problems related to moisture absorption may occur when the part is subjected to high temperatures during solder assembly.

The SKY62101 can be used for lead or lead-free soldering. For additional information, refer to Skyworks application note, "PCB Design and SMT Assembly/Rework Guidelines".

Care must be taken when attaching this product, whether it is done manually or in a production solder reflow environment. Refer to Standard SMT Reflow Profiles per JEDEC Standard J-STD-020.

6.1. Package Outline

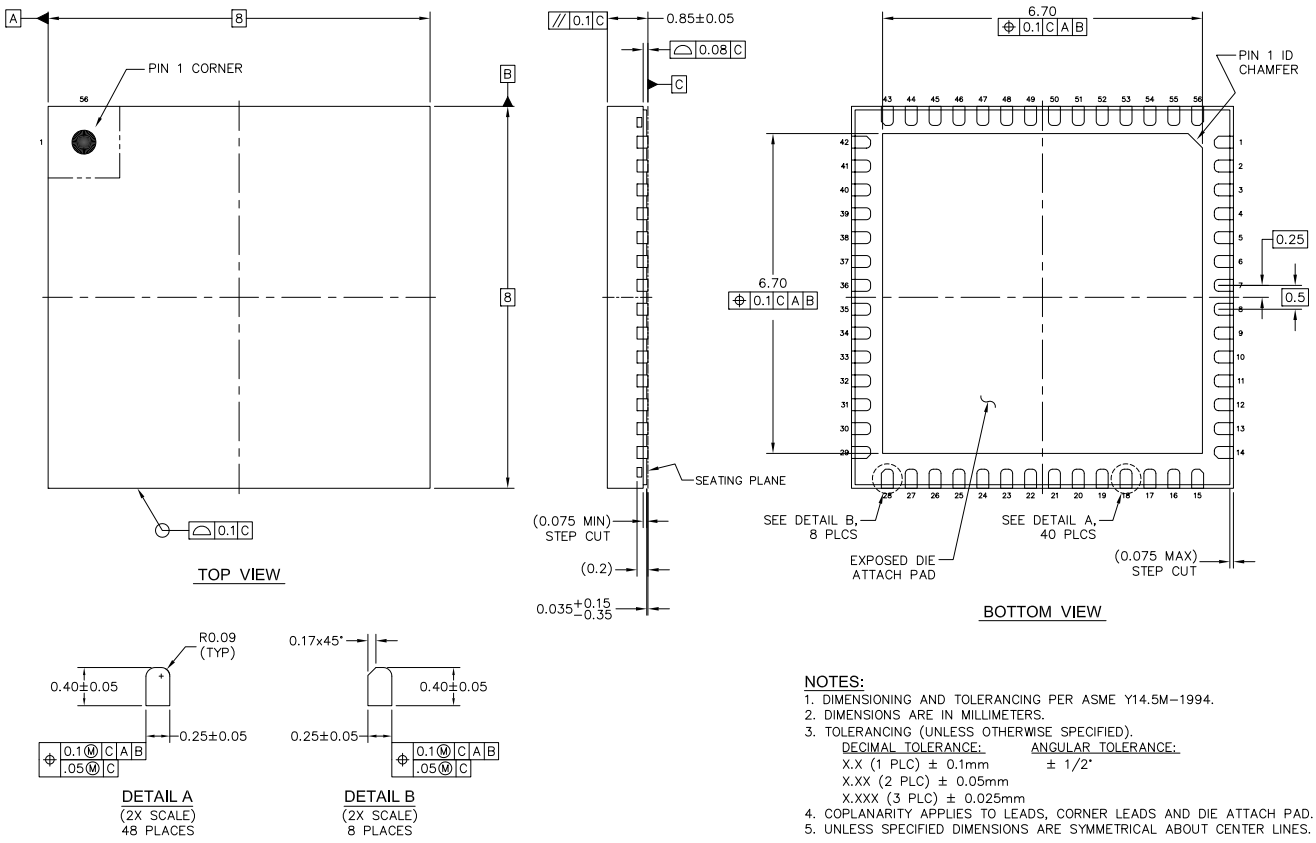


Figure 12. 56-QFN 8x8 mm Package Dimensions

6.2. PCB Layout Footprint

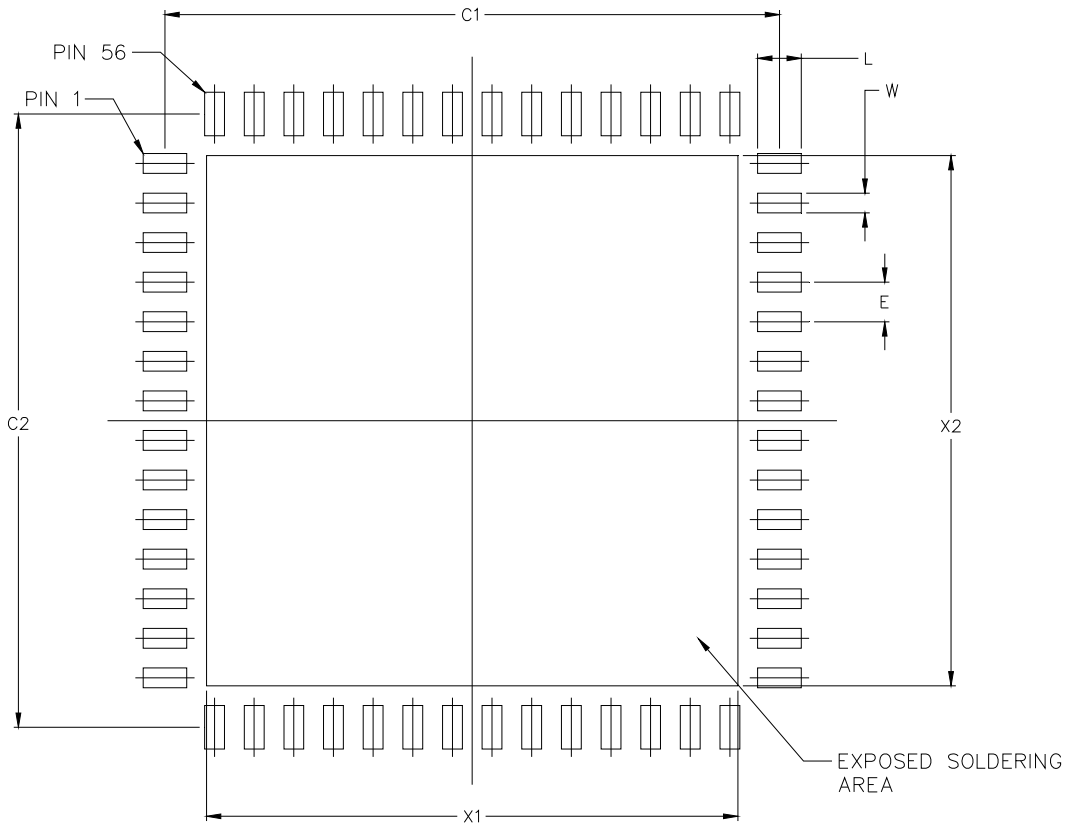


Figure 13. 56-QFN 8x8 mm PCB Layout Footprint

Table 20. PCB Layout Footprint Dimensions

Dimension	mm	Notes
C1	7.75	**General** 1. These notes and stencil design are shared as recommendations only. A customer or user may find it necessary to use different parameters and fine-tune their SMT process as required for their application and tooling. 2. All dimensions shown are in millimeters (mm). 3. This Land Pattern Design is based on the IPC-7351 guidelines. 4. All dimensions shown are at Maximum Material Condition (MMC). Least Material Condition (LMC) is calculated based on a fabrication allowance of 0.05 mm. **Solder Mask Design** 1. All metal pads are to be non-solder mask defined (NSMD). Clearance between the solder mask and the metal pad is to be 60 µm minimum, all the way around the pad. **Stencil Design** 1. A stainless-steel, laser-cut and electro-polished stencil with trapezoidal walls should be used to assure good solder paste release. 2. The stencil thickness should be 0.125 mm (5 mils). 3. The ratio of stencil aperture to land pad size should be 1:1 for all pads. 4. A 4 x 4 array of 1.45 mm square openings on a 2.00 mm pitch should be used for the center ground pad. **Card Assembly** 1. A No-Clean, Type-3 solder paste is recommended. 2. The recommended card reflow profile is per the JEDEC/IPC J-STD-020 specification for small body components.
C2	7.75	
E	0.5	
L	0.55	
W	0.25	
X1	6.7	
X2	6.7	

7. Top Marking

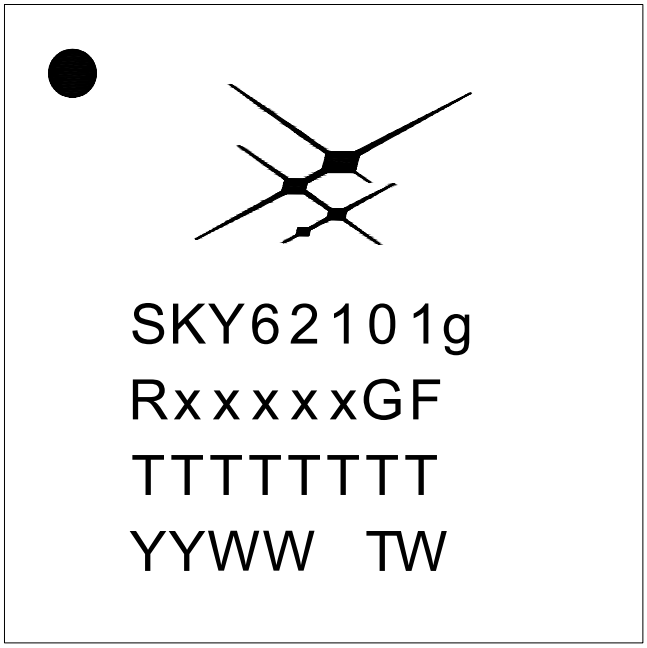


Figure 14. Top Marking

Table 21. Top Marking Explanation

Line	Characters	Description
1	Circle with 0.6 mm diameter	Pin 1 indicator; left-justified.
	SKY62101G	Base part number and device grade: G = device grade. See "8. Ordering Information" on page 36 for latest device grade information.
2	RxxxxxGF	R = product revision. See "8. Ordering Information" on page 36 for latest revision. xxxxx = customer-specific sequence number. Optional boot-configuration code assigned for custom, factory-programmed devices. Characters are not included for standard, factory-default-configured devices. See "8. Ordering Information" on page 36 for more information. GF = package (wettable flank QFN) and temperature range (–40 to +95 °C).
3	TTTTTTTT	TTTTTTTT = manufacturing trace code.
4	YYWW	YYWW = Year (YY) and Week (WW) of package assembly.
	TW	TW = Taiwan; Country of origin (ISO abbreviation).

8. Ordering Information

Table 22. Ordering Part Numbers

Ordering Part Number (OPN)[1]	Frequency Synthesis Mode	Max Differential Output Frequency	Internal NVM/ External Flash	Interface	Package	Temperature Range
SKY62101A-A-GF	Integer and fractional	3200 MHz	Internal NVM	SPI 4-wire	56-lead wettable-flank QFN 8x8 mm	–40 to 95 °C ambient –40 to 105 °C board
SKY62101AAxxxxxGF	Integer and fractional	3200 MHz	Internal NVM	SPI 4-wire or 3-wire or I^2C	56-lead wettable-flank QFN 8x8 mm	–40 to 95 °C ambient –40 to 105 °C board
SKY62101BAxxxxxGF	Integer and fractional	650 MHz	Internal NVM	SPI 4-wire or 3-wire or I^2C	56-lead wettable-flank QFN 8x8 mm	–40 to 95 °C ambient –40 to 105 °C board
SKY62101CAxxxxx-GF	Integer only	3200 MHz	Internal NVM	SPI 4-wire or 3-wire or I^2C	56-lead wettable-flank QFN 8x8 mm	–40 to 95 °C ambient –40 to 105 °C board
SKY62101DAxxxxxGF	Integer only	650 MHz	Internal NVM	SPI 4-wire or 3-wire or I^2C	56-lead wettable-flank QFN 8x8 mm	–40 to 95 °C ambient –40 to 105 °C board
SKY62101E-A-GF	Integer and fractional	3200 MHz	External Flash	SPI 4-wire	56-lead wettable-flank QFN 8x8 mm	–40 to 95 °C ambient –40 to 105 °C board
SKY62101EAxxxxxGF	Integer and fractional	3200 MHz	External Flash	SPI 4-wire or 3-wire or I^2C	56-lead wettable-flank QFN 8x8 mm	–40 to 95 °C ambient –40 to 105 °C board
SKY62101FAxxxxxGF	Integer and fractional	650 MHz	External Flash	SPI 4-wire or 3-wire or I^2C	56-lead wettable-flank QFN 8x8 mm	–40 to 95 °C ambient –40 to 105 °C board
SKY62101GAxxxxxGF	Integer only	3200 MHz	External Flash	SPI 4-wire or 3-wire or I^2C	56-lead Wettable-Flank QFN 8x8 mm	–40 to 95 °C ambient –40 to 105 °C board
SKY62101HAxxxxx-GF	Integer only	650 MHz	External Flash	SPI 4-wire or 3-wire or I^2C	56-lead Wettable-Flank QFN 8x8 mm	–40 to 95 °C ambient –40 to 105 °C board
SKY62101AA-EVB[2]	Integer and fractional	3200 MHz	Internal NVM (External Flash)	SPI 4-wire	Evaluation board	—

1. The blank parts, SKY62101A-A-GF and SKY62101D-A-GF, are preconfigured to be a 4-wire interface. For Factory programmed plans and blank parts requiring other interface standards like I^2C and 3-wire, custom part numbers (Axxxxx) are created using CBPro.
2. The SKY62101AA-EVB is supported by the Pluto evaluation platform. See the Pluto evaluation platform user guide for more information.

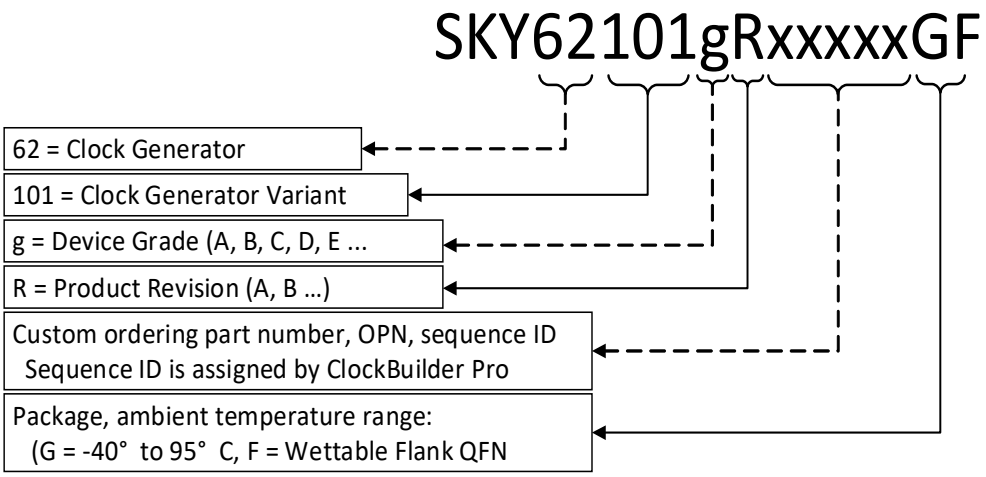


Figure 15. Ordering Guide Key

9. Revision History

Revision	Date	Description
A	June, 2025	Initial release.