APPLICATION NOTE

AN1214: Advanced Device Protection for the Si834x Isolated Smart Switch

Description

This application note describes the performance of the Si834x Isolated Smart Switch during surge events and the protection circuitry necessary to achieve compliance with applicable Zone B requirements as described in the IEC 61131-2 standard for programmable controllers.

The Si834x family of Isolated Smart Switches provide high current drive capability in a high-side (sourcing) or low-side (sinking) configuration. These switches are ideal for driving resistive and inductive loads such as solenoids, relays, and incandescent lamps commonly found in industrial environments. Output circuits in programmable logic controllers (PLCs) can be routinely subjected to adverse conditions such as high temperature, noisy buses, and unpredictable electrical events. Lightning surges are common culprits for inducing stress or failure in industrial electronic systems. This application note will explain the test method, results, and design considerations for the Si834x with respect to the IEC 61000-4-5 surge test specification.

All testing described in this document was completed using the Si834x Smart Switch Evaluation Kit. Schematic and layout files for the evaluation kit can be found in “7. Appendix A—Si834x Evaluation Board Schematic and Layout Files” on page 16. A complete guide on how to use the evaluation kit can be found in "UG390: Si834x-EVB User's Guide".

For more information on the Si834x family of products, please refer to the Si834x Data Sheet. For more information on advanced load-driving characteristics and application information, please refer to “AN1212: Advanced Load Driving Considerations for the Si834x Isolated Smart Switch”.

Visit the web site of the International Electrotechnical Commission for more information on standards IEC 61131-2 and IEC 61000-4-5.

Key Features

- Si834x product overview
- Breakdown of IEC 61131-2 and IEC 61000-4-5 standards
- Explanation of test procedure, test cases, and test results
- Si834x Evaluation Board schematic and layout files

1. Summary of Results

The table below summarizes the results of surge testing on the Si834x. For test cases involving one or more output channels, arbitrary identifiers Bn and Bo are used to indicate any channel and any other channel, respectively. For part numbers with more than one output channel, all channels were tested for compliance. For more information on how these results were obtained, refer to “2. Understanding the Si834x Isolated Smart Switch” on page 3, “3. Si834x Evaluation Board” on page 5, and “4. Relevant Standards and Test Setup” on page 10.

Table 1. Test Results for IEC 61000-4-5 Surge Test for Si834x

Pin Combination	Test Case	Surge Level	Result
VDD2 to GND2	—	±1 kV	Pass
VDD2 to GND1	—	±1 kV	Pass
GND2 to GND1	—	±1 kV	Pass
Bn to VDD2	Channel OFF	±1 kV	Pass
	Channel ON		
Bn to GND2	Channel OFF	±1 kV	Pass
	Channel ON		
Bn to GND1	Channel OFF	±1 kV	Pass
	Channel ON		
Bn to Bo	Both channels OFF	±1 kV	Pass
	Both channels ON		
	1 channel ON, 1 channel OFF		

2. Understanding the Si834x Isolated Smart Switch

The Si834x family of Isolated Smart Switches provide high current drive in sourcing and sinking configurations. Its robust design, dense form factor, and intelligent safety features make it an excellent choice for designers of industrial automation systems, programmable logic controllers (PLC), and any 12–32 V application that prioritizes safety and reliability.

One of the benefits of the Si834x that sets it apart from the competition is an advanced protection and diagnostics reporting system. The device contains built-in protection from overload conditions, short-circuits, over-temperature events, inductive kickback, communication failures, and more. It also provides diagnostics reporting on open-circuit status, supply undervoltage, supply out-of-spec events, and all the aforementioned conditions.

A system designer can incorporate these diagnostics into their controller to provide rapid response to potentially hazardous failures.

It is important to understand the internal structures that source and sink current through the output channels (Bn) during normal operation because these same devices form the primary internal protection mechanisms against surge and other electrical stress the device may experience.

2.1. Output Configurations

The Si834x product family contains a wide variety of selectable output configurations including sourcing switch, sinking switch, and one, two, or four separate channels for driving IEC 61131-2 rated loads of 2 A, 1 A, and 500 mA, respectively. Sourcing devices (part numbers beginning with Si8340) are comprised of a high-side switch (driver) and an innovative “smart” multi-voltage demagnetization clamp in parallel with the load to provide fast, efficient, and robust demagnetization of inductive loads during turn-off. Sinking devices (part numbers beginning with Si8341) are comprised of a low-side switch and the same smart clamp in parallel with the load, which clamps between the channel output Bn and VDD2. The following figures show diagrams of these devices.

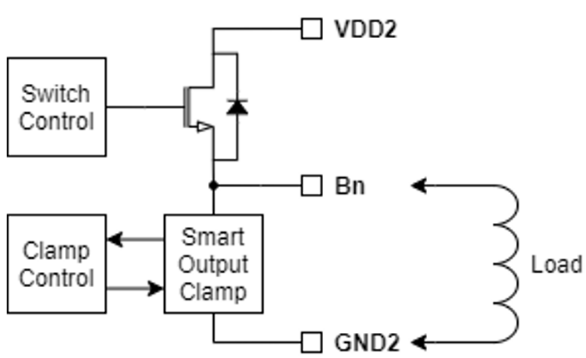


Figure 1. Si834x Sourcing Device

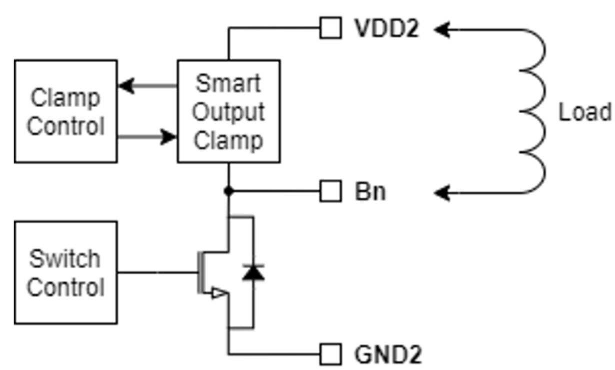


Figure 2. Si834x Sinking Device

During normal operation, the switch will close when the channel is turned ON from the input side. In sourcing systems, the switch will provide a low-resistance path from VDD2 to the load. In sinking systems, the switch will provide a low-resistance path from the load to GND2, enabling current flow and charging inductive loads. When the channel is turned off, the return path for inductor current is cut off, inducing a voltage kickback that is subsequently clamped by the Smart Output Clamp.

2.2. Current Paths

Due to architectural differences between sourcing and sinking parts, different internal devices will be conducting current for identical test cases from the IEC 61000-4-5 surge test specification. For example, a differential mode (DM) surge with positive polarity applied between the Bn and GND2 lines will forward bias the body diode of the sourcing switch. In contrast, the same surge applied to the sinking device will engage the smart clamp and conduct current through this device to the VDD2 supply capacitance and return through GND2 to the source of the surge.

As a result, it is imperative to test all viable surge cases within the requirements set forth in the IEC 61000-4-5 spec, including but not limited to: all output pin combinations, switch configurations, switch modes, and channel load ratings. Implementing test coverage for each of these test cases guarantees within reason that the worst-case scenarios be measured and understood, and that adequate external protection be incorporated into the design.

2.3. Surge Protection for the Si834x

As with all Skyworks' Si8xxx isolator products, the Si834x contains proprietary silicon dioxide isolation capacitors that form a galvanic isolation barrier between input side and output side. This barrier is rated for 1500 Vrms of isolation and protects sensitive circuitry from potentially hazardous electrical surges on the field side. For common mode (CM) surges (see "4.3. Protective Earth (PE) Ground and Test Modes" on page 12), this isolation barrier provides sufficient protection assuming that the input side is grounded to Earth GND. Depending on the classification of the PLC ports in the designer's system, the integrated isolation barrier may be adequate protection from surges.

However, many port definitions and system designs will require that the PLC output channels be able to survive differential mode surges. Differential mode surges can affect the Si834x output pins through the power supply rail or one of the output channels as shown in Figure 3 below. Surges of this nature require external protection circuitry to steer current away from the device and absorb energy.

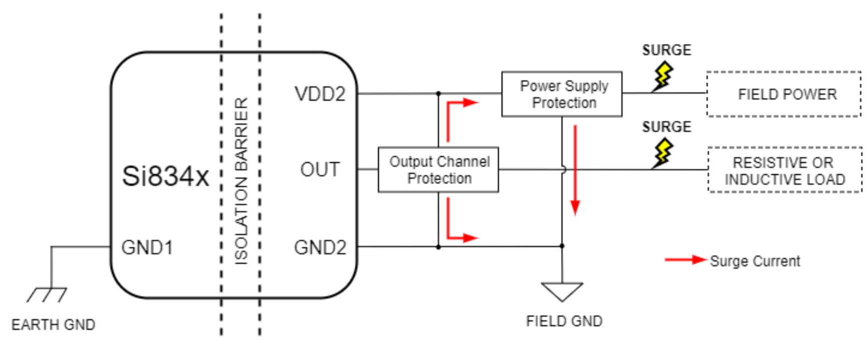


Figure 3. Diagram of External Surge Protection for Si834x

The Power Supply Protection and Output Channel Protection blocks serve as external protection for the Si834x. Surge currents incident on the VDD2 supply rail will travel through the supply protection block before reaching the device. Clamping devices prevent the supply voltage from reaching dangerous levels and dissipate energy from the surge. Likewise, the channel protection block will steer current to VDD2 or GND2 and absorb excess energy from the surge, protecting the output channels and preventing overload conditions from occurring. Without these protection blocks, high voltage differential mode surges could damage the internal devices of the Si834x and result in a failure to meet IEC 61131-2 safety standards. Therefore, it is essential to understand the requirements of the PLC system being designed and the location and purpose of protection circuits on the output side of the Si834x.

3. Si834x Evaluation Board

The testing described in this document was performed on the Si834xSRC-EVB Rev 4.0 and Si834xSNK-EVB Rev 4.0 evaluation boards. Partial schematics for these boards can be found in “3.1. Power Supply Protection” on page 6 and “3.2. External Channel Protection” on page 7. For complete schematic and layout diagrams, see “7. Appendix A—Si834x Evaluation Board Schematic and Layout Files” on page 16.

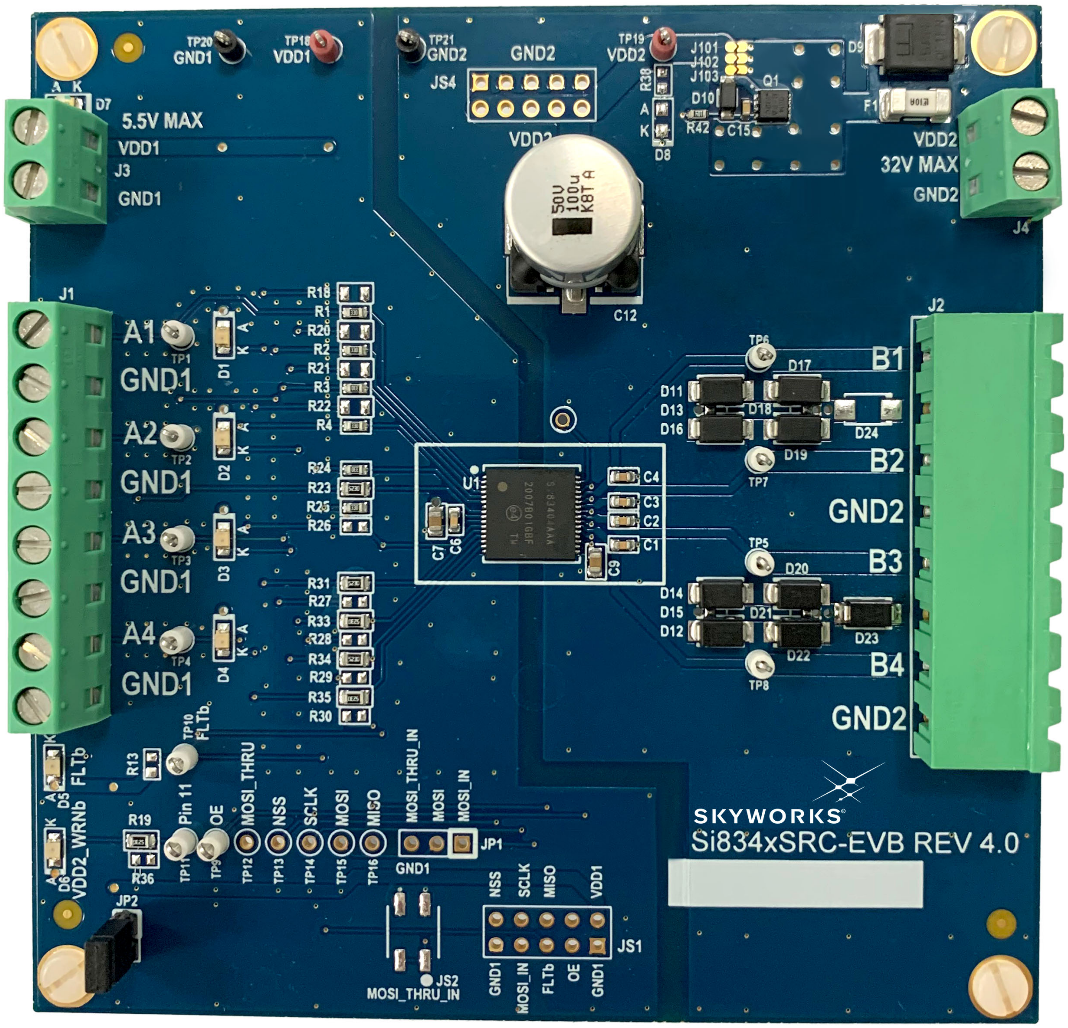


Figure 4. Si834x Evaluation Kit

The purpose of the evaluation board is to provide the user with an easy-to-use platform for evaluation of the Si834x device, and it includes input and output terminals, power supply terminals, LED indicators, and more.

When performing EMC tests such as surge testing, it is recommended to use the Si83404AAA-IF part number for sourcing (high-side) configuration and the Si83414AAA-IF for sinking (low-side) configuration. These parts have parallel inputs that receive hi/lo digital signals to activate and deactivate outputs. This is generally the easiest way to control the device state when using large test setups with high-voltage equipment and facilitates quick functionality verification for establishing passing or failing test cases. The SPI-enabled input devices may also be used if the user has access to a laptop or PC with which to control the device. More information on the operation and usage instructions for the EVB can be found in UG390: Si834x-EVB User’s Guide.

3.1. Power Supply Protection

The Si834x Rev 4.0 EVBs feature two circuit blocks of primary external protection from surge and other dangerous electrical transients. The schematic in the figure below shows the recommended power supply protection block. It consists of a fuse, diode-connected PMOS, and bidirectional TVS clamp among other components and is identical for both sourcing and sinking configurations.

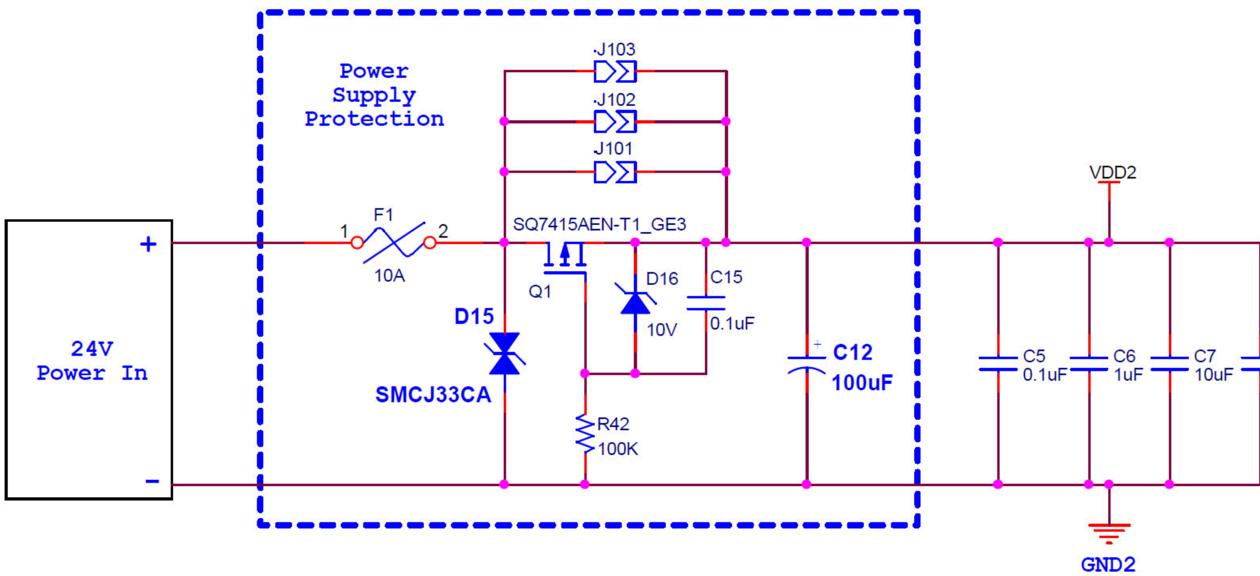


Figure 5. External Protection for Power Supply

The power supply protection block has several purposes: to suppress hazardous transient signals such as surges, to protect the Si834x (and other components powered by the VDD2 supply) from overload conditions, and to protect the system if the power (VDD2) and ground (GND2) pins were to be reversed. The components selected for this circuit have been extensively tested and verified in an application environment.

The fuse F1 does not provide protection against surge events, and its primary purpose is to open the current path between the power supply and field circuitry in the event of an overload condition or reverse bias condition. The combination of Q1, D16, C15, and R42 acts as a reverse bias protection circuit for low-voltage reverse power supply conditions. At higher voltages, D15 will clamp the supply voltage until the fuse F1 opens. The PMOSFET is oriented such that the drain-to-source body diode will be forward biased when a positive voltage is applied to VDD2 (as in normal operation). Once current begins to flow through Q1, V_{GS} will drop below $–V_{TH}$, pushing the MOSFET into saturation and turning the channel on. This serves as robust conduction path and preserves the VDD2 voltage with a low on-resistance (R_{ON}). The Zener diode, D16, protects the PMOS by clamping V_{GS} at –10 V. R42 pulls the PMOS gate to GND2 and provides bias current to D16, and C15 acts as a LPF on the supply line. J101, J102, and J103 are solder bumps that may be used to short out the reverse protection circuit if it is not desired.

The primary protection mechanisms against surge and high-voltage transients are D15 and C12. The SMCJ33CA bidirectional TVS diode clamps the voltage between VDD2 and GND2 at 33 V, protecting the Si834x Isolated Smart Switch (max of 32 V) and any other components sourced by this supply. The bulk capacitor C12 acts as a secondary protection mechanism by resisting a change in voltage across the supply pins. During a surge between VDD2 and GND2, the voltage across this capacitor will change by Q_{surge}/C_{bulk}. Therefore, larger bulk capacitors will be able to sustain a larger surge current (and thus higher surge voltage level) for a given change in voltage. It is recommended to use a 100 µF electrolytic capacitor, but only the system designer can determine the optimal type and value of capacitance to provide for the system. Note that the fuse rating and VDD2 ramp rate will impose restrictions on maximum capacitance. Capacitors C5–C8 are standard ceramic bypass capacitors. When both D15 and C12 are included in the design, these components will work in tandem to suppress an overvoltage on VDD2 and provide the best protection against power supply surges.

Table 2. Bill of Materials for Power Supply Protection Circuit

Reference Designator(s)	Component Type	Manufacturer PN	Manufacturer	PCB Footprint
C12	Electrolytic Capacitor	MAL216099101E3	Vishay	C12.5X12.5MM-4N
C15	Ceramic Capacitor	C0603X7R500-104K	Venkel	C0603
D15	Bidirectional TVS Diode	SMJC33CA	Littelfuse	DO-214AB
D16	Zener Diode	MMSZ4697T1G	On Semi	DO-214AC
F1	Fuse	0453 010	Littelfuse	FUSE-453
J101, J102, J103	Solder Bumps	—	—	—
Q1	PMOSFET	SQ7415AEN-T1_GE3	Vishay	Power33
R42	Resistor	CR0603-16W-104J	Venkel	R0603

3.2. External Channel Protection

The second circuit block recommended for protection against surge events is shown in Figure 6, “External Channel Protection for Sourcing OPNs,” on page 8. This circuit block is designed to protect the output ports of the Si834x. When paired with the power supply protection circuit, these external components will provide comprehensive protection from common mode and differential mode surge events under Zone B requirements.

The channel protection circuit consists of two primary components: rectifying diodes (D3–D14) and TVS diodes (D1–D2). In general, the protection circuits on the high side and low side of each configuration are intended to mimic the behavior of the internal multi-voltage clamp and output switch body diodes connected to the same nodes. All tests in this document were performed with a single TVS diode, but an additional socket was added to the board design to allow for redundancy. The BAV23C and BAV23A are smaller, dual diode packages that were validated as viable substitutions for the ES1B rectifying diodes in all surge test cases. While the BAV23 diodes consume less board space, they are also rated for lower peak surge current than the ES1B and therefore provide less margin than the ES1B for passing surge tests. If D3–D10 are populated with ES1B diodes, then there is no need to populate BAV23A or BAV23C at D11– D14 (and vice versa). Note the sourcing and sinking protection circuits have slightly different designs.

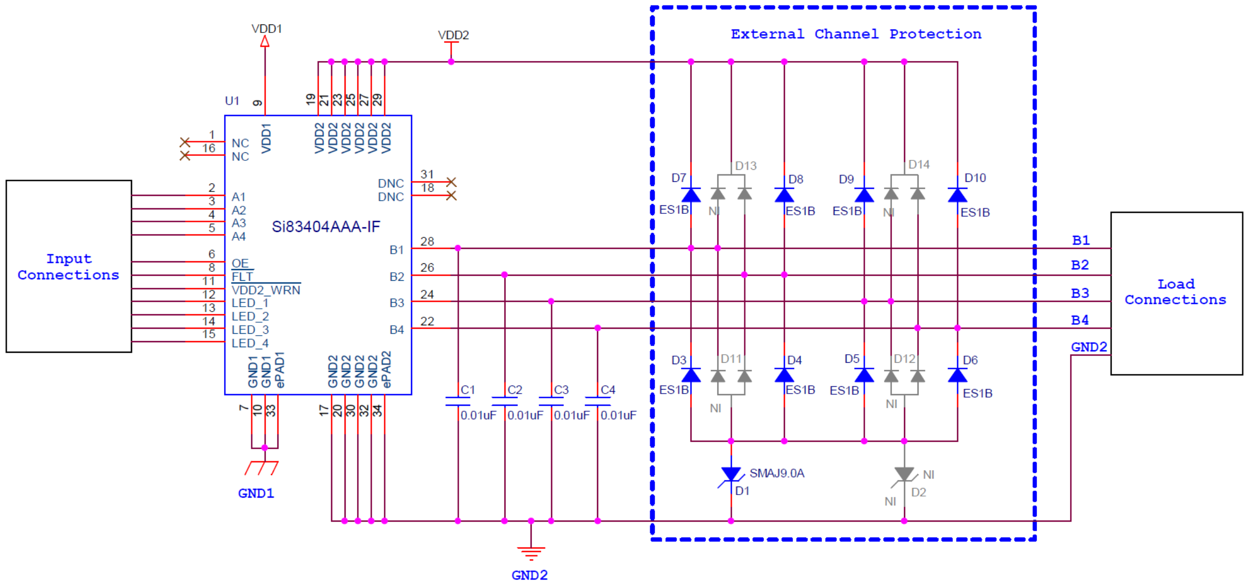


Figure 6. External Channel Protection for Sourcing OPNs

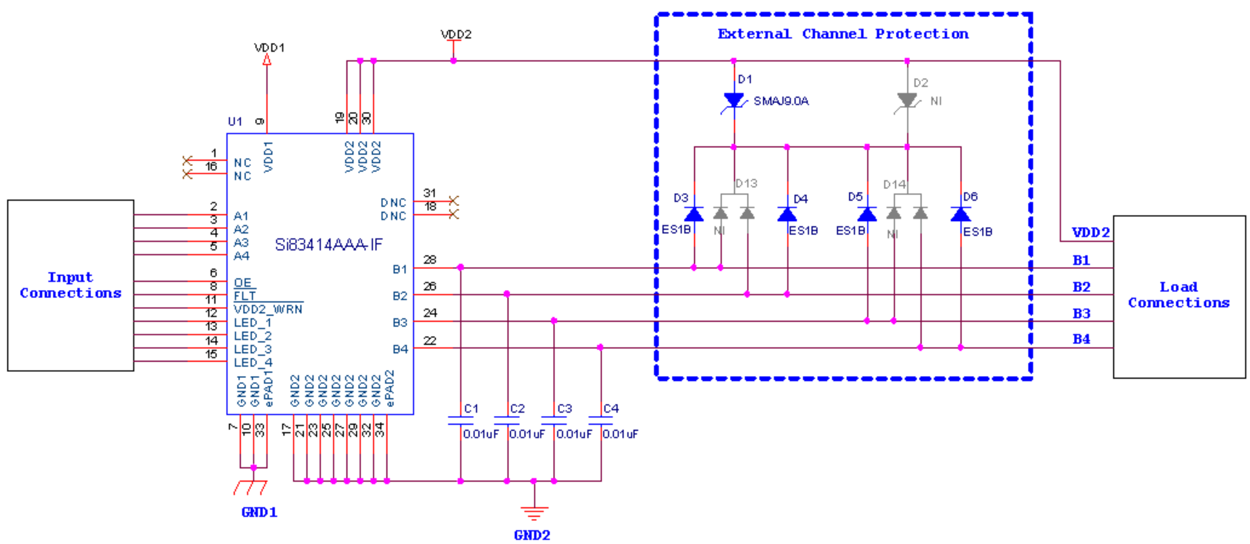


Figure 7. External Channel Protection for Sinking OPNs

For sourcing parts, a combination of rectifying diode and TVS diode is placed in parallel with the internal multi-voltage clamp to GND2, and a single rectifying diode is placed in parallel with the output switch body diode to VDD2. These external components form a separate current path to steer surge currents away from the Si834x device during line-to-line surge events. During a negative surge voltage on a channel Bn, the internal multi-voltage clamp will engage in high-voltage mode V_{CLMPH}, clamping at approximately –17.5 V. Simultaneously, the combination of ES1B and SMAJ9.0A will clamp the output channel to GND2 at approximately 12 V to 16 V ($V_{F,ES1B}$ + $V_{CLMP,SMAJ9}$). As a result, much of the surge current will be steered through the external clamping circuit. This greatly reduces the stress on the internal multi-voltage clamp and improves surge performance.

During a positive surge, the ES1B rectifying diode will clamp at a forward voltage of about $V_{F,ES1B}$ = 0.92 V. This will provide an alternative current path from the output switch body diode and reduce stress on the silicon die. These external current paths also divert surge current during line-to-line surges between output channels (e.g., B1 and B2).

For sinking parts, the rectifying diode and TVS diode form a path between output channel and VDD2, while the single rectifying diodes are not required for protection between channel and GND2. During positive surge voltages on the output channel, the internal multi-voltage clamp will enter high-voltage mode (V_{CLMPH} = –17.5 V), and the external protection circuit will clamp around –12 V to –16 V. During negative surge voltages, the switch body diode will forward bias and steer surge current from GND2 to Bn. The combination of external high-side and internal low-side protection on the output channels enables the Si834x to survive differential mode surge currents.

Please note it is important to place the external clamping components as close to the source of the surge as possible. This technique creates a sort of ballast resistance out of the copper traces connecting the output pins of the Si834x to the external clamps. Although most traces will only provide a few hundred milliohms of resistance at most, the voltage drop across this resistance can reach 3 to 5 V during a surge current of 20 A. This additional voltage drop increases the bias across the external clamping components, ensuring that they will conduct as much current as possible during a high-current surge event.

Table 3. Bill of Materials for External Channel Protection Circuits

Reference Designator(s)	Component Type	Manufacturer Part Number	Manufacturer	PCB Footprint
D3 to D10	Rectifying Diode	ES1B	Diodes Inc.	DO-214AC
D1 to D2	TVS Diode	SMAJ9.0A-E3/61	Vishay	DO-214AC
D11 to D12 (Optional Substitution)	Rectifying Diode	BAV23A	Diodes Inc.	SOT23-KKA
D13 to D14 (Optional Substitution)	Rectifying Diode	BAV23C	Diodes Inc.	SOT23-AAK

3.3. Clamping Performance with External Protection

Utilizing external components to protect against surge events can change the way inductive loads demagnetize during normal operation. Extensive testing was performed to validate the performance of the multi-voltage smart clamp with the external circuit shown above. The multi-voltage clamp operates normally during the discharge cycle of an inductive load, and the external clamp shares in the demagnetization current after the clamp switches into high-voltage mode (V_{CLMPH}). All diagnostics, safety mechanisms, and other features operate as intended.

3.4. 2-Channel and 1-Channel Devices

While this document primarily focuses on the protection and surge performance of the four-channel Si834x devices, testing was also conducted on the two-channel and one-channel devices to determine relative performance. The result of this testing led to the conclusion that no external channel protection is required to conform to Zone B requirements for surge testing. This is due to the higher current capability of the devices with lower channel count. However, the power supply protection circuitry presented in “3.1. Power Supply Protection” on page 6 is still recommended to pass surges applied to the power supply pin combination of VDD2 and GND2. The test results reported in “4. Relevant Standards and Test Setup” on page 10 are, therefore, applicable to all product offerings listed in the Ordering Guide of the Si834x Data Sheet.

4. Relevant Standards and Test Setup

Programmable logic controllers (PLC) are the controllers of choice in many industrial applications for their robustness, versatility, and ease of programming. In an effort to promote international uniformity for these devices, the International Electrotechnical Commission (IEC) has developed a series of standards titled IEC 61131-2 that govern the operation, safety, EMC performance, and general specifications for PLCs. PLC vendors use this standard to determine which tests to perform on their system and how to properly execute these tests. In this section, we will interpret the surge requirements set forth in IEC 61131-2 and IEC 61000-4-5 to explain how compliance is achieved with these standards.

4.1. IEC 61131-2 PLC Safety Standard

IEC 61131-2 breaks down the electromagnetic compatibility (EMC) requirements for PLC modules based on the designated factory "zone" of the device as well as the type and purpose of the connections which are being tested. The Si834x output channel pins qualify as Unshielded Unsymmetrical Digital/Analog I/O ports, and the power pins qualify as I/O Power ports. Zones with more severe environments have stricter requirements for EMC testing. These tests include conducted and radiated emissions, electrostatic discharge (ESD), radiofrequency (RF) immunity, electrical fast transients (EFT), and surge. In this document, we will focus on requirements for surge. The following table lists surge requirements based on zone and relevant output type:

Table 4. Surge Test Levels by Zone

Zone	Surge	Performance Criterion
A (DC I/O Power)	0.5 kV CM 0.5 kV DM	B
A (Unshielded Digital/Analog I/O)	None	B
B (DC I/O Power)	0.5 kV CM 0.5 kV DM	B
B (Unshielded Digital/Analog I/O)	1 kV CM	B
C (DC I/O Power)	1 kV CM 1 kV DM	B
C (Unshielded Digital/Analog I/O)	2 kV CM	B

Evaluation of pass or fail is based on the following predetermined performance criteria:

A—PLC system continues to operate as intended with no loss of function or performance.

B—PLC system may experience degradation of performance with no change in operating mode or permanent loss of data, and system must self-recover to normal operation after the test.

C—PLC system may lose function, but no destruction of hardware or software, and must resume normal operation after test automatically or after manual restart.

All surge specifications require the device to pass with performance criterion B. This means that the DUT may temporarily lose normal function during the test (i.e., during the surge or transient event) but must be able to self-recover to normal operation at the conclusion of the test. Damage to the hardware, loss of data, erroneous shutdown, and latch-up are examples of unacceptable responses to the stimulus by the DUT.

The standard specifies further test requirements and conditions for compliance:

- Five surges each in positive and negative polarities
- Minimum repetition rate of one surge per minute
- 42 Ω, 0.5 µF output impedance

These requirements ensure that each surge test case is easily repeatable. Note that the 42 Ω source impedance is typical in most compliant surge machines, while the 0.5 µF capacitance serves as the coupling method. A complete diagram and explanation of the test setup can be found at the end of "4.2. IEC 61000-4-5 Surge Test Specification" on page 11.

4.2. IEC 61000-4-5 Surge Test Specification

Each EMC test has a specification that explains in detail the test requirements, measurement techniques, and procedure. The standardized specifications for surge testing can be found in IEC 61000-4-5. In the spec, the combination waveform generator is used to output a 1.2/50 µs waveform as shown in the image below. This is the standard surge waveform for lightning surge testing of electronic devices in industrial environments and is defined in the image below.

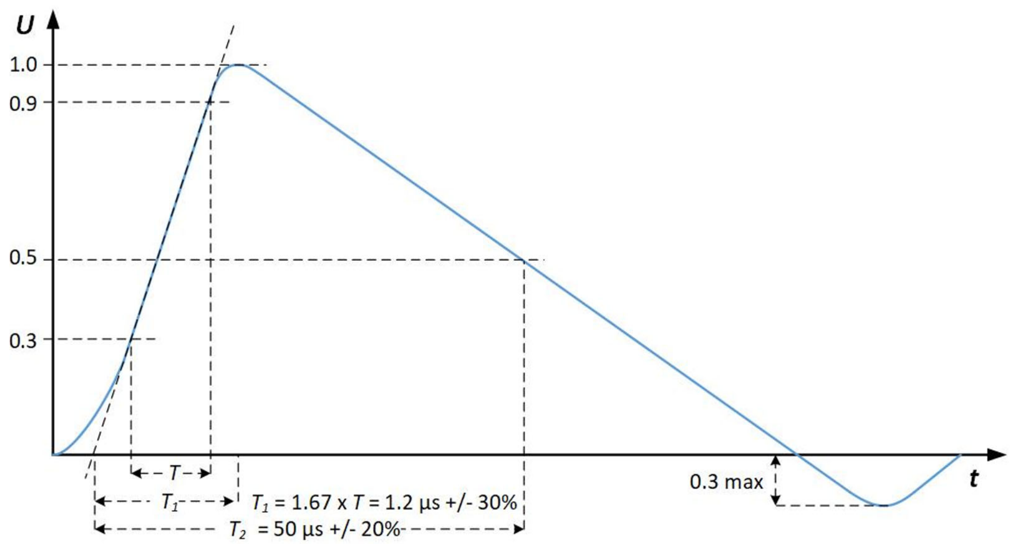


Figure 8. Waveform of Open-Circuit Surge Voltage per IEC 61000-4-5

The open-circuit voltage is measured without the EUT connected and may appear differently when the device is connected. This waveform can be produced using the simplified circuit diagram in the standard document, although it is generally advisable to use certified test equipment. For all surge tests reported in the following section, the EMC Partner MIG2403-1522 was used.

The preferred range of test levels for this test are enumerated in Table 5.

Table 5. Surge Test Levels

Level	Open-Circuit Test Voltage (kV)
1	0.5
2	1.0

Table 5. Surge Test Levels

Level	Open-Circuit Test Voltage (kV)
3	2.0
4	4.0

Using Table 4 on page 10 and Table 5 above, it is clear that lines categorized as Unshielded Digital/Analog I/O in Zone B must pass Test Level 2, while lines categorized as DC I/O Power must pass test level 1. For simplicity, all test cases were conducted at Test Level 2.

4.3. Protective Earth (PE) Ground and Test Modes

In an isolated system, multiple grounds will exist. This leads to the possibility of one ground and all circuits referenced to it experiencing a large potential shift with respect to protective Earth (PE) ground. In surge testing, this is referred to as a common mode (CM) surge, or line-to-ground. In the Si834x application circuit, the isolated or low-voltage ground (GND1) is typically understood to be considered the “safety ground”, or PE ground. However, this is not a requirement of the device but a design choice to the system designer. For that reason, we have taken the least restrictive approach of interpreting either ground (GND1 and GND2) as possible PE grounds.

In other cases, lightning surges can be coupled directly onto a “line” running out of a PLC system. This line will experience a rapid rise in voltage with respect to other lines in the system, resulting in a differential mode (DM) surge, or line-to-line. In this case, the surge voltage is referenced to another line, and PE ground is disconnected from the equipment under test (EUT), or the Si834x evaluation board.

While systems configured to source current will make use of channel (Bn) and ground (GND2) lines running to the load, sinking-configured systems will typically make use of channel (Bn) and power (VDD2) lines. As a result, there is significant overlap in line-to-line and line-to-ground test cases, and some test cases may apply to Digital I/O ports as well as I/O Power ports. Therefore, each possible line combination was tested to the highest test level required of Zone B Digital I/O ports in both CM and DM test modes where applicable. This provides the best coverage of possible test cases, regardless of the system design.

4.4. Test Setup

The IEC 61000-4-5 surge test specification outlines proper test setup for compliance testing. This is to ensure proper repeatability and consistency of test results. The required equipment for the test setup is as follows: equipment under test (EUT), auxiliary equipment (AE, such as power supplies), cables, coupling/decoupling networks, surge generator, protection devices as needed, and a ground reference plane (GRP).

The coupling network for unshielded unsymmetrical interconnection lines for line-to-line and line-to-ground test cases consists of a 40 Ω resistor and 0.5 µF capacitor in series with the surge generator output. The circuit diagram for surge generators calls for 2 Ω of effective series resistance, creating a combined source resistance of 42 Ω which is internal to the Modular Impulse Generator. The coupling capacitor is added externally.

The decoupling network serves to protect the AE from possible damage as a result of the surge impulse and a series inductance of 20 mH on each line connecting to the EUT is recommended.

Finally, the GRP serves as an earth ground source and is used to ground one side of the isolator during common mode test cases. A diagram of the complete test setup is shown in the following figure. Note that the GRP should be 1 m from the ground and that the length of cable from the CDN to EUT should be no greater than 2 m.

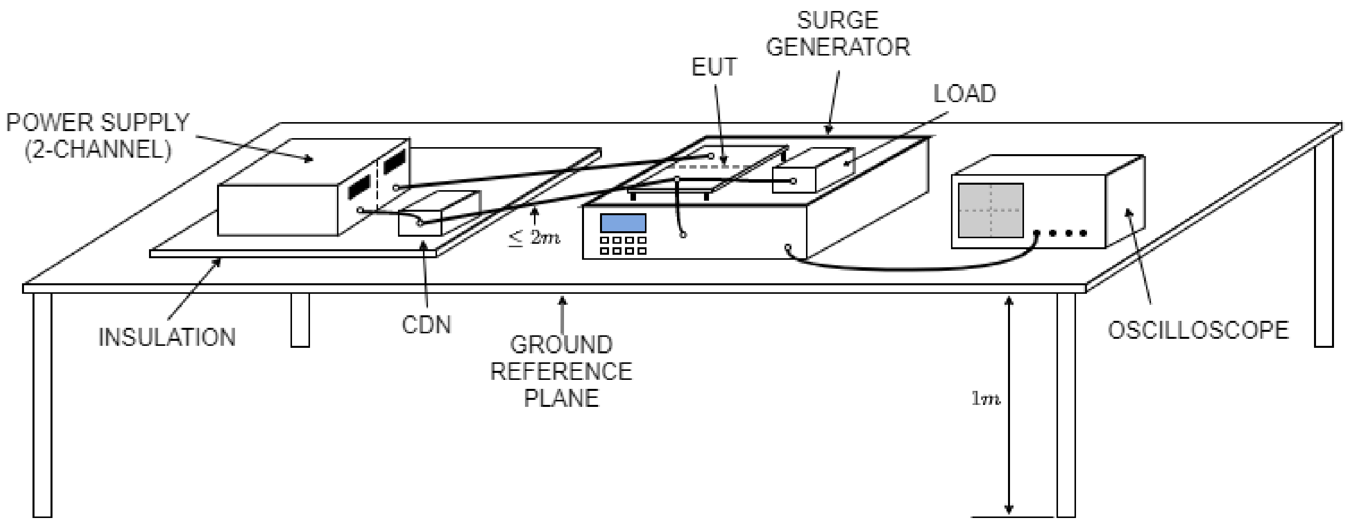


Figure 9. Test Setup for IEC 61000-4-5 Surge Test

5. Test Results

The table below summarizes the results of surge testing on the Si834x. For test cases involving one or more output channels, arbitrary identifiers Bn and Bo are used to indicate any channel and any other channel, respectively. For part numbers with more than one output channel, all channels were tested for compliance.

Table 6. Test Results for IEC 61000-4-5 Surge Test for Si834x

Pin Combination	Test Case	Surge Level	Result
VDD2 to GND2	—	±1 kV	Pass
VDD2 to GND1	—	±1 kV	Pass
GND2 to GND1	—	±1 kV	Pass
Bn to VDD2	Channel OFF	±1 kV	Pass
	Channel ON		
Bn to GND2	Channel OFF	±1 kV	Pass
	Channel ON		
Bn to GND1	Channel OFF	±1 kV	Pass
	Channel ON		
Bn to Bo	Both channels OFF	±1 kV	Pass
	Both channels ON		
	1 channel ON, 1 channel OFF		

The positive and negative voltage waveforms captured during common mode testing can be seen in Figure 10 below. These closely resemble the open-circuit voltage waveform shown in "3.2. External Channel Protection" on page 7 due to the high-impedance nature of the Si834x isolation barrier. The vertical scale in these captures is 2400 V/V.

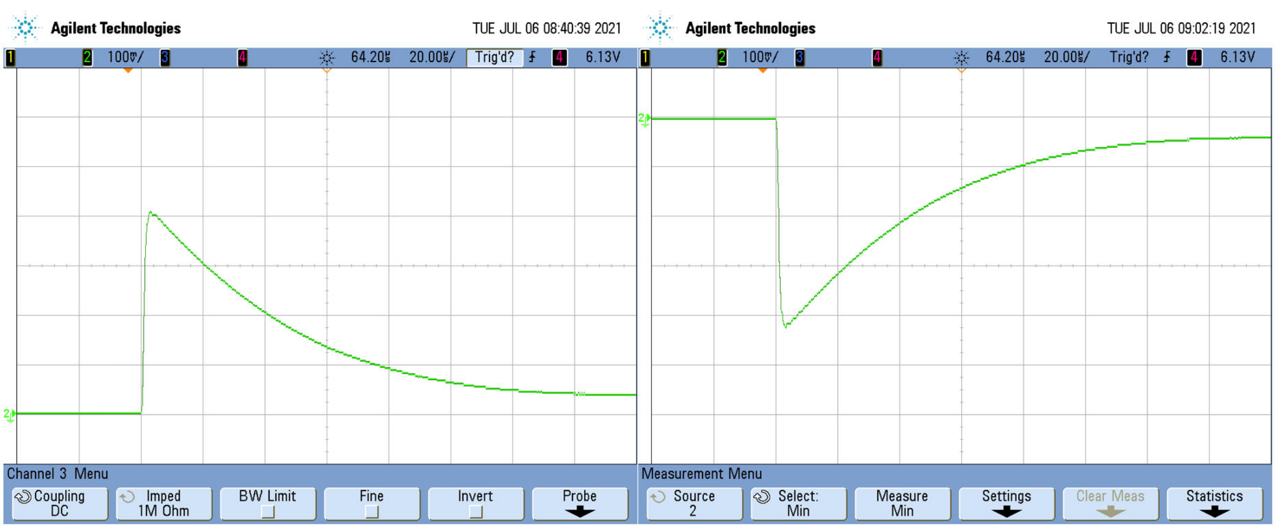


Figure 10. Positive (Left) and Negative (Right) Surge Voltage Waveforms

6. Summary

This application note discussed the motivation for external surge protection for the Si834x family of Isolated Smart Switches. The primary governing standards IEC 61131-2 and IEC 61000-4-5 were explained and translated into a relevant test setup, test procedure, and test cases. Finally, the results for all relevant test cases necessary to prove Zone B compliance for surge protection were delivered. In order to achieve these results, external protection circuits were added to the Si834x output channels and power supply rails. In addition to these external circuits, several recommendations were provided for further improved surge performance including redundant TVS diodes, spacing between the output pins and the external components, and adequate bulk capacitance. For more information on the Si834x Isolated Smart Switch, please refer to the Si834x Data Sheet and "UG390: Si834x-EVB User's Guide".

7. Appendix A—Si834x Evaluation Board Schematic and Layout Files

Following are the schematic and layout files for the Si834x EVBs described in “2. Understanding the Si834x Isolated Smart Switch” on page 3. Note that component designators may differ from the partial schematics and BOMs presented in that section, as those were modified for simplicity.

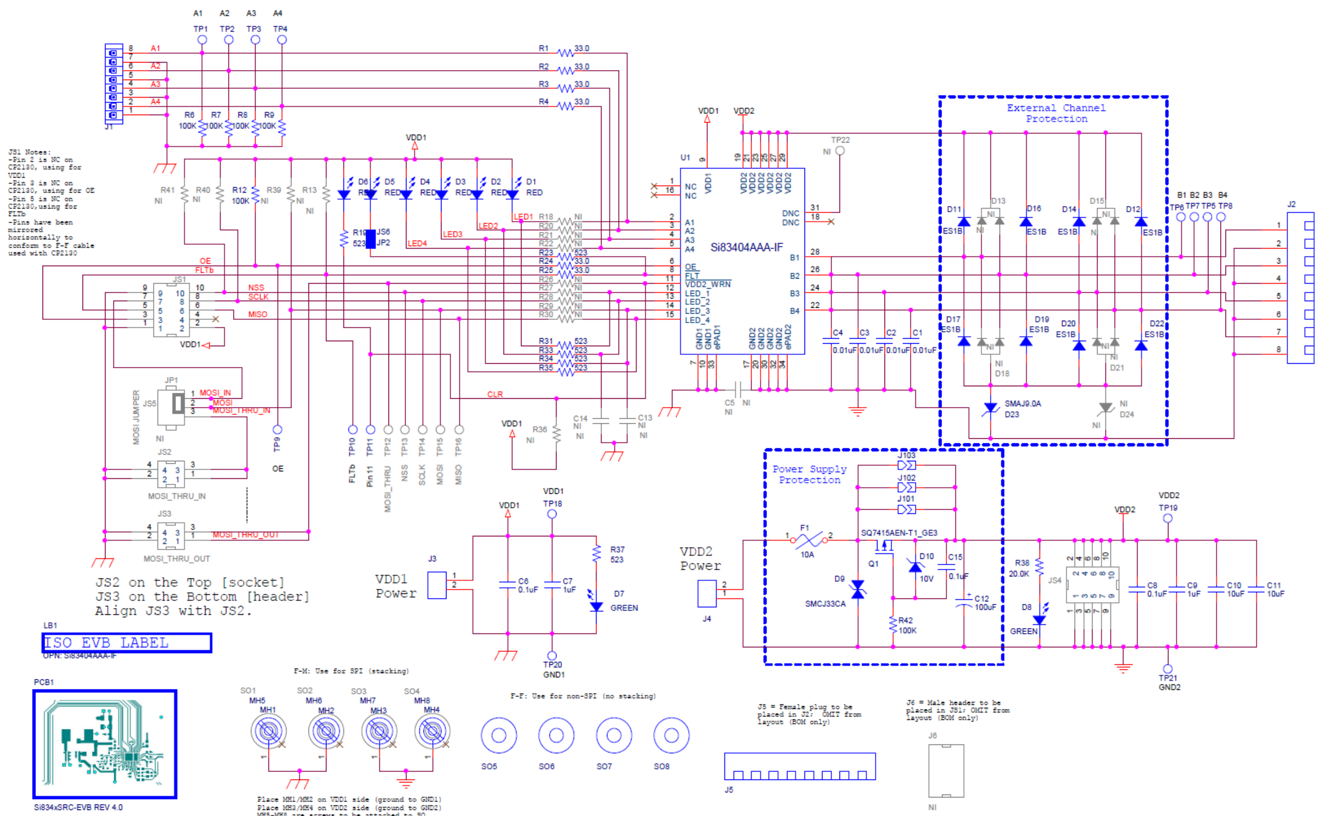


Figure 11. Si834xSRC-EVB Rev 4.0 Schematic

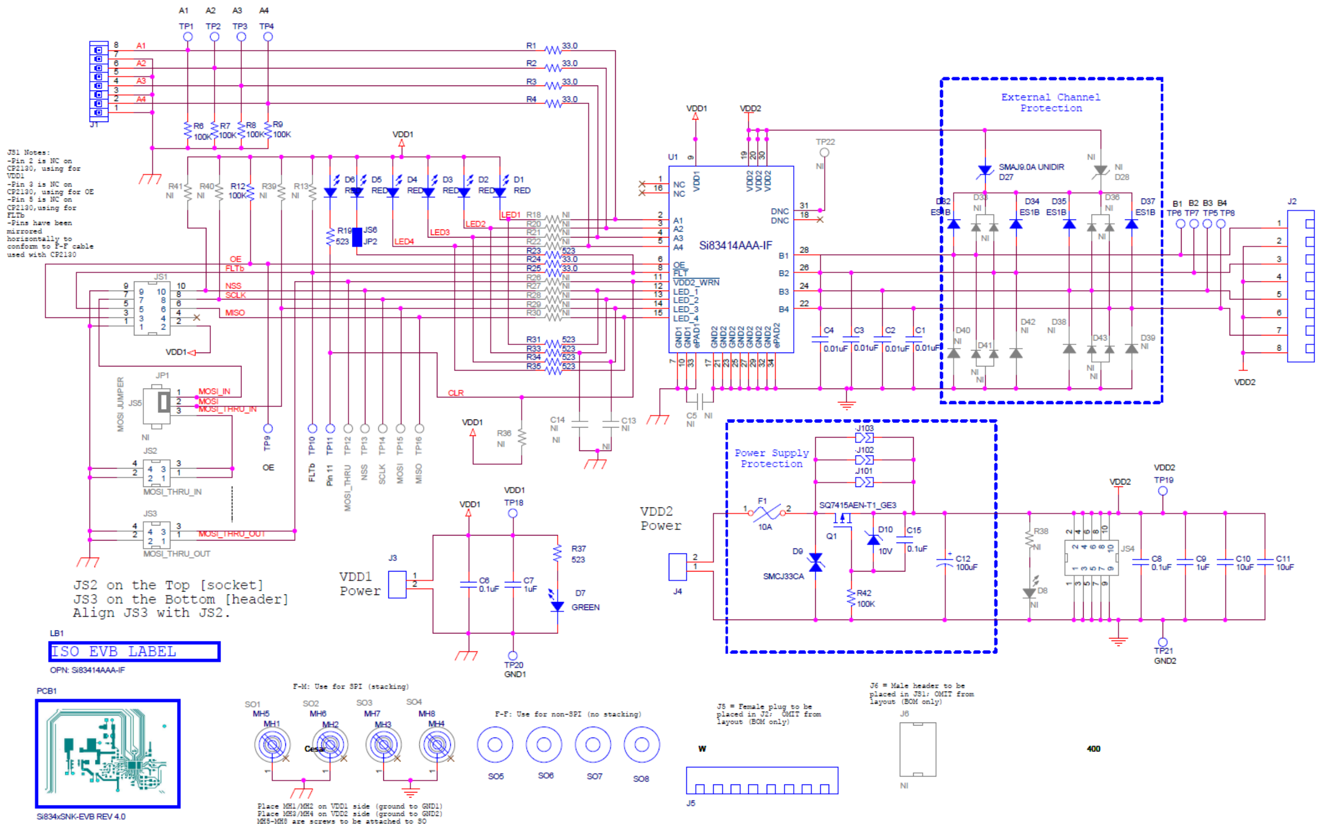


Figure 12. Si834xSNK-EVB Rev 4.0 Schematic

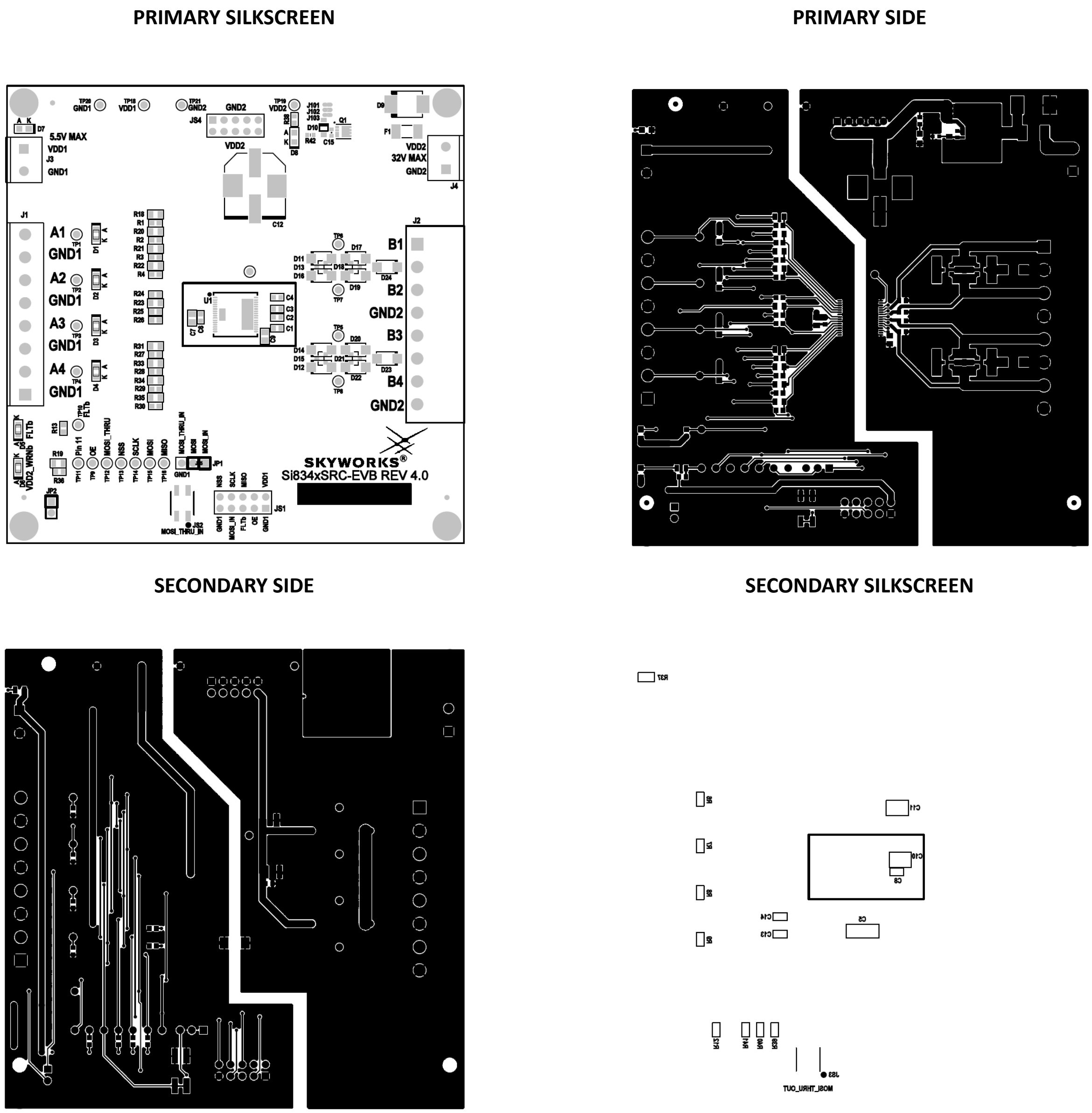
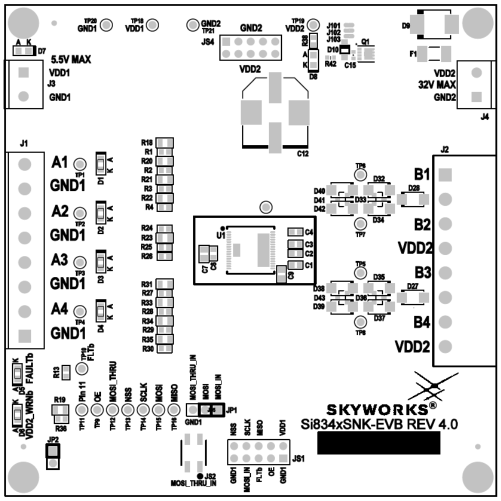
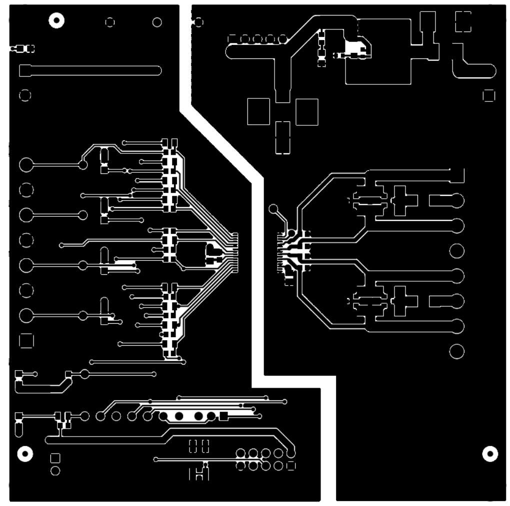


Figure 13. Si834x SRC-EVB Rev 4.0 Layout Files (Primary Silk, Primary, Secondary, Secondary Silk)

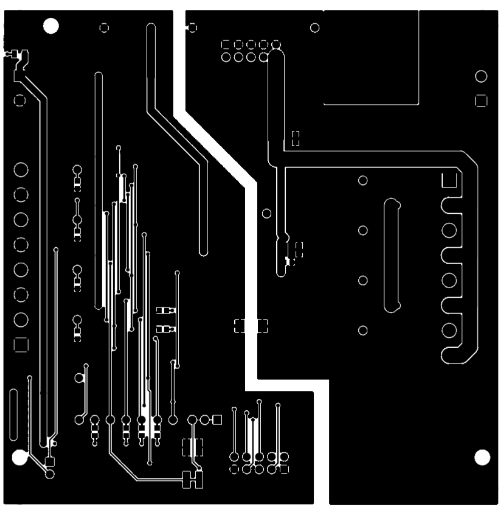
PRIMARY SILKSCREEN



PRIMARY SIDE



SECONDARY SIDE



SECONDARY SILKSCREEN

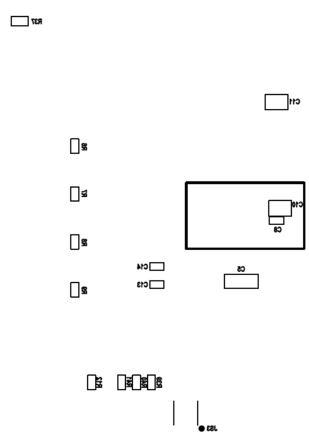


Figure 14. Si834x SNK-EVB Rev 4.0 Layout Files (Primary Silk, Primary, Secondary, Secondary Silk)