DATA SHEET

SKY66194-12: 4400 to 5000 MHz High-gain, Wide Instantaneous Driver Amplifier

Applications

- Massive MIMO
- Driver amplifier for micro and macro base stations
- 4G LTE and 5G NR TDD systems
- Supports 3GPP n79

Features

- High gain: 34.5 dB
- High linearity: < –32 dBc open loop ACLR at +15 dBm (200 MHz LTE, 8.5 dB PAR signal)
- Wide instantaneous signal bandwidth: 200 MHz
- Internally matched input and output return loss to 50 Ω systems
- Integrated active bias, performance compensated over temperature
- Integrated enable ON/OFF function: PAEN = 1.7 to 2.5 V
- Single supply voltage: 5.0 V or 3.3 V
- Pin-to-pin compatible PA family supporting major 3GPP bands
- Compact (16-pin, 5 x 5 x 1.24 mm) package (MSL3, 260 °C per JEDEC J-STD-020)
- For RoHS and other product compliance information, see the Skyworks Certificate of Conformance.

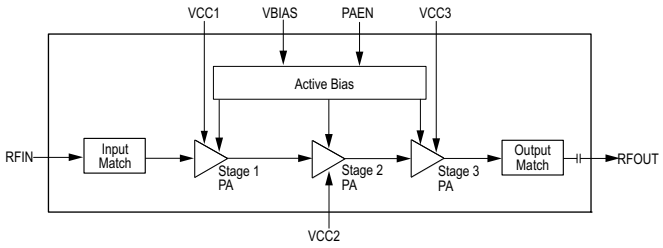


Figure 1. Block Diagram

Description

The SKY66194-12 is a high-gain, linear, wide instantaneous bandwidth, driver amplifier that is fully input/output matched.

The compact 5 x 5 mm driver amplifier is designed for 4G LTE and 5G NR TDD systems operating from 4400 to 5000 MHz. The active biasing circuitry is integrated to compensate performance over temperature, voltage, and process variation.

A block diagram of the SKY66194-12 is shown in Figure 1. The device package and pinout is shown in Figure 2. Signal pin assignments and functional pin descriptions are described in Table 1.

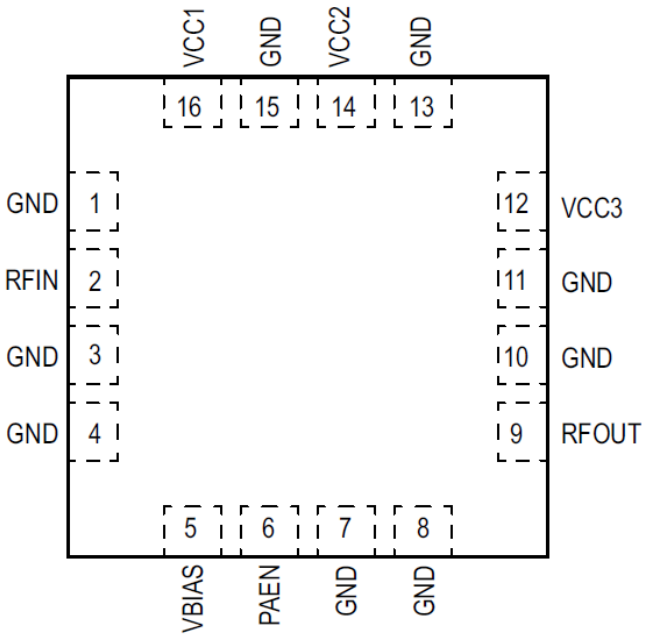


Figure 2. Pinout

Table 1. Signal Descriptions[1]

Pin	Name	Description	Pin	Name	Description
1	GND	Ground	9	RFOUT	RF output port
2	RFIN	RF input port	10	GND	Ground
3	GND	Ground	11	GND	Ground
4	GND	Ground	12	VCC3	Stage 3 collector voltage
5	VBIAS	Bias voltage	13	GND	Ground
6	PAEN	PA enable	14	VCC2	Stage 2 collector voltage
7	GND	Ground	15	GND	Ground
8	GND	Ground	16	VCC1	Stage 1 collector voltage

1. The center ground pad must have a low inductance and low thermal resistance connection to the application's printed circuit board ground plane.

Technical Description

The matching circuits are contained within the device. An on-chip active bias circuit is included within the device for both input and output stages, which provides excellent gain tracking over temperature and voltage variations.

The SKY66194-12 is internally matched for maximum output power and efficiency. The input and output stages are independently supplied using the VCC1, VCC2, and VCC3 supply lines (pins 16, 14, and 12, respectively). The DC control voltage that sets the bias is supplied by the VBIAS signal (pin 5).

Electrical and Mechanical Specifications

The absolute maximum ratings of the SKY66194-12 are shown below. The recommended operating conditions are specified in Table 3, followed by other electrical specifications.

Table 2. Absolute Maximum Ratings[1]

Parameter	Symbol	Minimum	Maximum	Units
RF input power (CW)	P_{IN}		10	dBm
Supply voltage (VCC1, VCC2, VCC3, VBIAS)	V_{CC}		5.5	V
PA enable	VEN		2.8	V
Operating temperature	T_C	–40	+110	°C
Storage temperature	T_{ST}	–55	+125	°C
Junction temperature	T_J		+150	°C

1. Exposure to maximum rating conditions for extended periods may reduce device reliability. There is no damage to device with only one parameter set at the limit and all other parameters set at or below their nominal value. Exceeding any of the limits listed here may result in permanent damage to the device.

ESD Handling: Industry-standard ESD handling precautions must be adhered to at all times to avoid damage to this device.

Table 3. Recommended Operating Conditions

Parameter	Symbol	Min	Typ	Max	Units
Supply voltage (VCC1, VCC2, VCC3, VBIAS)	V_{CC1}, V_{CC2}, V_{CC3}, V_{BIAS}	3.3	5	5.25	V
PA enable: ON OFF	PAEN	1.7	 2.0 0	 2.5 0.5	 V V
PA enable current	I_{ENABLE}		1	12	µA
Operating frequency	f	4400		5000	MHz
Operating temperature	T_C	–40	+25	+110	°C

Table 4. Electrical Specifications[1]

(VCC1 = VCC2 = VCC3 = VBIAS = 5 V, PAEN = 2.0 V, f = 4900 MHz, TC = +25 °C, Input/Output Load = 50 Ω, Unless Otherwise Noted)

Parameter	Symbol	Test Condition	Min	Typ	Max	Units
Frequency	f		4400		5000	MHz
Small signal gain	|S21|	PIN = –30 dBm	33	34.5		dB
Gain @ +15 dBm	|S21|@+15 dBm	POUT = +15 dBm	33	35		dB
Input return loss	|S11|	PIN = –30 dBm	10	15		dB
Output return loss	|S22|	PIN = –30 dBm	10	15		dB
Reverse isolation[2]	|S12|	PIN = –30 dBm	38	45		dB
ACLR @ raw dBm[2]	ACLR	POUT = +15 dBm (200 MHz LTE, 8.5 dB PAR signal)		–32		dBc
Output power at 1dB gain compression[2]	P1dB	CW, reference to small signal gain (PIN = –30 dBm)	+28	+30		dBm
Output power at 3 dB gain compression[2]	P3dB	CW, reference to small signal gain (PIN = –30 dBm)		+34		dBm
2nd harmonic[2]	2fO	CW, POUT = +15 dBm		–40	–34	dBc
3rd harmonic[2]	3fO	CW, POUT = +15 dBm		–50	–45	dBc
Quiescent current	Iccq	No RF signal		110	135	mA
Power dissipation[2]	PD	Tcase = +110 °C, Pout = +15 dBm		1.2		W
Device thermal resistance[2]	ΘJC	Tcase = +110 °C, Pout = +15 dBm		16.3		°C/W
RF turn-on/turn-off time[3]				0.8	1	µs

1. Performance is guaranteed only under the conditions listed in this table.
2. Not tested in production. Verified by design.
3. RF turn-on time is measured from the time the PA enable reaches 50% of PA enable "on" level to the time at which the RF output power achieves 90% of the average steady-state "on" level.
   RF turn-off time is measured from the time the PA enable reaches 50% of PA enable "on" level to the time at which the RF output power decreases to 10% of the average steady-state "on" level.

Evaluation Board Description

An Evaluation Board is used to test the performance of the SKY66194-12. An application schematic is provided in Figure 3. Table 6 provides the Bill of Materials (BOM) list for Evaluation Board components.

An assembly drawing for the Evaluation Board is shown in Figure 4. Board layer details are shown in Figure 5. Layer detail physical characteristics are noted in Figure 6.

Circuit Design Considerations

The following design considerations are general in nature and must be followed regardless of final use or configuration:

- Paths to ground should be made as short as possible.
- The ground pad of the SKY66194-12 has special electrical and thermal grounding requirements. This pad is the main thermal conduit for heat dissipation.

Because the circuit board acts as the heat sink, it must shunt as much heat as possible from the

device. Therefore, design the connection to the ground pad to dissipate the maximum wattage produced by the circuit board. Multiple vias to the grounding layer are required.

NOTE: A poor connection between the ground pad and ground increases junction temperature (TJ), which reduces the life of the device.

Evaluation Board Test Procedure

Turn-On Sequence

1. Connect 50 Ω test equipment or load to the input and output RF ports of the Evaluation Board.
2. Connect the DC ground.
3. Connect all VCCs and VBIAS lines to a +5 V supply. Connect PAEN to a 2.0 V supply.
4. Without applying RF, turn on the 5 V supply, then turn on the 2 V PAEN.
5. Apply RF signal data at –30 dBm and observe that the gain of the device is approximately 35 dB. Begin measurements.

Turn-Off Sequence

1. Turn off the RF input to the device.
2. Turn off PAEN (set to 0 V).
3. Turn off all VCCs and VBIAS.

NOTE: It is important to adjust the VCC voltage sources so that +5 V is measured at the board. High collector currents drop the collector voltage significantly if long leads are used. Adjust the bias voltage to compensate.

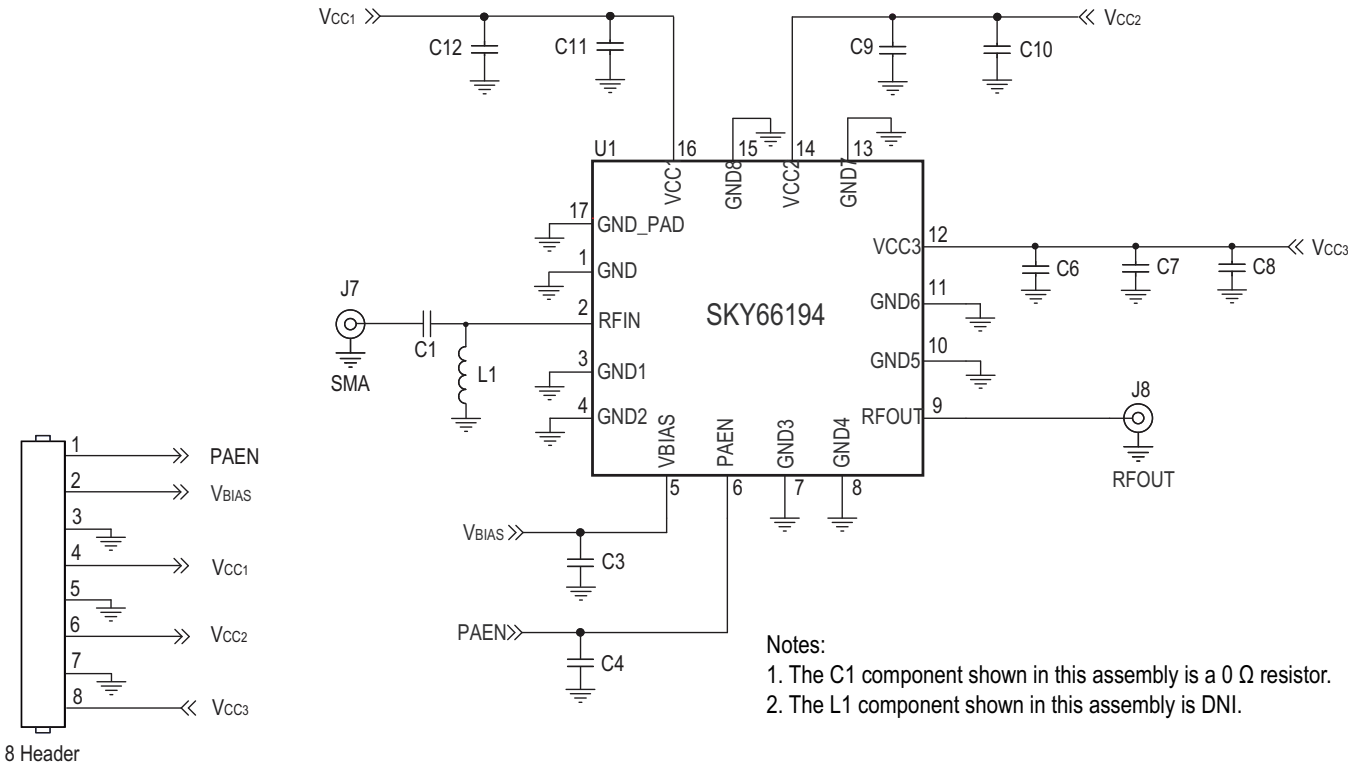
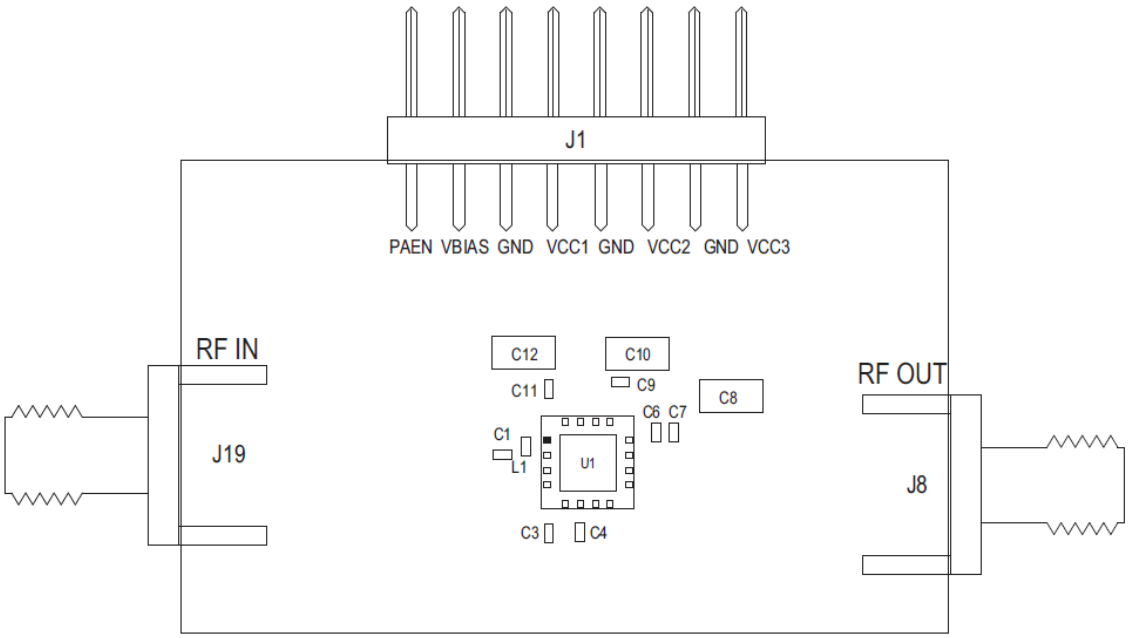


Figure 3. Application Schematic

Table 5. Evaluation Board Bill of Materials (BOM)

Component	Description	Size
C1	Resistor, 0 Ω, 0.063 W	0402
C3	Ceramic capacitor, 1 µF, ±10%, 16 V	0402
C4, C7	Ceramic capacitor, 3300 pF, X7R, ±10%, 50 V	0402
C6, C9, C11	Ceramic capacitor, 0.47 µF	0402
C8, C10, C12	Ceramic capacitor, 10 µF, X7R, ±10%, 16 V	1206
L1	DNI	
TW21-D690-XXXX	Evaluation board	



Notes

1. Evaluation Board Gerber files are available on request.
2. The C1 component shown in this assembly is a 0 Ω resistor.
3. The L1 component shown in this assembly is DNI.

Figure 4. Evaluation Board Assembly Drawing

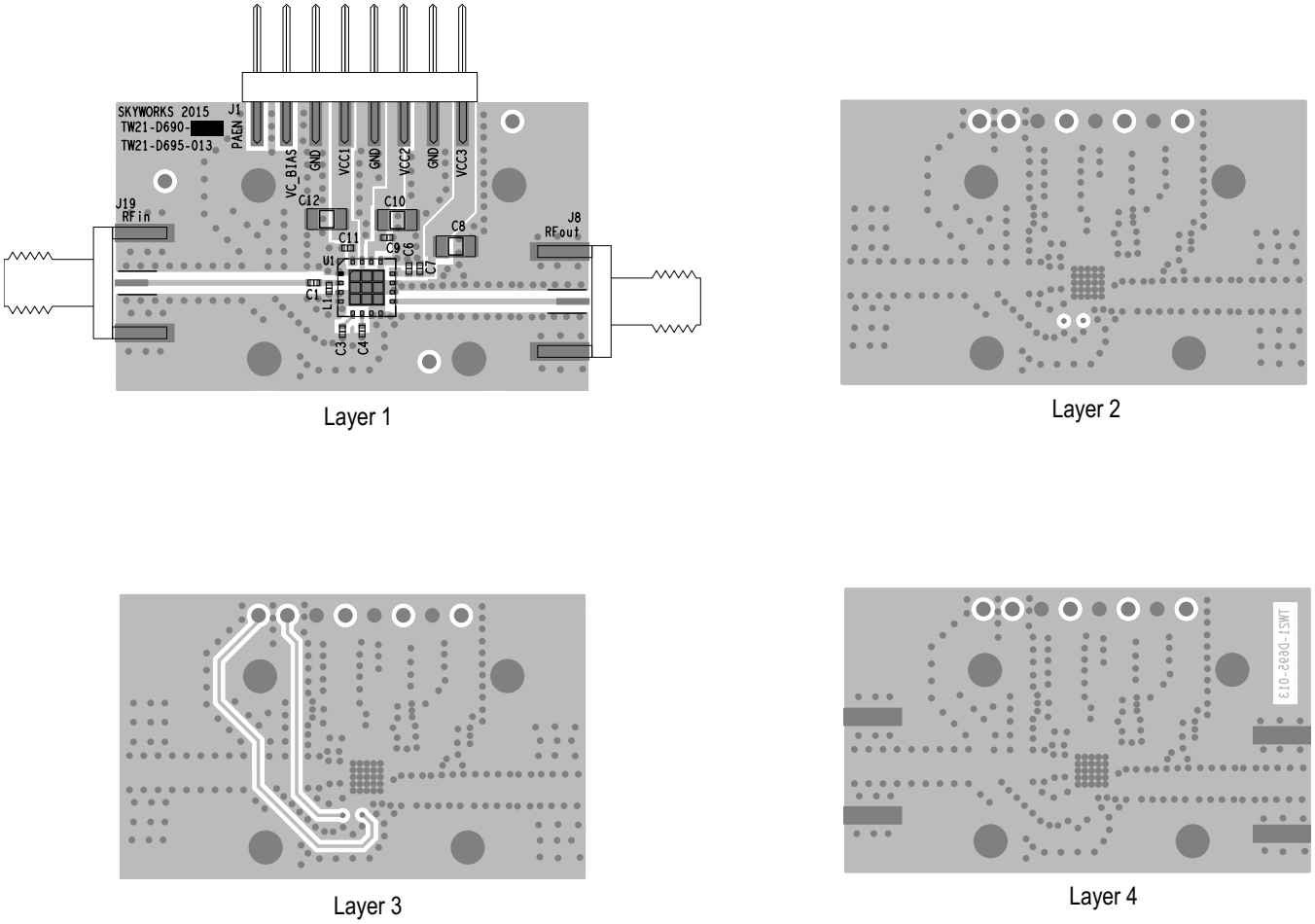


Figure 5. Board Layer Detail

50 Ohm	Cross Section	Name	Thickness (mm)	Materials
W = 0.500 mm		TMask	0.010	Solder Resist
		L1	0.035	Cu, 1 oz.
		Dielectric	0.250	R04350
		L2	0.035	Cu, 1 oz.
		Dielectric	0.350	FR4
		L3	0.035	Cu, 1 oz.
		Dielectric	0.250	FR4
		L4	0.035	Cu, 1 oz.
		BMask	0.010	Solder Resist

Figure 6. Layer Detail Physical Characteristics

Application Circuit Notes

Center Ground. It is extremely important to sufficiently ground the bottom ground pad of the device for both thermal and stability reasons. Multiple small vias are acceptable and work well under the device if solder migration is an issue.

GND (pins 1, 3, 4, 7, 8, 10, 11, 13, and 15). Attach all ground pins to the RF ground plane with the largest diameter and lowest inductance via that the layout allows. Multiple small vias are acceptable and will work well under the device if solder migration is an issue.

VBIAS (pin 5). The bias supply voltage for each stage, nominally set to +5 V.

RFOUT (pin 9). Amplifier RF output pin (Z_0 = 50 Ω). The module includes an internal DC blocking capacitor. All impedance matching is provided internal to the module.

VCC1, VCC2, and VCC3 (pin 16, 14, and 12, respectively). Supply voltage for each stage collector bias is nominally set to 5 V. The evaluation board has inductors L1 and L2. These are place holders and should be populated with 0 Ω resistors. Bypass and decoupling capacitors C6 through C12 should be placed in the approximate location shown on the evaluation board assembly drawing, although exact placement is not critical.

RFIN (pin 2). Amplifier RF input pin (Z_0 = 50 Ω). All impedance matching is provided internally to the module.

Package and Handling Information

Since the device package is sensitive to moisture absorption, it is baked and vacuum packed before shipping. Instructions on the shipping container label regarding exposure to moisture after the container seal is broken must be followed. Otherwise, problems related to moisture absorption may occur when the part is subjected to high temperature during solder assembly.

The SKY66194-12 is rated to Moisture Sensitivity Level 3 (MSL3) at 260 °C. It can be used for lead or lead-free soldering. For additional information, refer to the Skyworks Application Note, Solder Reflow Information, document number 200164.

Care must be taken when attaching this product, whether it is done manually or in a production solder reflow environment. Production quantities of this product are shipped in a standard tape and reel format.

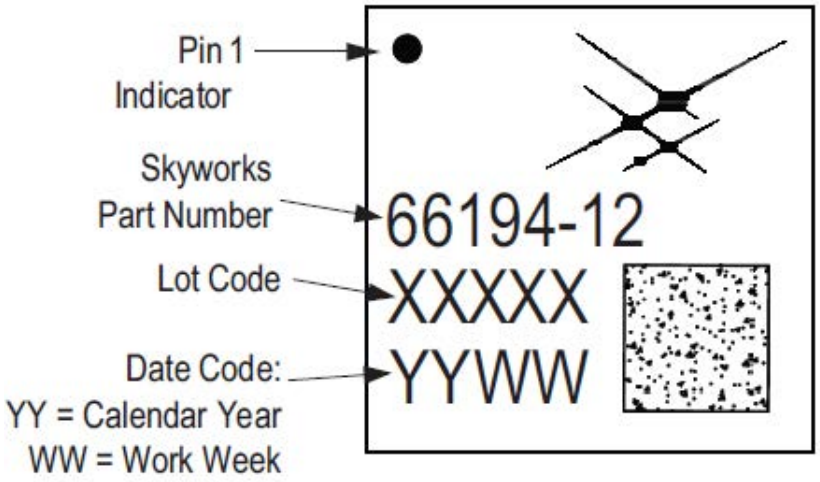
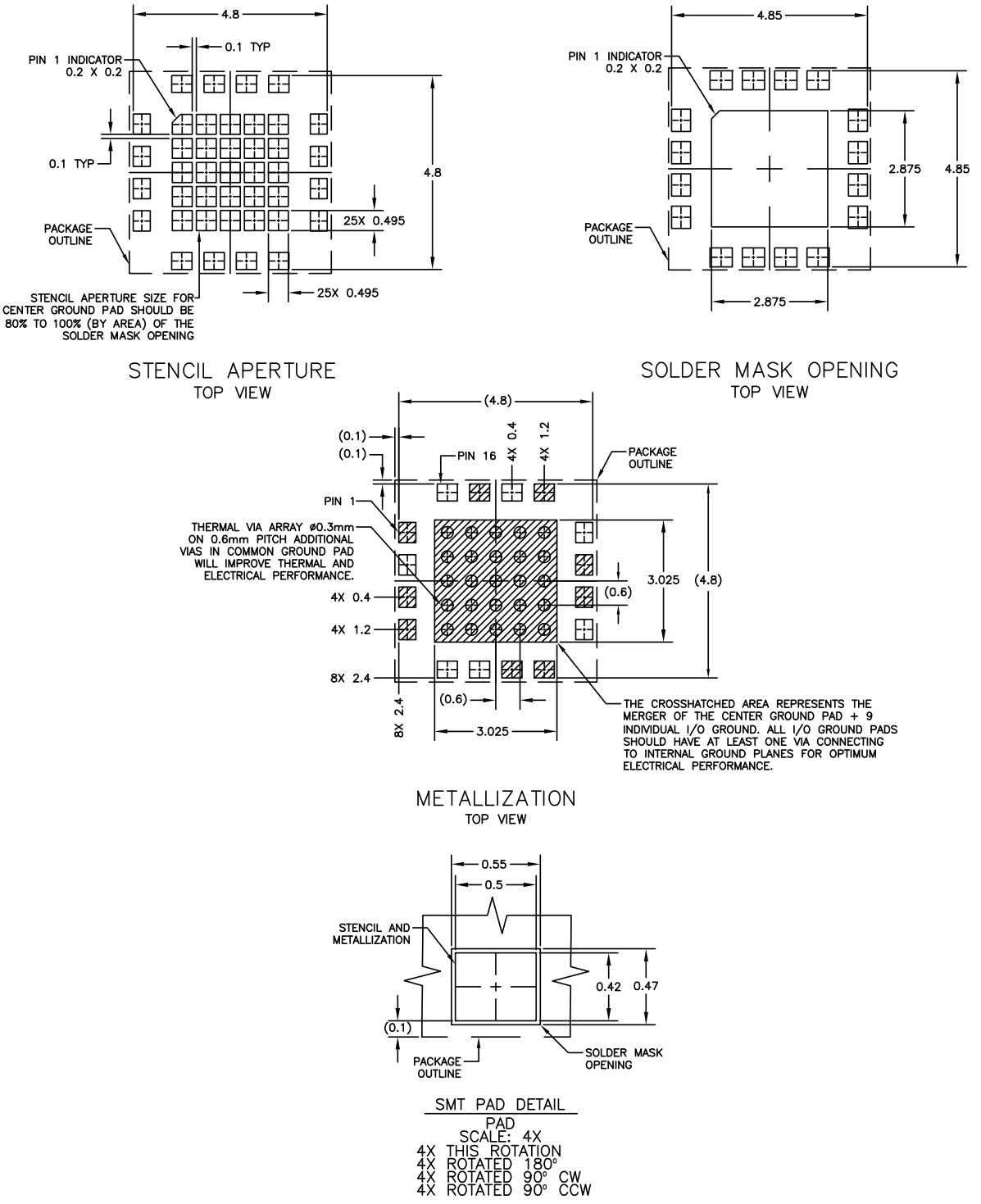


Figure 7. Typical Part Marking



NOTES:
1. DIMENSIONS ARE IN MILLIMETERS, UNLESS OTHERWISE SPECIFIED.
2. THERMAL VIAS SHOULD BE RESIN FILLED AND CAPPED IN ACCORDANCE WITH IPC–4761 TYPE VII VIAS. 30–35UM Cu THICKNESS IS RECOMMENDED.

Figure 8. PCB Layout Footprint

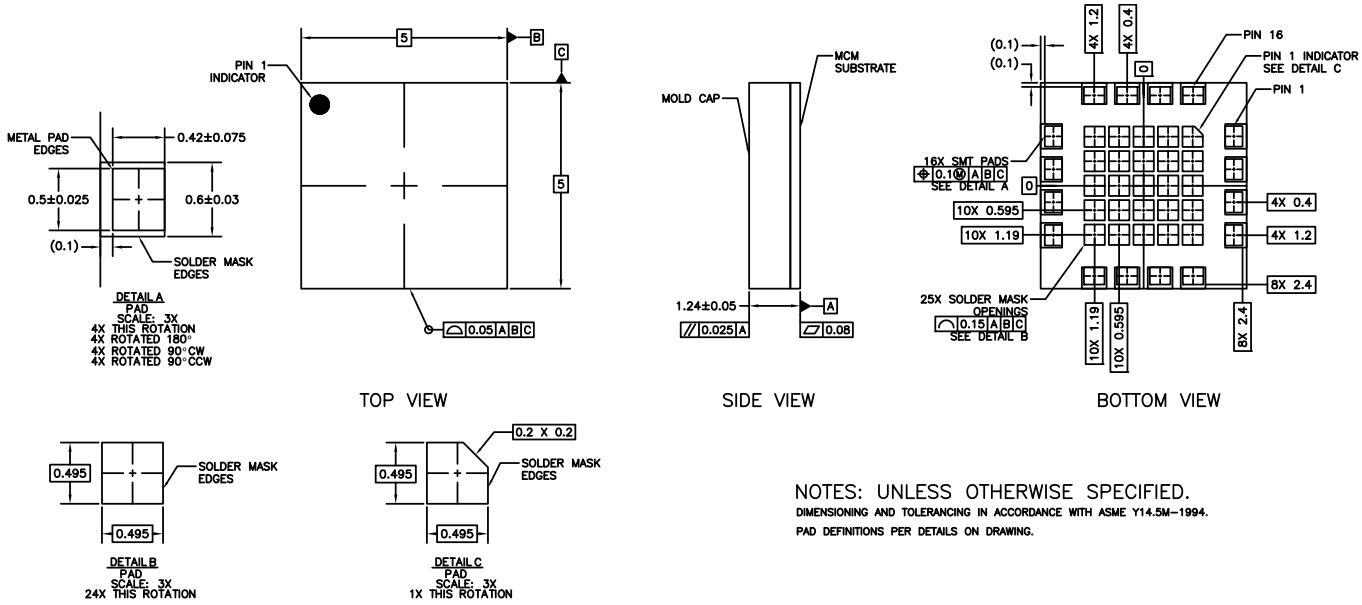


Figure 9. Package Dimensions

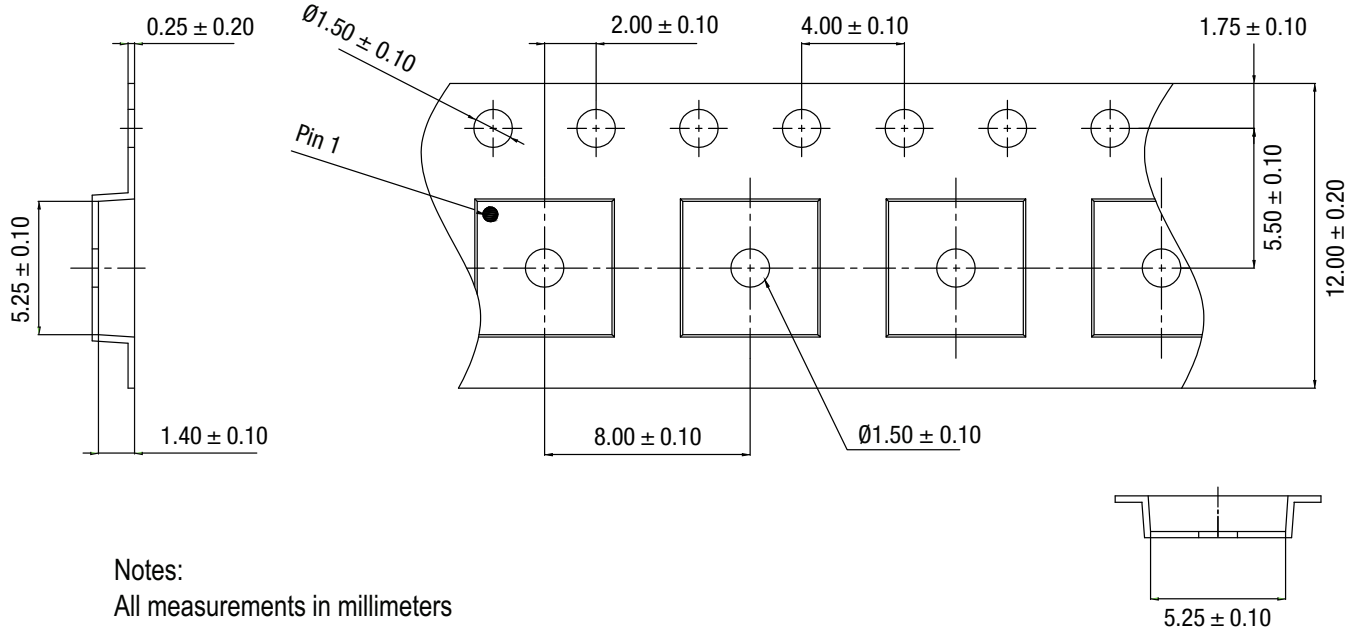


Figure 10. Tape and Reel Dimensions

Ordering Information

Part Number	Part Description	Evaluation Board Part Number
SKY66194-12	4400 to 5000 MHz High-Gain, Wide Instantaneous Driver Amplifier	SKY66194-12EK1