DATA SHEET

SKY13638-700LF: 0.4 to 3.8 GHz SP10T LTE Transmit/Receive Switch with Mobile Industry Processor Interface (MIPI®)

Applications

- 3G/4G multimode cellular tablets and handsets (LTE, UMTS, CDMA2000)
- Embedded data cards

Features

- Broadband frequency range: 0.4 to 3.8 GHz
- Low insertion loss, 0.75 dB typical @ 2.7 GHz
- High isolation and linearity
- Multi-closed function for CA applications
- Integrated, programmable MIPI® version 2.0
- Default USID = 1010
- Ten linear TRX ports with isolation greater than 26 dB@ 2.7 GHz
- Small 20-pin, 2.4 x 2.4 x 0.50 mm Quad Flat No-Lead (QFN) package, MSL1, 260 °C per JEDEC-J-STD-020
- For RoHS and other product compliance information, see the Skyworks Certificate of Conformance.

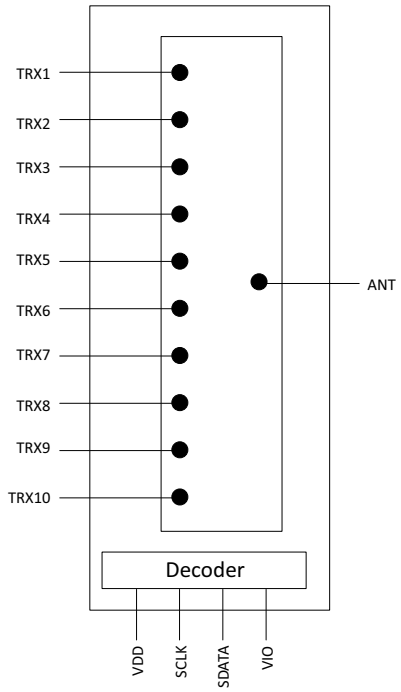


Figure 1. Functional Block Diagram

Description

The SKY13638-700LF is a single-pole, ten-throw (SP10T) antenna switch with MIPI, Version 2.0.

Using advanced switching technologies, the switch maintains low insertion loss and high isolation for the transmit and receive switching paths.

The high-linearity performance and low insertion loss makes the SKY13638-700LF an ideal choice for UMTS, CDMA2000, and LTE applications.

The switch also exhibits an excellent triple beat ratio and second- and third-order intermodulation distortion (IMD) performance.

Switching is controlled by an integrated MIPI interface. Depending on the logic applied to the decoder, the antenna pin is connected to one of 10 switched RF ports using a low insertion loss path, while the paths between the antenna pin and the other RF pins are in a high isolation state.

No external dc blocking capacitors are required on the RF paths.

Any two arms can be switched on at the same time with multi-closed function for CA applications.

A functional block diagram is shown in Figure 1. The pin configuration and package are shown in Figure 2. Signal pin assignments and descriptions are provided in Table 1.

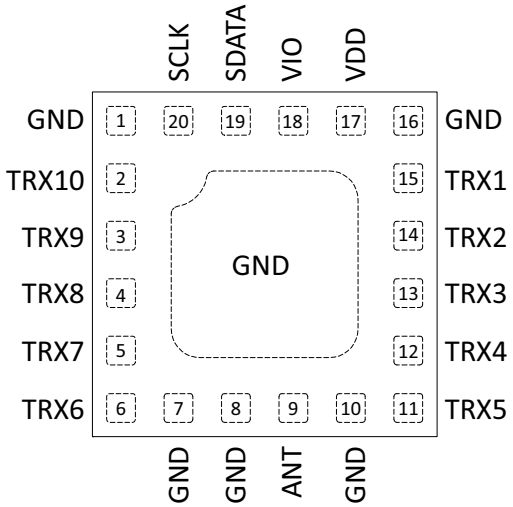


Figure 2. Pinout (Top View)

Table 1. Pin Descriptions

Pin	Name	Description	Pin	Name	Description
1	GND	Ground	11	TRX5	RF input/output path 5
2	TRX10	RF input/output path 10	12	TRX4	RF input/output path 4
3	TRX9	RF input/output path 9	13	TRX3	RF input/output path 3
4	TRX8	RF input/output path 8	14	TRX2	RF input/output path 2
5	TRX7	RF input/output path 7	15	TRX1	RF input/output path 1
6	TRX6	RF input/output path 6	16	GND	Ground
7	GND	Ground	17	VDD	DC power supply
8	GND	Ground	18	VIO	MIPI decoder interface/reference voltage
9	ANT	Antenna input/output	19	SDATA	Data input/output
10	GND	Ground	20	SCLK	Clock signal

Electrical and Mechanical Specifications

Figure 3 illustrates the test setup used to measure intermodulation products. This industry standardized test is used to simulate the WCDMA Band 1 linearity of the antenna switch. A +20 dBm CW signal, f_{FUND}, is sequentially applied to the TRX1 through TRX10 ports, while a –15 dBm CW blocker signal, f_{BLK}, is applied to the ANT port.

The resulting third-order intermodulation distortion (IMD3), f_{RX}, is measured over all phases of f_{FUND}. The SKY13638-700LF exhibits exceptional performance for all TX/RX ports.

IMD2 and IMD3 test conditions for various frequencies are listed in Tables 2 and 3.

Table 8 describes the register content and programming read/write sequences. Refer to the MIPI Alliance Specification for RF Front-End Control Interface (RFFE), version 2.0 for additional information on MIPI programming sequences and MIPI bus specifications.

Figures 5 and 6 provide the timing diagrams for register write commands and read commands. Table 9 provides the Register_0 logic. Table 10 describes the register parameters and bit values.

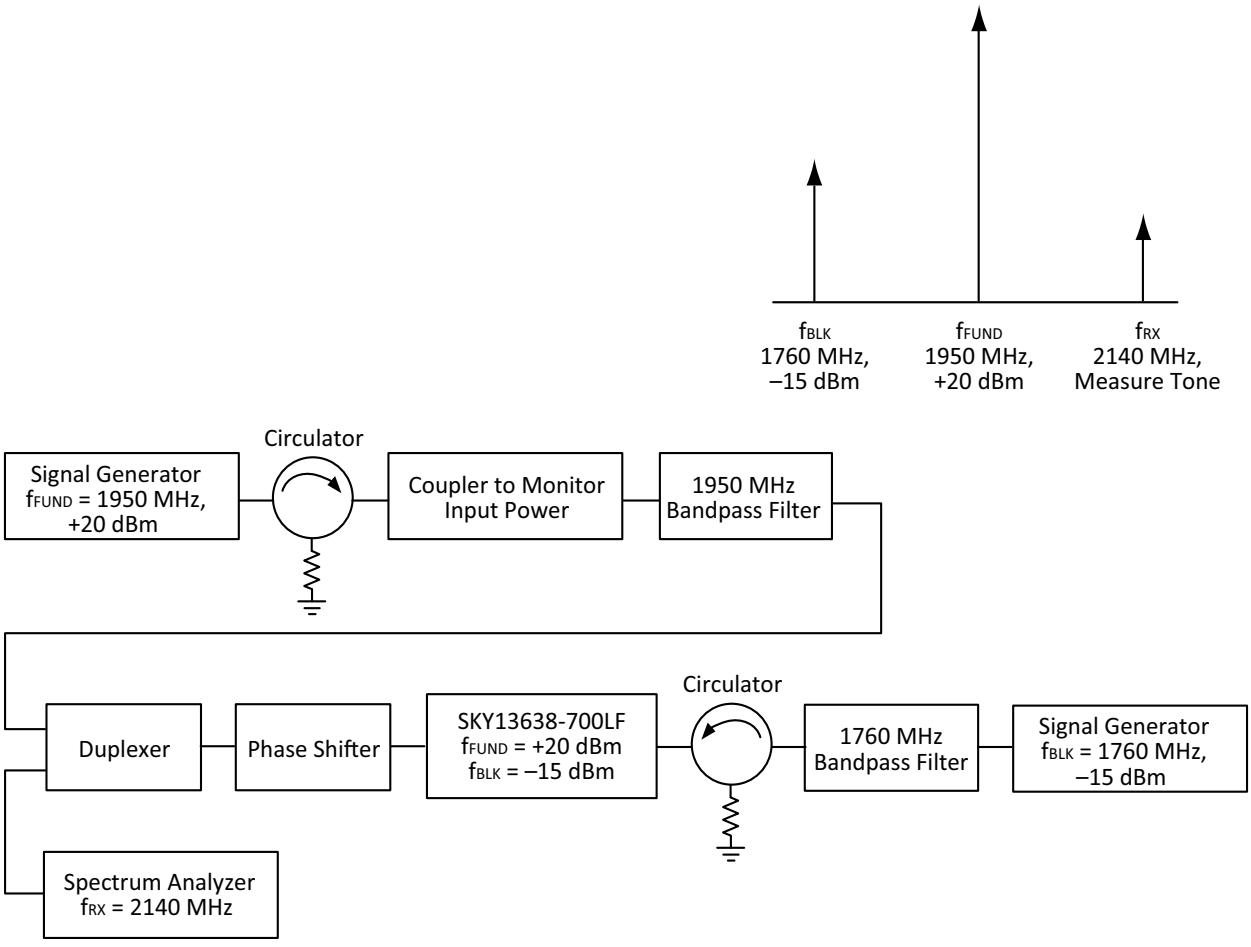


Figure 3. Third-Order Intermodulation Test Setup

Table 2. IMD2 Test Conditions

Band	Transmit Frequency (MHz)	Transmit Power (dBm)	Frequency Blocker, Low (MHz)	Frequency Blocker, High (MHz)	Power Blocker (dBm)	Receive Frequency (MHz)
1	1950.0	+20	190	4090	-15	2140.0
2	1880.0		80	3840		1960.0
4	1732.0		400	3864		2132.0
5	836.5		45	1718		881.5
7	2535.0		120	5187		2655.0
8	897.0		45	1839		942.0

Table 3. IMD3 Test Conditions

Band	Transmit Frequency (MHz)	Transmit Power (dBm)	Frequency Blocker (MHz)	Power Blocker (dBm)	Receive Frequency (MHz)
1	1950.0	+20	1760.0	–15	2140.0
2	1880.0		1800.0		1960.0
4	1732.0		1332.0		2132.0
5	836.5		791.5		881.5
7	2535.0		2415.0		2655.0
8	897.0		852.0		942.0
11/21	1452		1404		1500

Table 4. Absolute Maximum Ratings[1]

Parameter	Symbol	Min	Max	Units
Power supply	V_{DD}	–0.5	6.0	V
Digital control signal	V_{IO}	–0.5	2.8	V
RF input power	P_{IN}		+35	dBm
Storage temperature	T_{STG}	–55	+150	°C
Operating temperature	T_{OP}	–40	+90	°C
Electrostatic discharge Human Body Model (HBM), Class 1C	ESD		1500	V
Charged Device Model (CDM), Class C3			1000	

1. Exposure to maximum rating conditions for extended periods may reduce device reliability. There is no damage to device with only one parameter set at the limit and all other parameters set at or below their nominal value. Exceeding any of the limits listed here may result in permanent damage to the device.

ESD Handling: *Industry-standard ESD handling precautions must be adhered to at all times to avoid damage to this device.*

Table 5. General Electrical Specifications[1]

(V_{DD} = 2.85 V, V_{IO} = 1.8 V, T_{OP} = +25 °C, Characteristic Impedance [Z_O] = 50 Ω, Unless Otherwise Noted)

Parameter	Symbol	Test Condition	Min	Typ	Max	Units
Supply voltage	V_{DD}		2.4	2.85	5.8	V
Supply current, active mode	I_{DD}			50	100	µA
Supply current, low power mode	I_{DDL}			12	30	µA
Interface supply	V_{IO}		1.65	1.80	1.95	V
Interface signal: high			0.8 x V_{IO}			V
Interface signal: low					0.2 x V_{IO}	
Control current: high	I_{CTL}	V_{IO} = 1.8 V		6	20	µA
Control current: low		V_{IO} = 0 V		3	5	
Turn-on time[2]	t_{ON}	Measured from 50% of final VDD supply voltage to 90% of RF power		5	20	µs
Switching time[2]	t_{SW}	Measured from the rising edge of last clock signal to 90% RF power		2	5	µs

1. Performance is assured only under the conditions listed in this table.
2. P_{IN} = +27 dBm, T_A = –40 to +90 °C. See Figure 4.

Table 6. Small Signal Specifications[1]

Parameter	Symbol	Test Condition	Min	Typ	Max	Units
Insertion loss ANT to TRX1-TRX10	IL	400 to 960 MHz		0.3	0.5	dB
		1420 to 2170 MHz		0.55	0.75	
		2170 to 2690 MHz		0.75	0.95	
		3400 to 3800 MHz		0.9	1.25	
Isolation ANT to TRX1-TRX10, non-adjacent	ISO	400 to 960 MHz	37	40		dB
		1420 to 2170 MHz	29	32		
		2170 to 2690 MHz	27	30		
		3400 to 3800 MHz	23	26		
Isolation ANT to TRX1-TRX10, adjacent	ISO	400 to 960 MHz	34	37		dB
		1420 to 2170 MHz	28	31		
		2170 to 2690 MHz	26	29		
		3400 to 3800 MHz	21	24		
Return loss ANT to TRX1-TRX10	RL	400 to 2690 MHz	9	11		dB
		3400 to 3800 MHz	8	11		

1. Performance is assured only under the conditions listed in this table.

Table 7. Large Signal Specifications[1]

Parameter	Symbol	Test Condition	Min	Typ	Max	Units
P0.2dB	P0.2dB	Up to 3800 MHz	+35	+38		dBm
LTE/WCDMA harmonic, TRX1-TRX10 to ANT, low-band	2fo	fo = 400 to 960 MHz, P_{IN} = +26 dBm, VSWR = 1:1		–80	–67	dBm
	3fo			–81	–75	
	2fo	fo = 400 to 960 MHz, P_{IN} = +26 dBm, VSWR = 6:1		–71	–59	
	3fo			–69	–64	
LTE/WCDMA harmonic, TRX1-TRX10 to ANT, mid-band	2fo	fo = 1427 MHz to 1910 MHz, P_{IN} = +26 dBm, VSWR = 1:1		–77	–61	dBm
	3fo			–76	–71	
	2fo	fo = 1427 MHz to 1910 MHz, P_{IN} = +26 dBm, VSWR = 6:1		–71	–60	
	3fo			–63	–58	
LTE/WCDMA harmonic, TRX1-TRX10 to ANT, high-band	2fo	fo = 1910 to 2690 MHz, P_{IN} = +26 dBm, VSWR = 1:1		–73	–61	dBm
	3fo			–71	–66	
	2fo	fo = 1910 to 2690 MHz, P_{IN} = +26 dBm, VSWR = 6:1		–70	–60	
	3fo			–59	–54	
LTE harmonic, ultra-high-band ANT to TRX1-TRX10	2fo	fo = 3400 to 3800 MHz, P_{IN} = +26 dBm, VSWR = 1:1		–72	–56	dBm
	3fo			–72	–67	
	2fo	fo = 3400 to 3800 MHz, P_{IN} = +26 dBm, VSWR = 5:1		–67	–54	
	3fo			–63	–58	
Harmonics band 17, TRX1-TRX10 to ANT	B17 3fo	fo = 710 MHz, P_{IN} = +25 dBm, VSWR = 1:1		–85	–81	dBm
	B17 3fo	fo = 710 MHz, P_{IN} = +25 dBm, VSWR = 5:1		–76	–71	
Harmonics band 13, TRX1-TRX10 to ANT	B13 2fo	fo = 787 MHz, P_{IN} = +25 dBm, VSWR = 1:1		–86	–78	dBm
	B13 2fo	fo = 787 MHz, P_{IN} = +25 dBm, VSWR = 5:1		–76	–60	
Second-order intermodulation distortion	IMD2	TRX1 to TRX10, see test conditions in Table 4		–115	–105	dBm
Third-order intermodulation distortion	IMD3	TRX1 to TRX10, see test conditions in Table 5		–113.5	–105	dBm

1. Performance is assured only under the conditions listed in this table.

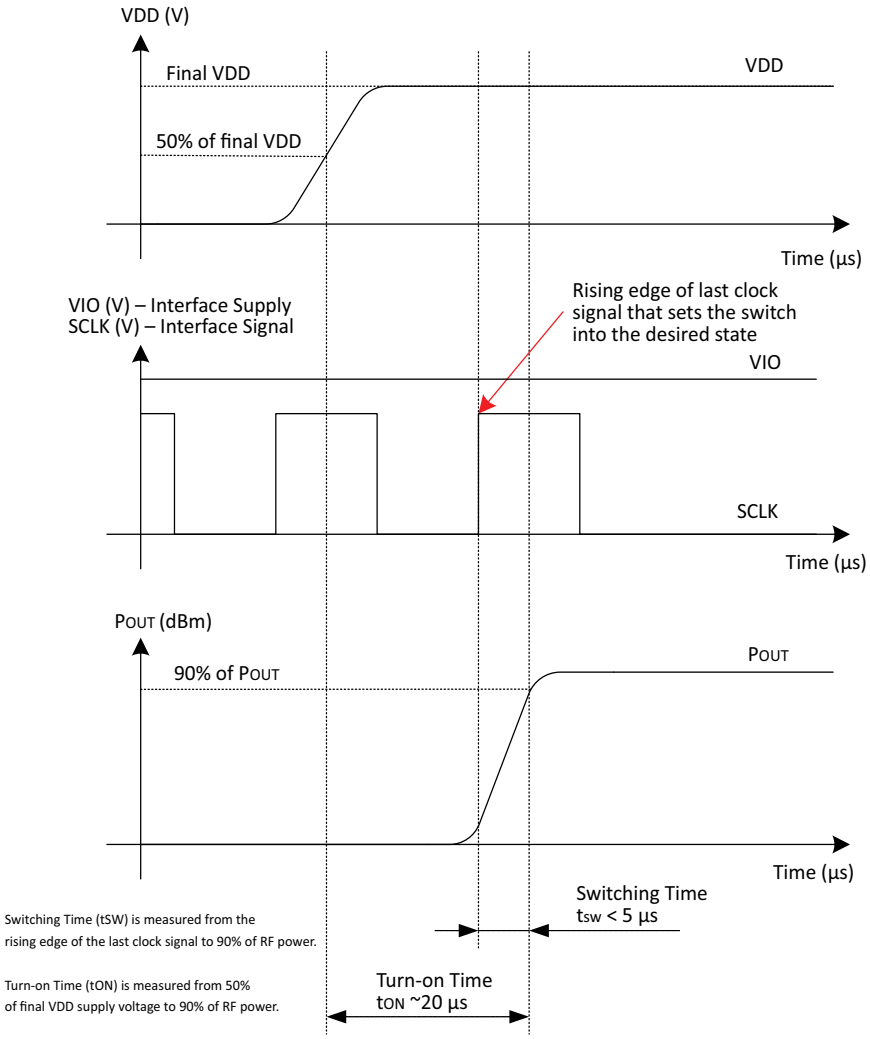


Figure 4. Timing Diagram

Table 8. Command Sequence Bit Definitions[1]

Type	SSC	C11-C8	C7	C6-C5	C4	C3-C0	Parity Bits	BPC	Extended Operation					
									DA7(1)-DA0(1)	Parity Bits	BPC	DA7(n)-DA0(n)	Parity Bits	BPC
Reg0 Write	Y	SA[3:0]	1	Data[6:5]	Data[4]	Data{3:0]	Y	Y	-	-	-	-	-	-
Reg Write	Y	SA[3:0]	0	10	Addr[4]	Addr[3:0]	Y	-	Data[7:0]	-	-	-	Y	Y
Reg Read	Y	SA[3:0]	0	11	Addr[4]	Addr[3:0]	Y	Y	Data[7:0]	-	-	-	Y	Y

1. SSC = sequence start command, DA = data/address frame bits, BC = byte count (# of consecutive addresses), C = command frame bits, BPC = bus park cycle

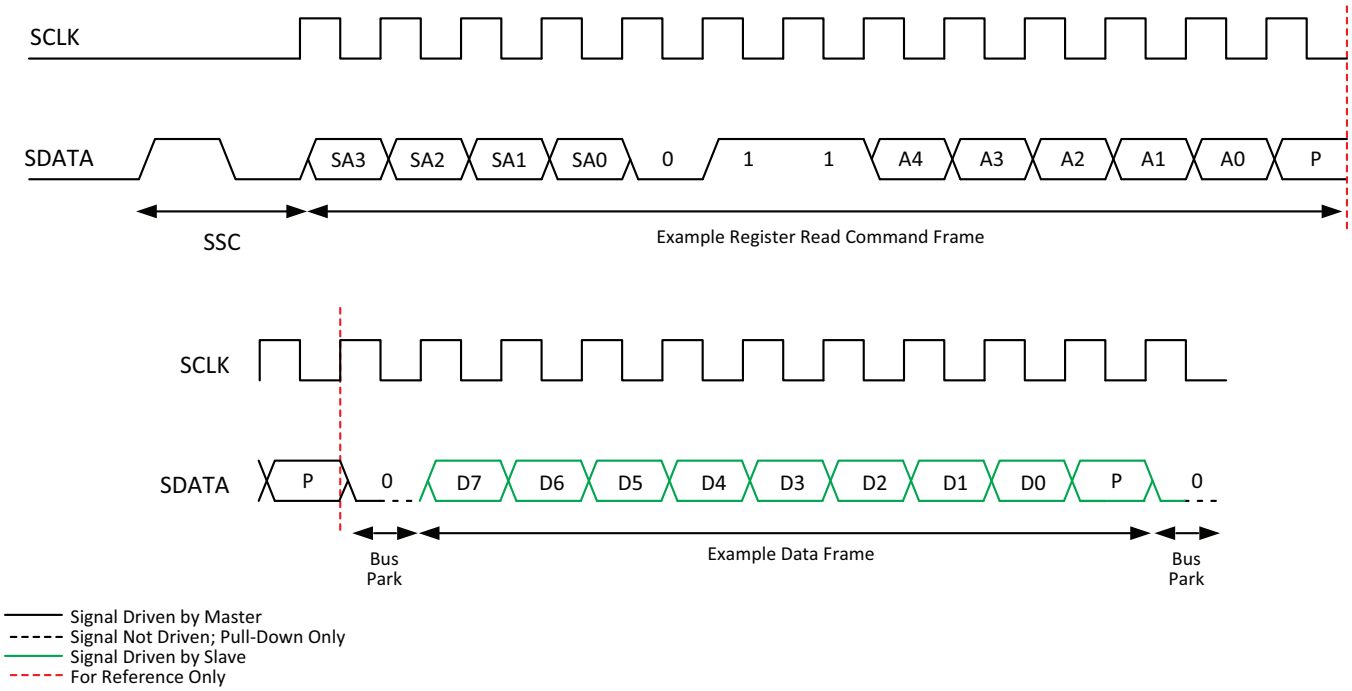


Figure 5. Register Write Command Timing Diagram

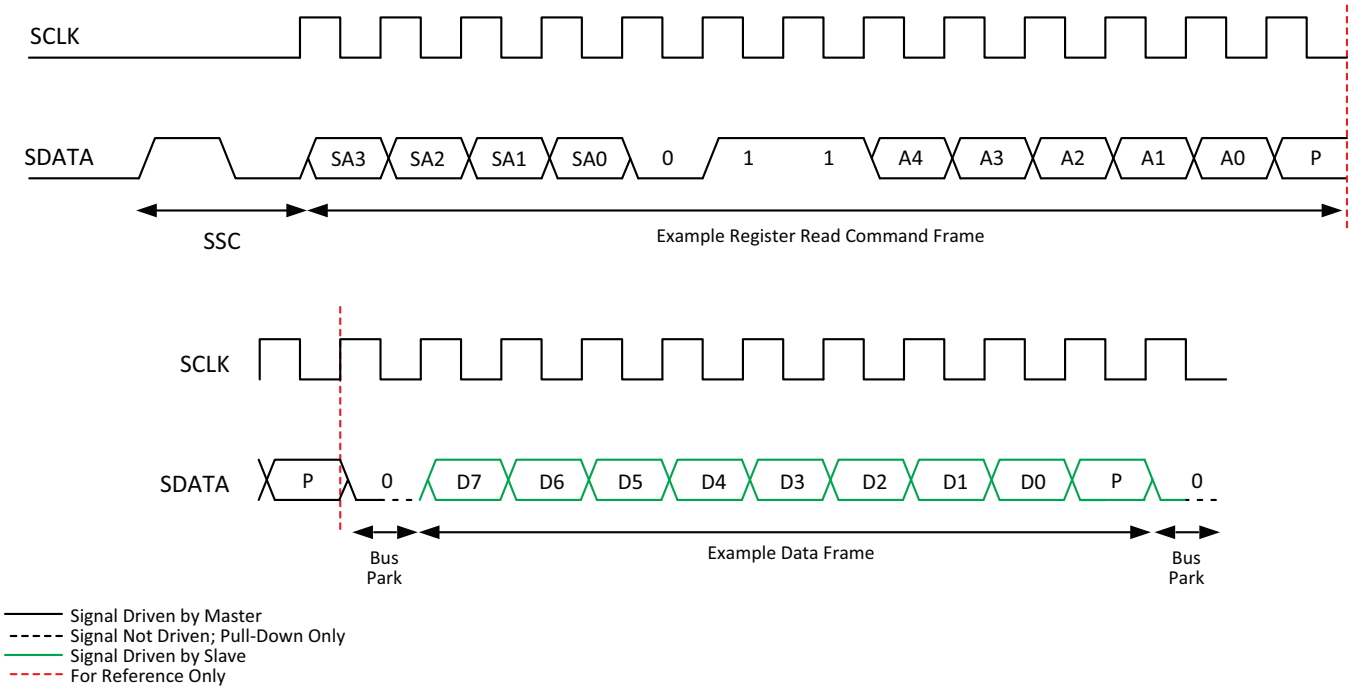


Figure 6. Register Read Command Timing Diagram

Table 9. Register_0 Truth Table

State	Mode	Dregister_0_Bits Bits							
		D7	D6	D5	D4	D3	D2	D1	D0
1	Isolation (default)	X	0	0	0	0	0	0	0
2	ANT-TRX1	X	0	0	0	0	0	1	0
3	ANT-TRX2	X	0	0	0	1	0	1	0
4	ANT-TRX3	X	0	0	0	1	1	1	0
5	ANT-TRX4	X	0	0	0	1	0	1	1
6	ANT-TRX5	X	0	0	0	0	0	0	1
7	ANT-TRX6	X	0	0	0	1	0	0	1
8	ANT-TRX7	X	0	0	0	0	1	1	0
9	ANT-TRX8	X	0	0	0	0	1	0	0
10	ANT-TRX9	X	0	0	0	1	1	0	0
11	ANT-TRX10	X	0	0	0	1	0	0	0
12	ANT-TRX1 + TRX2	0	0	0	1	0	0	0	0
13	ANT-TRX1 + TRX3	0	0	0	1	0	0	0	1
14	ANT-TRX1 + TRX4	0	0	0	1	0	0	1	0
15	ANT-TRX1 + TRX5	0	0	0	1	0	0	1	1
16	ANT-TRX1 + TRX6	0	0	0	1	0	1	0	0
17	ANT-TRX1 + TRX7	0	0	0	1	0	1	0	1
18	ANT-TRX1 + TRX8	0	0	0	1	0	1	1	0
19	ANT-TRX1 + TRX9	0	0	0	1	0	1	1	1
20	ANT-TRX1 + TRX10	0	0	0	1	1	0	0	0
21	ANT-TRX2 + TRX3	0	0	0	1	1	0	0	1
22	AN-TRX2 + TRX4	0	0	0	1	1	0	1	0
23	ANT-TRX2 + TRX5	0	0	0	1	1	0	1	1
24	ANT-TRX2 + TRX6	0	0	0	1	1	1	0	0
25	ANT-TRX2 + TRX7	0	0	0	1	1	1	0	1
26	ANT-TRX2 + TRX8	0	0	0	1	1	1	1	0
27	ANT-TRX2 + TRX9	0	0	0	1	1	1	1	1
28	ANT-TRX2 + TRX10	0	0	1	0	0	0	0	0
29	ANT-TRX3 + TRX4	0	0	1	0	0	0	0	1
30	ANT-TRX3 + TRX5	0	0	1	0	0	0	1	0
31	ANT-TRX3 + TRX6	0	0	1	0	0	0	1	1
32	ANT-TRX3 + TRX7	0	0	1	0	0	1	0	0
33	ANT-TRX3 + TRX8	0	0	1	0	0	1	0	1

Table 9. Register_0 Truth Table (Continued)

State	Mode	Dregister_0_Bits Bits							
		D7	D6	D5	D4	D3	D2	D1	D0
34	ANT-TRX3 + TRX9	0	0	1	0	0	1	1	0
35	ANT-TRX3 + TRX10	0	0	1	0	0	1	1	1
36	ANT-TRX4 + TRX5	0	0	1	0	1	0	0	0
37	ANT-TRX4 + TRX6	0	0	1	0	1	0	0	1
38	ANT-TRX4 + TRX7	0	0	1	0	1	0	1	0
39	ANT-TRX4 + TRX8	0	0	1	0	1	0	1	1
40	ANT-TRX4 + TRX9	0	0	1	0	1	1	0	0
41	ANT-TRX4 + TRX10	0	0	1	0	1	1	0	1
42	ANT-TRX5 + TRX6	0	0	1	0	1	1	1	0
43	ANT-TRX5 + TRX7	0	0	1	0	1	1	1	1
44	ANT-TRX5 + TRX8	0	0	1	1	0	0	0	0
45	ANT-TRX5 + TRX9	0	0	1	1	0	0	0	1
46	ANT-TRX5 + TRX10	0	0	1	1	0	0	1	0
47	ANT-TRX6 + TRX7	0	0	1	1	0	0	1	1
48	ANT-TRX6 + TRX8	0	0	1	1	0	1	0	0
49	ANT-TRX6 + TRX9	0	0	1	1	0	1	0	1
50	ANT-TRX6 + TRX10	0	0	1	1	0	1	1	0
51	ANT-TRX7 + TRX8	0	0	1	1	0	1	1	1
52	ANT-TRX7 + TRX9	0	0	1	1	1	0	0	0
53	ANT-TRX7 + TRX10	0	0	1	1	1	0	0	1
54	ANT-TRX8 + TRX9	0	0	1	1	1	0	1	0
55	ANT-TRX8 + TRX10	0	0	1	1	1	0	1	1
56	ANT-TRX9 + TRX10	0	0	1	1	1	1	0	0

Table 10. MIPI® Register Map

Register Address	Register Name	Data Bit	Bit Name	Default	R/W	Description
0x00	MODE_CTRL	7:0	MODE CONTROL	0x0	R/W	Described in Table 9.
0x1C	PM_TRIGGER	7	PWR_MODE[1], Operation Mode	0x0	R/W	0: Normal operation (ACTIVE)
						1: Low power mode (LOW POWER)
		6	PWR_MODE[0], State Bit Vector	0x0	R/W	0: No action (ACTIVE)
						1: Powered reset (STARTUP to ACTIVE to LOW POWER)
		5	Trigger_Mask_2	0x0	R/W	If this bit is set to 1, trigger_2 is disabled
		4	Trigger_Mask_1	0x0	R/W	If this bit is set to 1, trigger_1 is disabled
		3	Trigger_Mask_0	0x0	R/W	If this bit is set to 1, trigger_0 is disabled
		2	Trigger_2	0x0	W	A write of 1 to this bit loads trigger_2 registers
		1	Trigger_1	0x0	W	A write of 1 to this bit loads trigger_1 registers
		0	Trigger_0	0x0	W	A write of 1 to this bit loads trigger_0 registers
0x1D	PRODUCT_ID	7:0	PRODUCT_ID[7:0]	0x0A	R	Product identification
0x1E	MANUFACTURER_ID	7:0	MANUFACTURER_ID[7:0]	0xA5	R	LSB manufacturing identification
0x1F	MAN_USID	7:6	RESERVED	0x0	R	Reserved for future use
		5:4	MANUFACTURER_ID[9:8]	0x1	R	MSB manufacturing identification
		3:0	USID[3:0]	0xA	R/W	Programmable USID. A write to these bits programs the USID
0x20	EXT_PROD_ID	7:0	EXT_PRODUCT_ID[7:0]	0x03	R	
0x21	REV_ID	7:0	REVISION_ID	0x00	R	
0X22	GROUP_SID	7:4	GSID0[3:0]	0x0	R/W	Primary group ID
		3:0	RESERVED	0x0	R	Reserved for secondary group slave ID
0x23	SOFTWARE_RESET	7	UDR_RST	0	R/W	
	RESERVED	6:0	RESERVED	0x00	R/W	Reserved (set to zero)

Table 10. MIPI® Register Map (Continued)

Register Address	Register Name	Data Bit	Bit Name	Default	R/W	Description
0x24	ERR_SUM	7	RESERVED	0	R	Reserved
		6	COMMAND_FRAME_ PARITY_ERR	0	R/W	Command Sequence received with parity error - discard command. The RFFE_STATUS register shall reset after it is read.
		5	COMMAND_LENGTH_ ERR	0		Command length error. The RFFE_STATUS register shall reset after it is read.
		4	ADDRESS_FRAME_ PARITY_ERR	0		Address frame with parity error. The RFFE_STATUS register shall reset after it is read.
		3	DATA_FRAME_PARITY_ERR	0		Data frame with parity error. The RFFE_STATUS register shall reset after it is read.
		2	READ_UNUSED_REG	0		Read command to an invalid address. The RFFE_STATUS register shall reset after it is read.
		1	WRITE_UNUSED_REG	0		Write command to an invalid address. The RFFE_STATUS register shall reset after it is read.
		0	BID_GID_ERR	0		Read command with a BROADCAST_ID or GROUP_ID. The RFFE_STATUS register shall reset after it is read.
0x2B	BUS_LD	7:4	RESERVED	0x00	R/W	Reserved for future use. Set to all 0.
		1:0	BUS_LD[1:0]	0x0		0x0: 50 pF
						0x1: 150 pF
						0x2: 250 pF
						0x3: 350 pF
						RFFE drive strength select. Program the drive strength of the SDATA driver in readback modes
0x2C	TEST_PATT	7:0	TEST_PATT[7:0]	1101 0010	R	A read to this register address will trigger the slave to transmit a fixed pattern of 0xD2

Evaluation Board Description

An evaluation board (EVB) is used to test the performance of the SKY13638-700LF. An EVB schematic is provided in Figure 7. Figure 8 shows recommended ESD protection circuits. An assembly drawing for the evaluation board is shown in Figure 9.

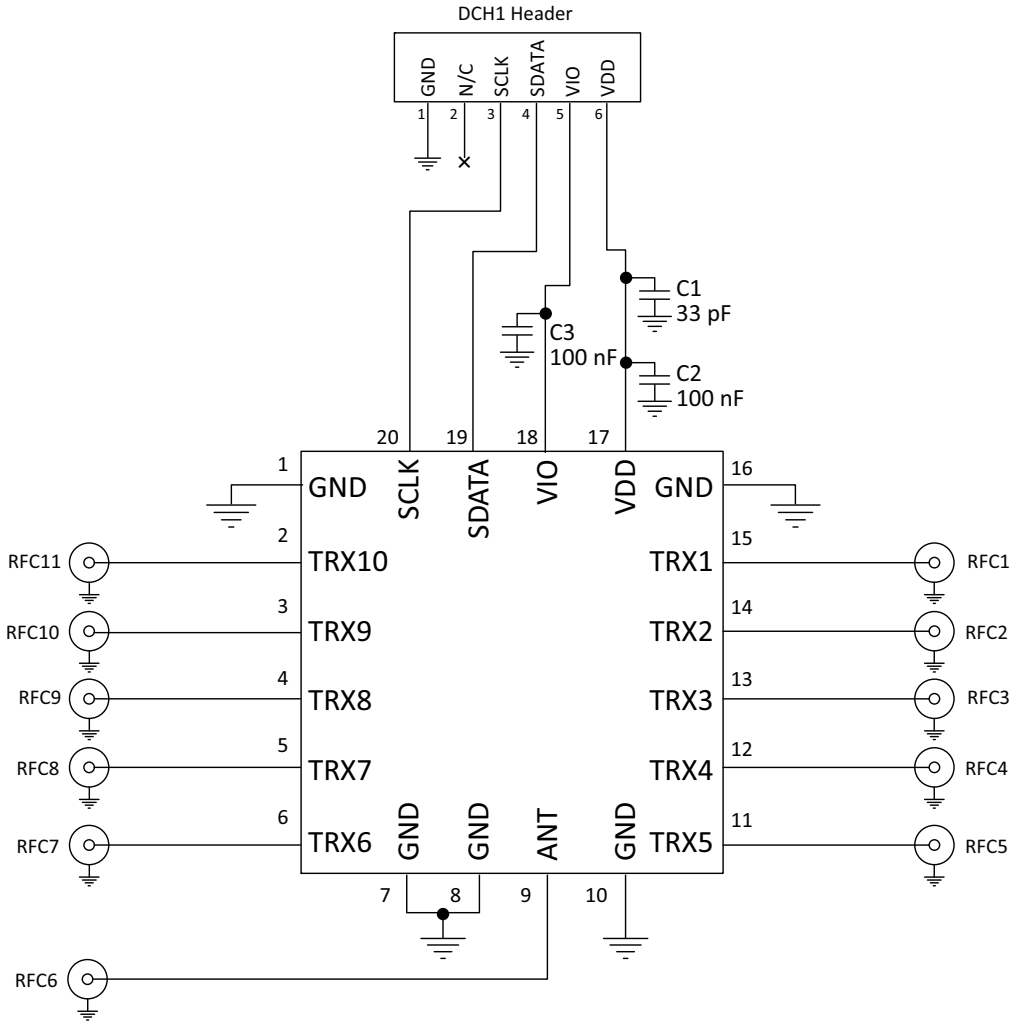
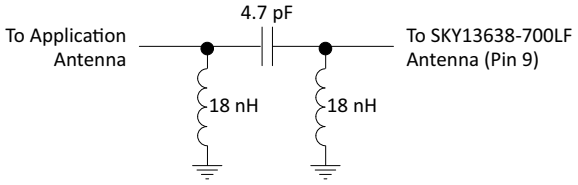
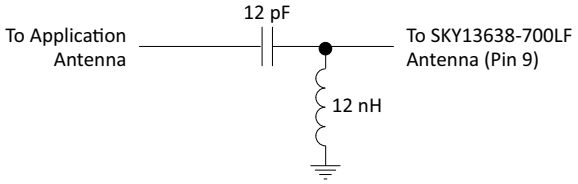


Figure 7. Evaluation Board Schematic



ESD Circuit 1



ESD Circuit 2

Figure 8. Recommended ESD Protection Circuits

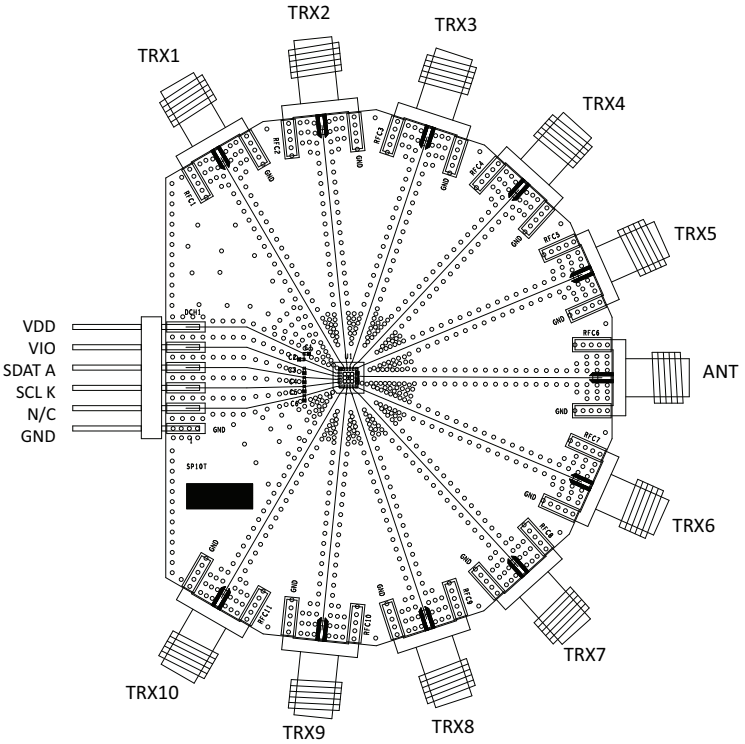


Figure 9. Evaluation Board Assembly Diagram

Package and Handling Information

Instructions on the shipping container label regarding exposure to moisture after the container seal is broken must be followed. Otherwise, problems related to moisture absorption may occur when the part is subjected to high temperature during solder assembly.

The SKY13638-700LF is rated to Moisture Sensitivity Level 1 (MSL1) at 260 °C. It can be used for lead- or lead-free soldering. For additional information, refer to the Skyworks Application Note, “Solder Reflow Information,” document number 200164.

Care must be taken when attaching this product, whether it is done manually or in a production solder reflow environment. Production quantities of this product are shipped in a standard tape and reel format

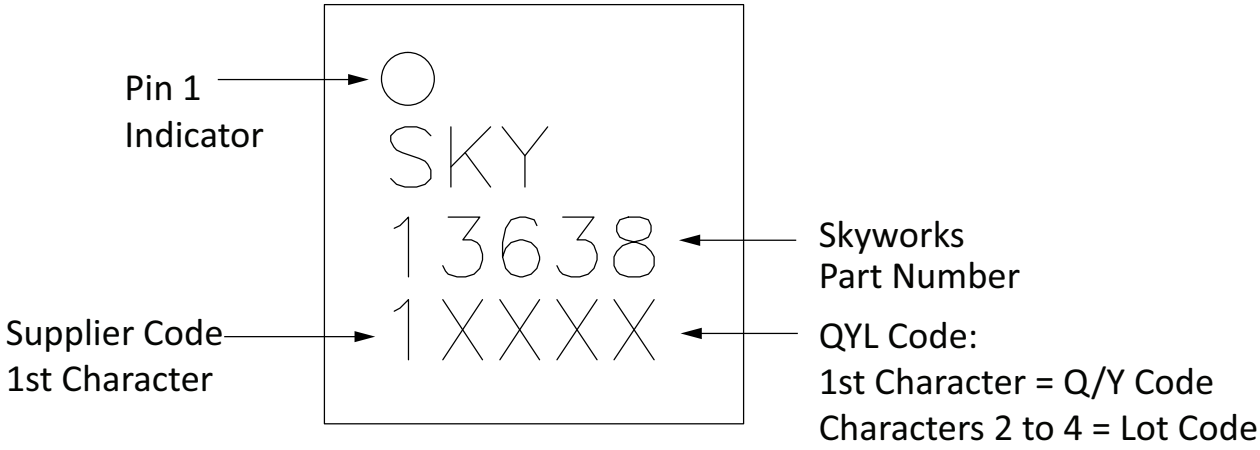
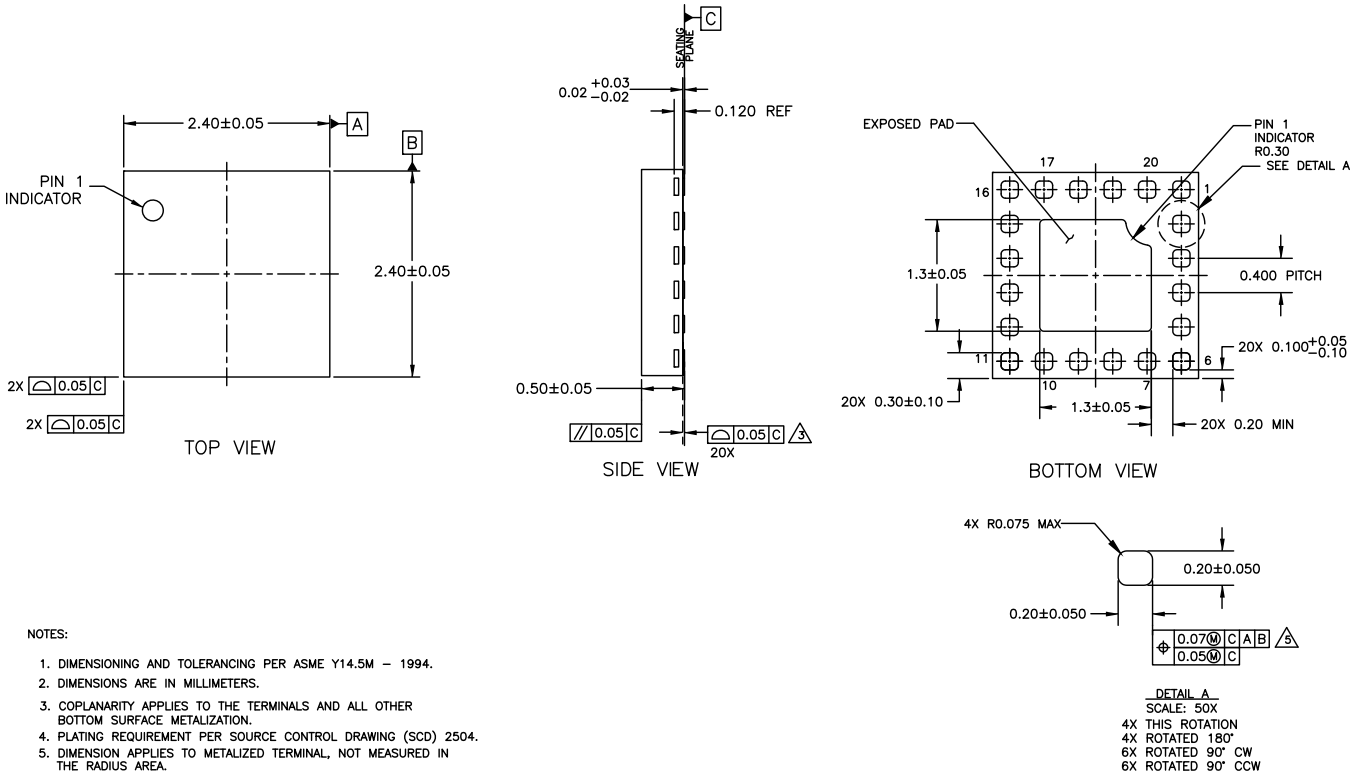


Figure 10. Typical Part Marking



NOTES:

1. DIMENSIONING AND TOLERANCING PER ASME Y14.5M – 1994.
2. DIMENSIONS ARE IN MILLIMETERS.
3. COPLANARITY APPLIES TO THE TERMINALS AND ALL OTHER BOTTOM SURFACE METALIZATION.
4. PLATING REQUIREMENT PER SOURCE CONTROL DRAWING (SCD) 2504.
5. DIMENSION APPLIES TO METALIZED TERMINAL, NOT MEASURED IN THE RADIUS AREA.

Figure 11. Package Dimensions

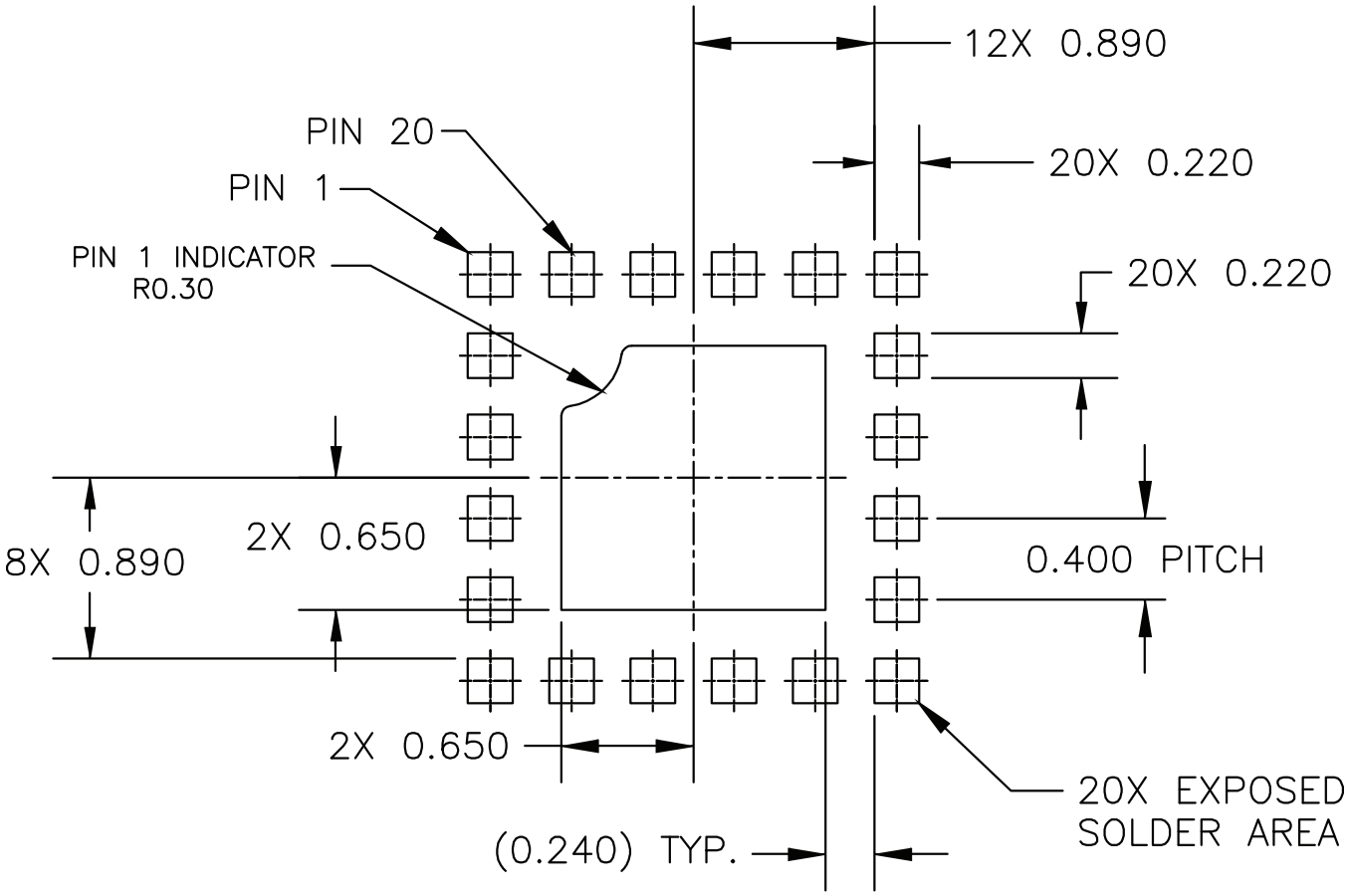
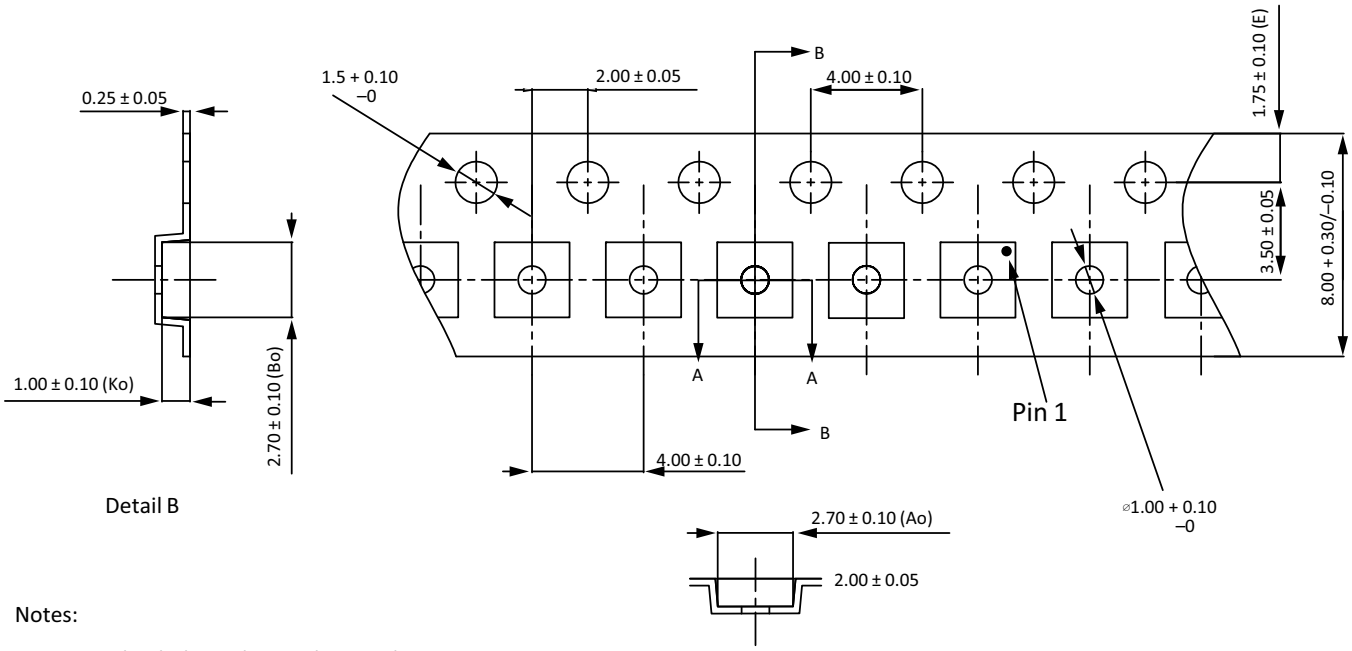


Figure 12. PCB Layout Footprint



Notes:

1. 10-sprocket hole pitch cumulative tolerance: ± 0.20 mm.
2. Ao and Bo measured on plane 0.30 mm above the bottom of the pocket.
3. All dimensions are in millimeters.

Figure 13. Tape and Reel Information

Ordering Information

Part Number	Description	Evaluation Board Part Number
SKY13638-700LF	0.4 to 3.8 GHz SP10T LTE Transmit/Receive Switch with MIPI®	SKY13638-700LFEK1