DATA SHEET

SKYA21050: 750 to 770 MHz Linear Power Amplifier

Automotive Applications

- Japan Intelligent Transport Systems 700 MHz power amplifier (PA): ARIB STD-T109
- LTE Cellular Band 13 PA
- Active distributed antenna system
- Cellular repeaters
- Driver amplifier

Features

- AEC-Q100 grade 3 (–40 °C to +85 °C) qualification in process
- High gain: 35 dB (unconditionally stable)
- High linearity:
  Adjacent channel power (ACP) ≤ –39 dBm/100 kHz with POUT = +23.5 dBm
  (10 MHz signal bandwidth LTE modulated signal)
- RF input and output internally matched to 50 Ω
- Integrated active bias: performance compensated over temp
- Integrated coupler for output power monitoring
- PA on/off function: 4.0 µs switching time
- Single supply voltage: 3.3 V
- Minimal external components
- Level 3 PPAP available at release to production
- Small 5 x 5 mm, 28-pin package
- (MSL3, 260 °C per JEDEC J-STD-020)
- For RoHS and other product compliance information, see the Skyworks Certificate of Conformance.

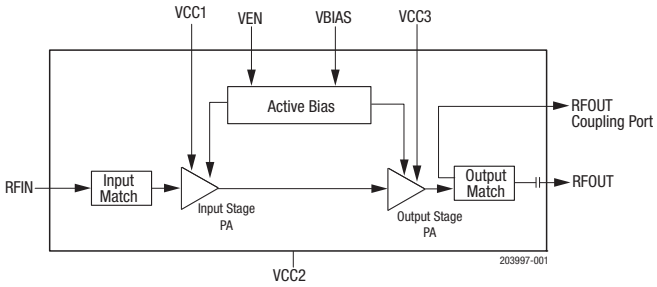


Figure 1. Functional Block Diagram

Description

The SKYA21050 is a high-linearity PA with fully matched input/output and high gain. The compact 5 x 5 mm PA is designed for the Japan market 760 MHz vehicle-to-vehicle and infrastructure communication based on the ARIB STD-T109.

The active biasing circuitry is integrated to compensate PA performance over temperature, voltage, and process variation as well as an internal coupler for power monitoring.

A block diagram of the SKYA21050 is shown in Figure 1. The device package and pinout are shown in Figure 2.

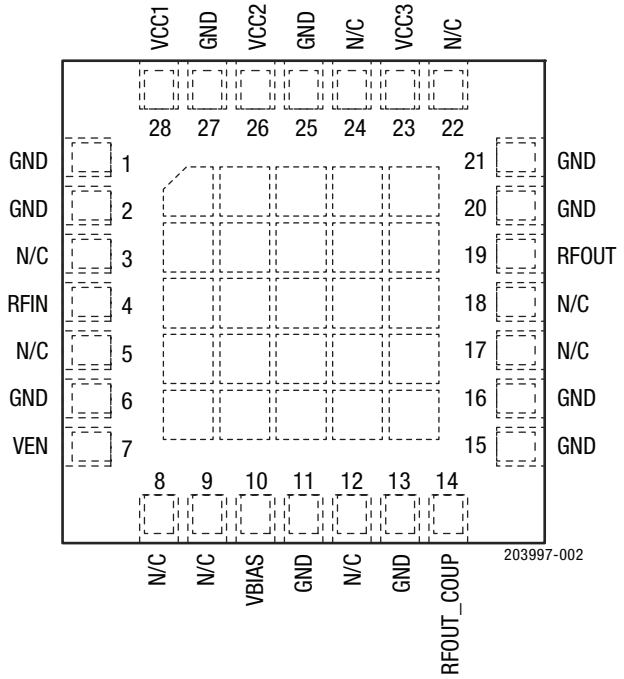


Figure 2. Pinout (Top View)

Table 1. Pinout Descriptions

Pin	Name	Description	Pin	Name	Description
1	GND	Ground	15	GND	Ground
2	GND	Ground	16	GND	Ground
3	N/C	No internal connection	17	N/C	No internal connection
4	RFIN	RF input	18	N/C	No internal connection
5	N/C	No internal connection	19	RFOUT	RF output
6	GND	Ground	20	GND	Ground
7	VEN	Enable (active low)	21	GND	Ground
8	N/C	No internal connection	22	N/C	No internal connection
9	N/C	No internal connection	23	VCC3	Output stage supply voltage
10	VBIAS	Bias voltage	24	N/C	No internal connection
11	GND	Ground	25	GND	Ground
12	N/C	No internal connection	26	VCC2	No internal connection
13	GND	Ground	27	GND	Ground
14	RFOUT_COUP	RF output coupling port	28	VCC1	Input stage supply voltage

Technical Description

The SKYA21050 PA contains all of the needed RF matching and DC biasing circuits. This two-stage device is optimized for high linearity and power efficiency. These features make the device suitable for wideband applications where PA linearity and power consumption are of critical importance.

The device is designed for standard ARIB STD-T109 modulated signals. Under these stringent test conditions, the device exhibits excellent spectral purity and power efficiency.

Electrical Specifications

The absolute maximum ratings of the SKYA21050 are provided in Table 2. The recommended operating conditions are specified in Table 3, and electrical specifications are provided in Table 4.

Typical performance characteristics are shown in Figures 3 through 12.

Table 2. Absolute Maximum Ratings [1]

Parameter	Symbol	Minimum	Maximum	Units
Supply voltage (VCC)	V_{CC}	0	+4.0	V
Total supply current	I_{CC}		700	mA
Logic control input voltage (VEN)	V_{EN}	–0.5	3.6	V
Case operating temperature[2]	T_C[2]	–40	+100	°C
Storage temperature	Tstg	–55	+150	°C
Junction temperature	Tj		+150	°C
Thermal resistance	θ_{JC}		21	°C/W
Power dissipation	P_{DISS}		2.3	W
Electrostatic discharge: Charged Device Model (CDM) Human Body Model (HBM)	ESD		 500 150	 V V

1. Exposure to maximum rating conditions for extended periods may reduce device reliability. There is no damage to the device with only one parameter set at the limit and all other parameters set at or below their nominal value. Exceeding any of the limits listed here may result in permanent damage to the device.
2. Case operating temperature (Tc) refers to the temperature of the bottom ground pad.

ESD Handling: Industry-standard ESD handling precautions must be adhered to at all times to avoid damage to this device.

Table 3. Recommended Operating Conditions [1]

Parameter	Symbol	Minimum	Typical	Maximum	Units
Frequency range	f	750		770	MHz
Supply voltage (VCC1, VCC2, VCC3)[2]	VCC	3.1	3.3	3.6	V
PA enable control voltage (active low): Disable Enable	 VENH VENL	 1.5 0		 3.6 0.6	 V V
PA enable current (@ PAEN = 3.6 V)	IEN			<1	mA
Case operating temperature	TC	–40		+85	°C

1. Exposure to maximum rating conditions for extended periods may reduce device reliability. Exceeding any of the limits listed here may result in permanent damage to the device.
2. Voltage levels measured at the pads of the package. The evaluation board supply voltage levels may be different.

Table 4. Electrical Specifications[1]

(VCC = +3.3 V, TC = +25 °C, f = 760 MHz, Characteristic Impedance [ZO] = 50 Ω, VEN = 0 V, Unless Otherwise Noted)

Parameter	Symbol	Test Condition	Min	Typ	Max	Units
Gain	G@+23.5 dBm	CW, POUT = +23.5 dBm	35	37		dB
Input return loss	|S11|	CW, PIN = –30 dBm	7.5	9		dB
Output return loss	|S22|	CW, PIN = –30 dBm, 750 to 770 MHz	10	15		dB
Quiescent current	ICQ	No RF		155	185	mA
Operating current	ICC	CW, POUT = +23.5 dBm		510	600	mA
Power-down current	IPD	VEN = 2.5 V		0.1	0.5	mA
Adjacent channel power: ACP/100 kHz @ 750 MHz ACP/100 kHz @ 770 MHz	 ACPLO ACPHI	 Measured with 10 MHz BW, LTE waveform POUT = +23.5 dBm, VCC = 3.1 V and 3.6 V		 –38 –41	 –35 –38	 dBm/100 kHz dBm/100 kHz
Output P1dB[2]	OP1dB	CW, Referenced to Gain, POUT = +23.5 dBm		+31		dBm
Power-added efficiency	PAE	CW, POUT = +23.5 dBm	11	13		%
Output coupling factor	CPLOUT	CW, POUT = +23.5 dBm	16.5	18.5	20.5	dB
Turn-on time[2]	t_{ON}	Time from VEN = 50% to RF = 90%		4.5	6.5	s
Turn-off time[2]	t_{OFF}	Time from VEN = 50% to RF = 10%		1.0	2.0	s

1. Performance is guaranteed only under the conditions listed in this table.
2. Not tested in production. Verified by characterization.

Typical Performance Characteristics

(VCC = +3.3 V, TC = +25 °C, f = 760 MHz, Characteristic Impedance [ZO] = 50 Ω, VEN = 0 V, Unless Otherwise Noted)

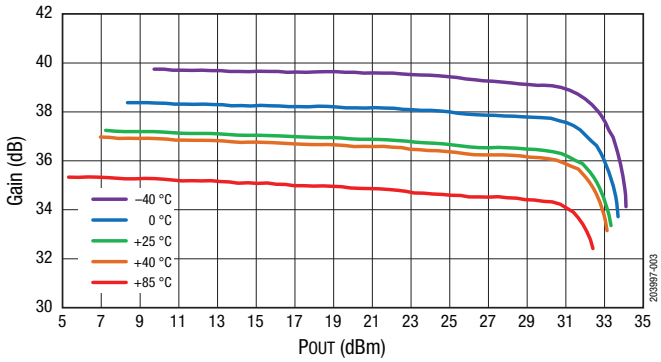


Figure 3. Gain vs. POUT Across Temperature

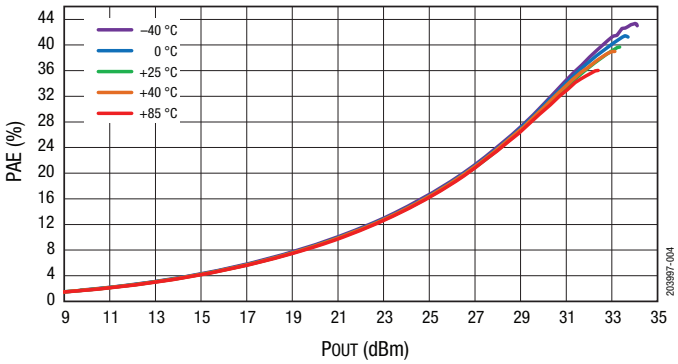


Figure 4. PA vs. POUT Across Temperature

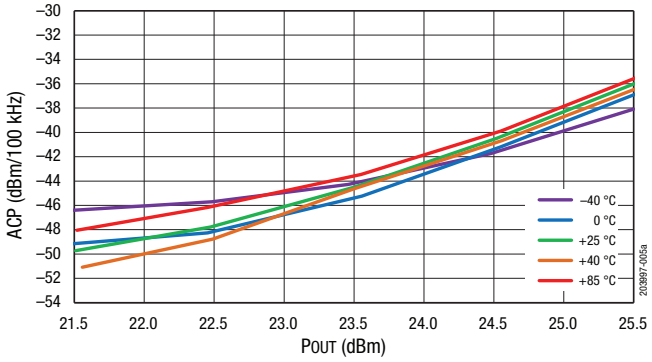


Figure 5. ACP_High (10 MHz) vs. POUT Across Temperature (@760 MHz, 3.3 V)

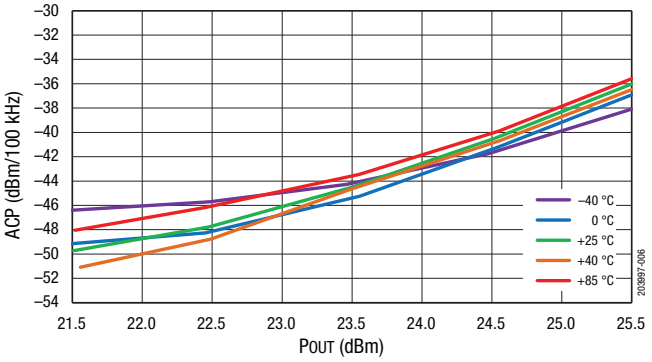


Figure 6. ACP_Low (10 MHz) vs. POUT Across Temperature (@760 MHz, 3.3 V)

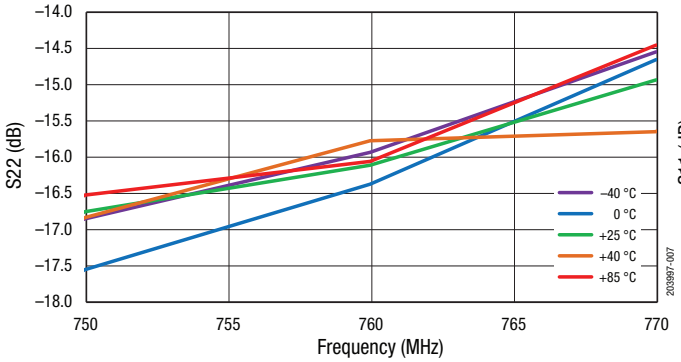


Figure 7. S22 vs. Frequency Across Temperature

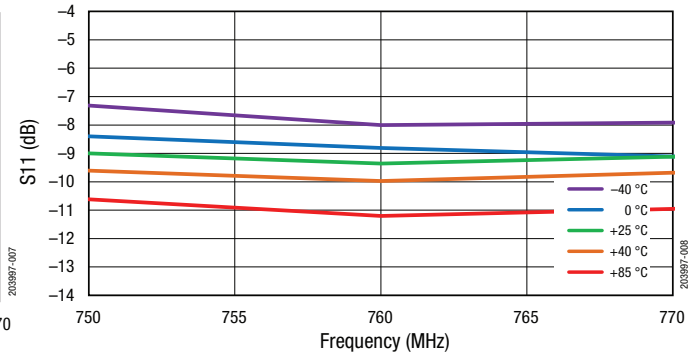


Figure 8. S11 vs. Frequency Across Temperature

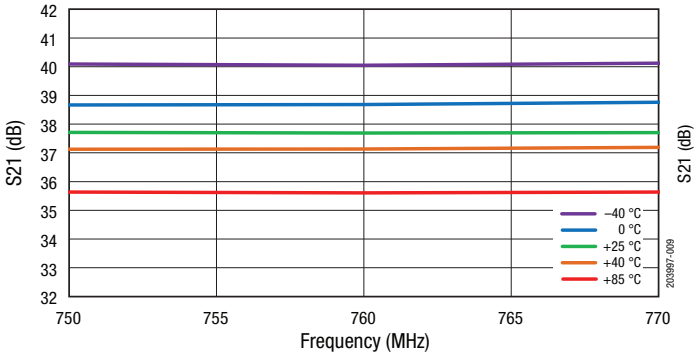


Figure 9. S21 vs. Frequency Across Temperature

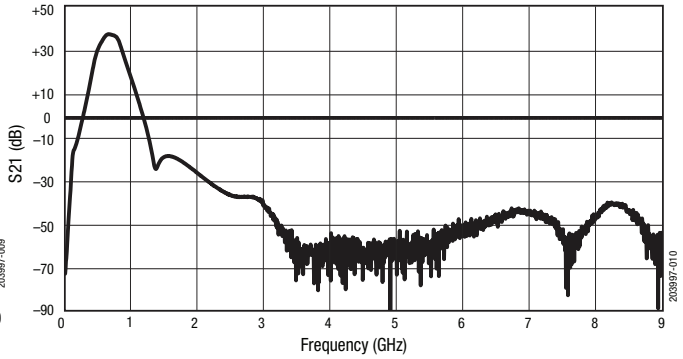


Figure 10. S21 vs. Frequency

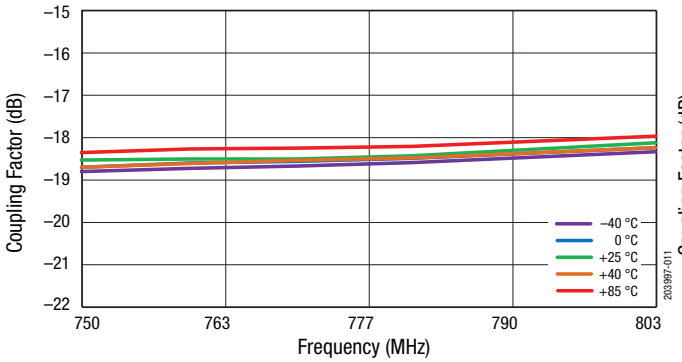


Figure 11. Coupling Factor vs. Frequency Across Temperature

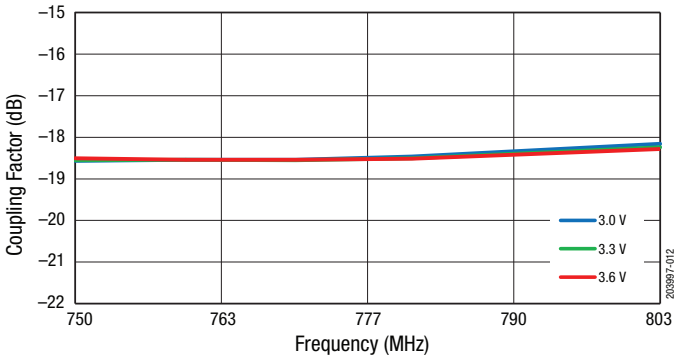


Figure 12. Coupling Factor vs. Frequency Across Power Supply

Evaluation Board Description

The SKYA21050 evaluation board is used to test the performance of the SKYA21050 PA. A typical application schematic diagram is shown in Figure 13. A Bill of Materials for the SKYA21050 evaluation board is listed in Table 6. An assembly drawing for the evaluation board is shown in Figure 14. The board layer detail is shown in Figure 15. The layer detail physical characteristics are shown in Figure 16.

Application Circuit Notes

Center Ground. It is extremely important to sufficiently ground the bottom ground pad of the device for both thermal and stability reasons. Multiple small vias are acceptable and work well under the device if solder migration is an issue.

GND (pins 1, 2, 6, 11, 13, 15, 16, 20, 21, 25, and 27). Attach all ground pins to the RF ground plane with the largest diameter and lowest inductance via that the layout allows. Multiple small vias are acceptable and work well under the device if solder migration is an issue.

VBIAS (pin 10). The bias supply voltage for each stage, nominally set to +3.3 V.

RFOUT (pin 19). Amplifier RF output pin (ZO = 50 Ω). The module includes an onboard internal dc-blocking capacitor. All impedance matching is provided internal to the module.

VCC1 and VCC3 (pins 28 and 23, respectively). Supply voltage for each stage collector bias is nominally set to 3.3 V. Bypass and decoupling capacitors C1, C2, C5, and C6 should be placed in the approximate location shown on the evaluation board assembly drawing, although exact placement is not critical.

RFIN (pin 4). Amplifier RF input pin (Zo = 50 Ω). The module includes an onboard internal dc-blocking capacitor. All impedance matching is provided internal to the module.

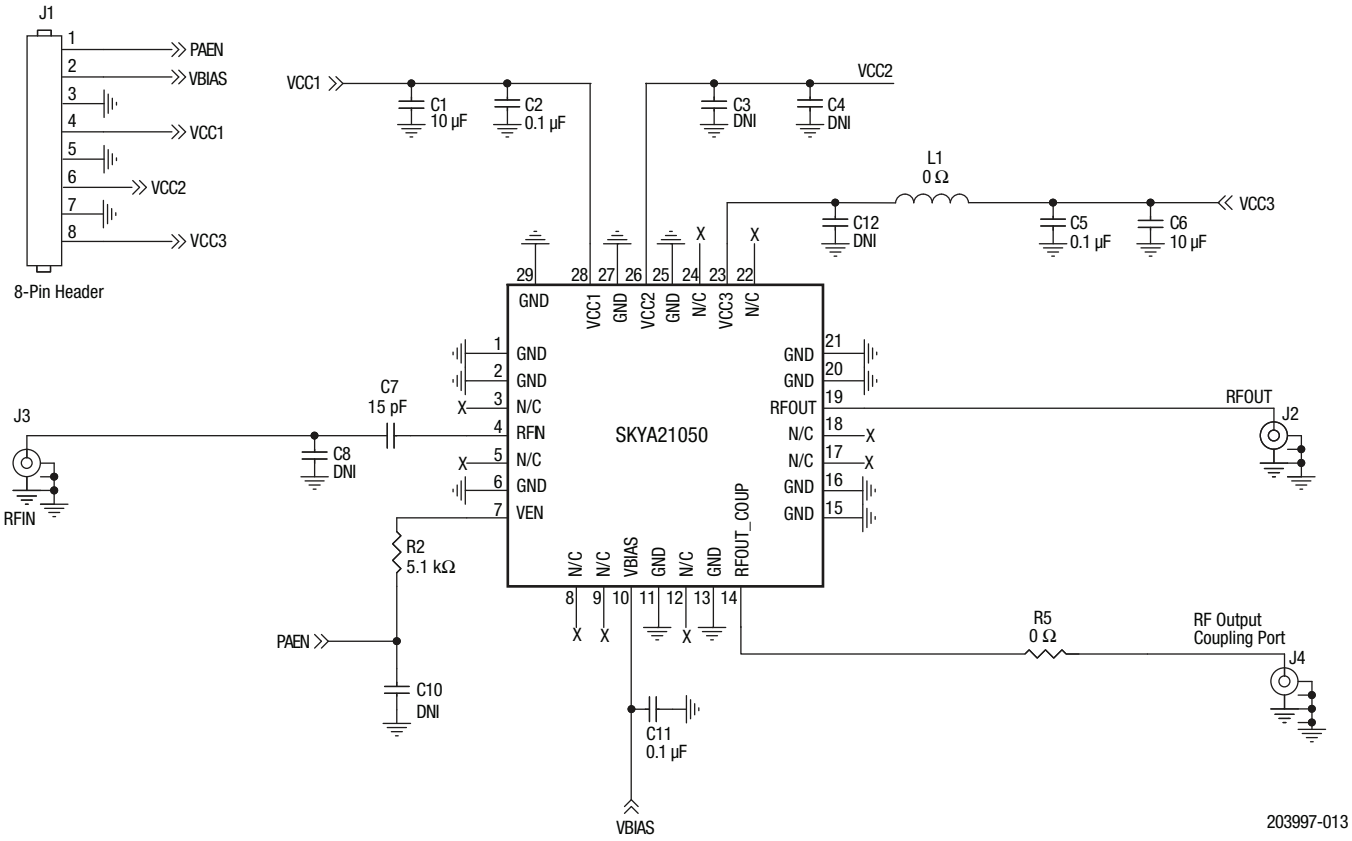
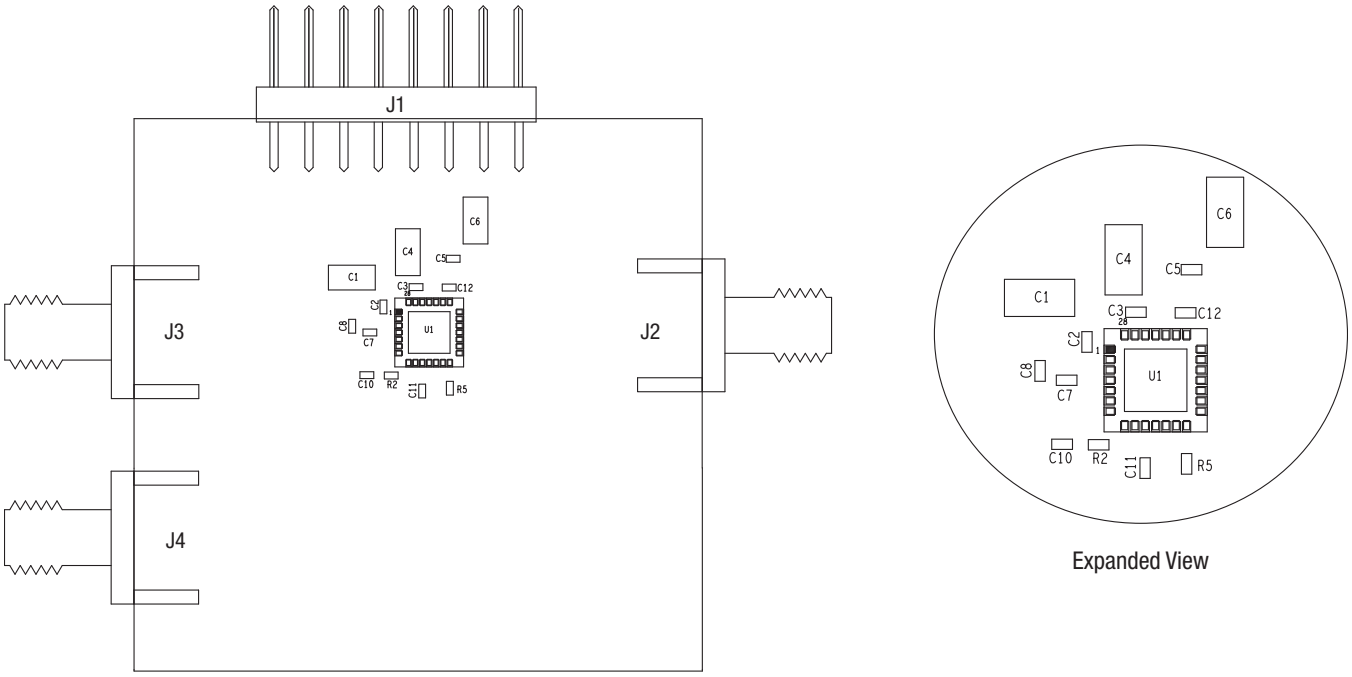


Figure 13. Application Schematic

Table 5. Evaluation Board Bill of Materials (BOM)

Quantity	Component	Size	Part Number	Description
2	C1, C6	1206	C1206X7R160-106KNE	Capacitor, 10 µF, 16 V, ±10%, X7R
3	C2, C5, C11	0402	GRM155R71C104KA88	Ceramic capacitor, 0.1 µF, 10%, X7R, 16 V
5	C3, C4, C8, C10, C12		DNI	DNI
1	C7	0402	GRM1555C1H150JZ01J	Capacitor, 15 pF, 5%, 0.063 W
1	L1	0603	RM73ZIJ000	Resistor, 0 Ω, 5%
1	R2	0402	ERJ2GEJ512	Resistor, 5100 Ω, 5%, 0.063 W
1	R5	0402	ERJ2GE0R00	Resistor, 0 Ω, jumper, 0.063 W
1		PCB	TW22-D115-002	SKYA21050 evaluation board



Notes:

The C3 and C4 components are not required.
Some of the other components shown are optional.

Figure 14. Evaluation Board Assembly Diagram

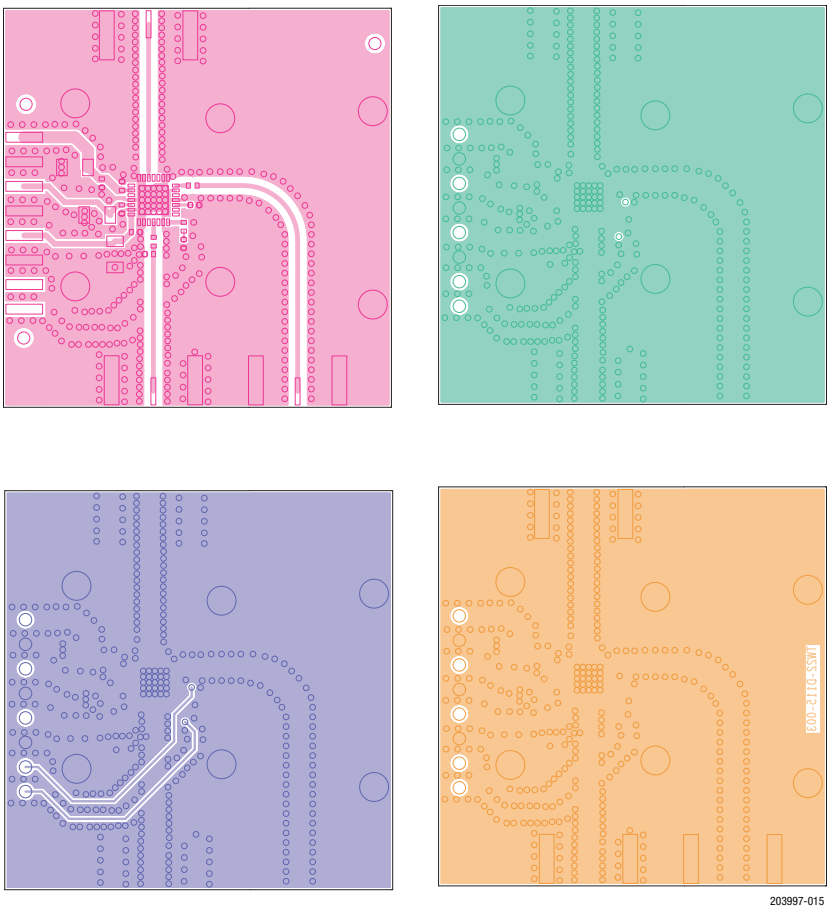


Figure 15. Board Layer Detail

Cross Section	Name	Thickness (mm)	Material
	Top Solder Mask	0.010	Solder Resist
	L1	0.035	Cu – 1 oz
	Dielectric	0.250	Rogers RO4350B
	L2	0.035	Cu – 1 oz
	Dielectric	0.500	FR4
	L3	0.035	Cu – 1 oz
	Dielectric	0.250	FR4
	L4	0.035	Cu – 1 oz
	Bottom Solder Mask	0.010	Solder Resist

203997-016

Figure 16. Layer Detail Physical Characteristics

Package and Handling Information

Since the device package is sensitive to moisture absorption, it is baked and vacuum packed before shipping. Instructions on the shipping container label regarding exposure to moisture after the container seal is broken must be followed. Otherwise, problems related to moisture absorption may occur when the part is subjected to high temperature during solder assembly.

The SKYA21050 is rated to Moisture Sensitivity Level 3 (MSL3) at 260 °C. It can be used for lead or lead-free soldering. For additional information, refer to the Skyworks Application Note, *PCB Design and SMT Assembly/ Rework Guidelines for MCM-L Packages*, document number 101752.

Care must be taken when attaching this product, whether it is done manually or in a production solder reflow environment. Production quantities of this product are shipped in a standard tape and reel format.

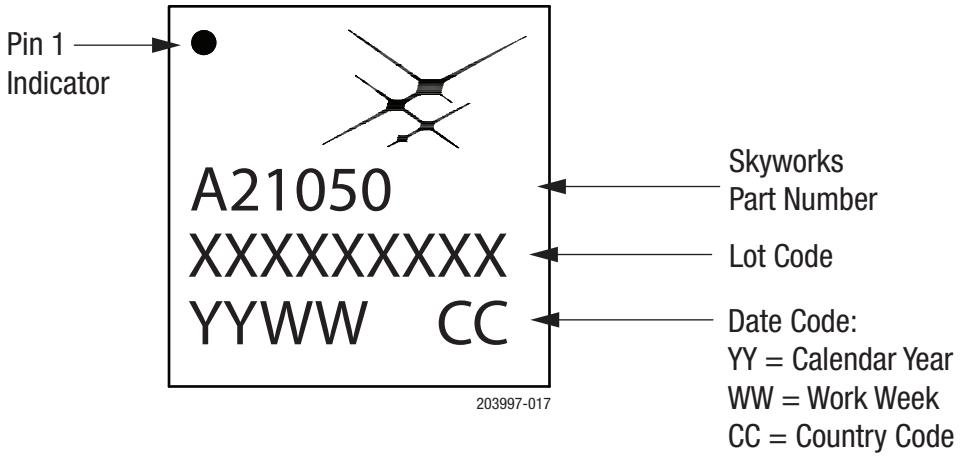


Figure 17. Typical Part Marking

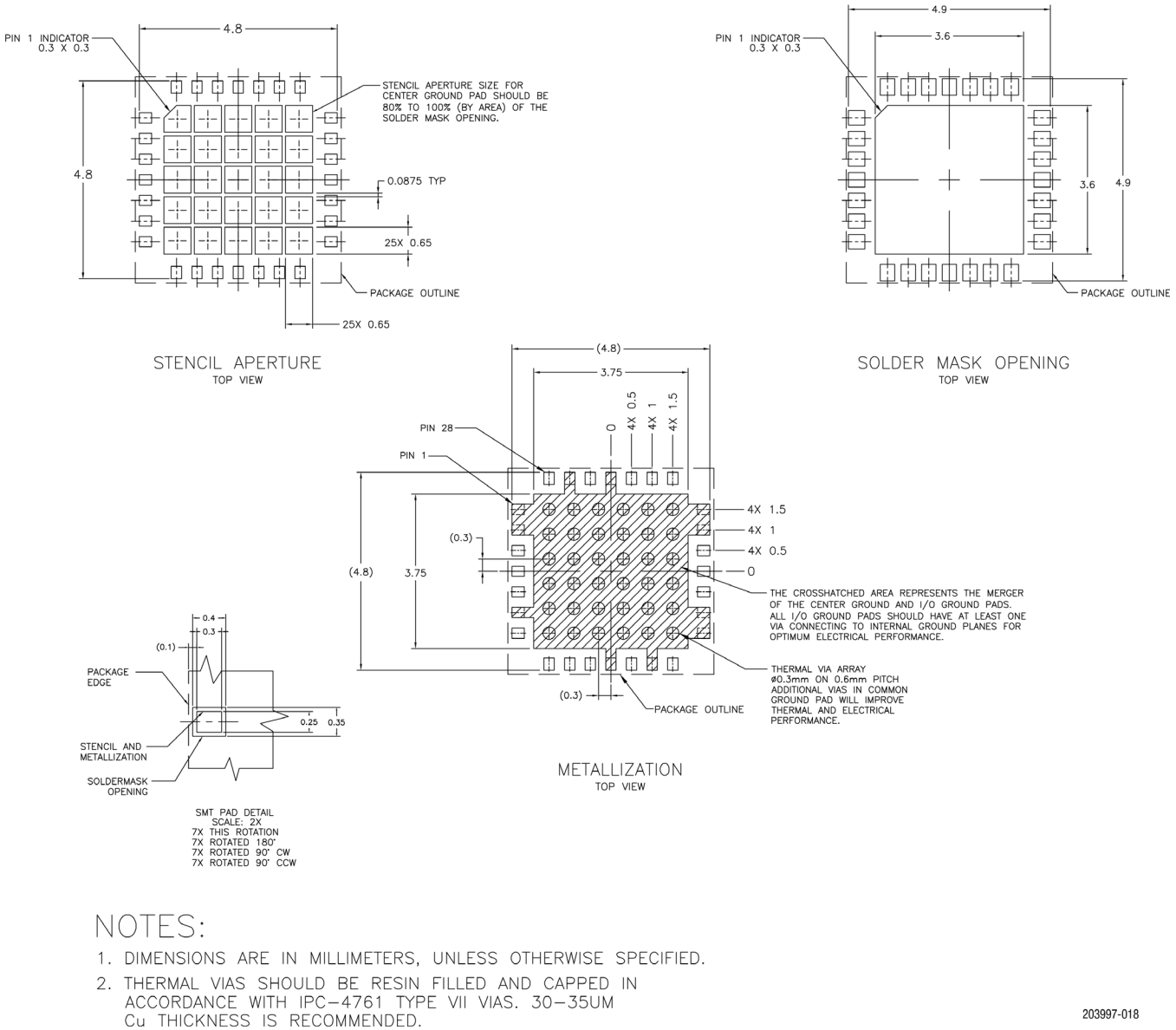


Figure 18. PCB Layout Footprint (Top View)

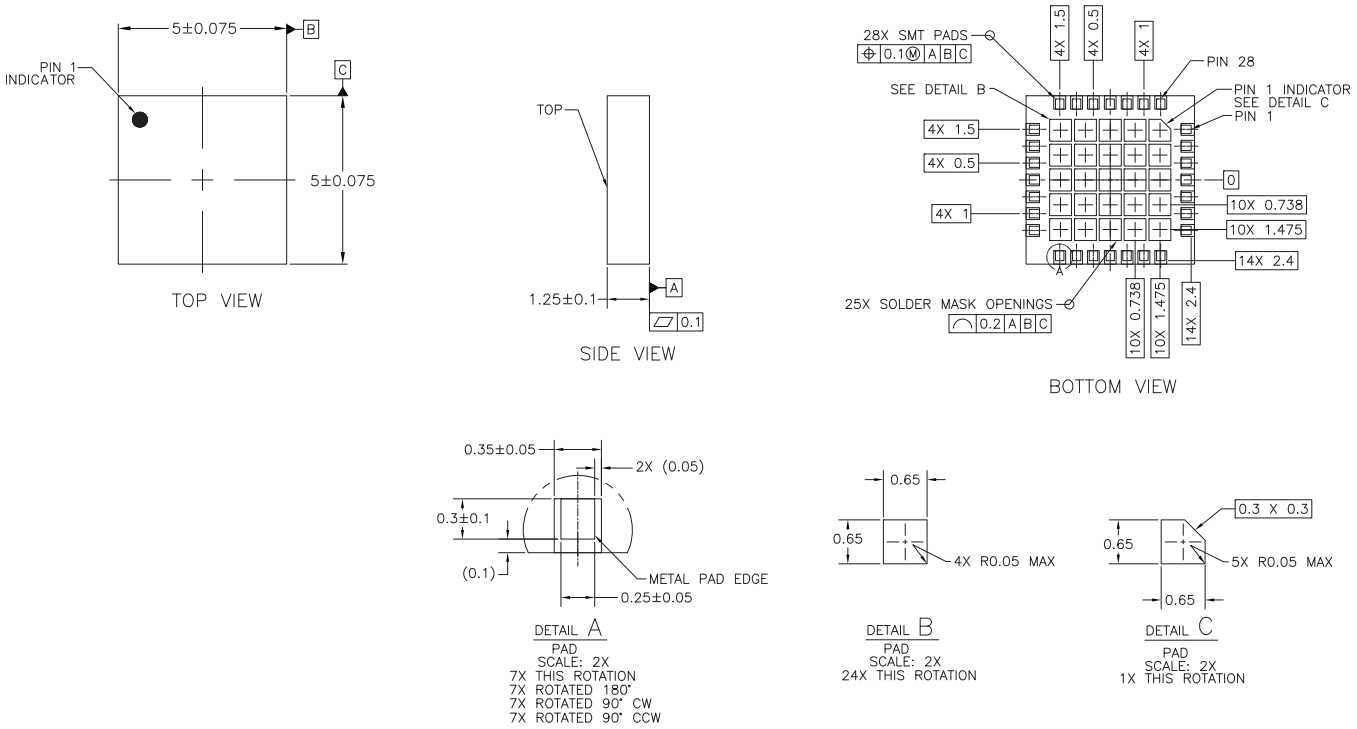
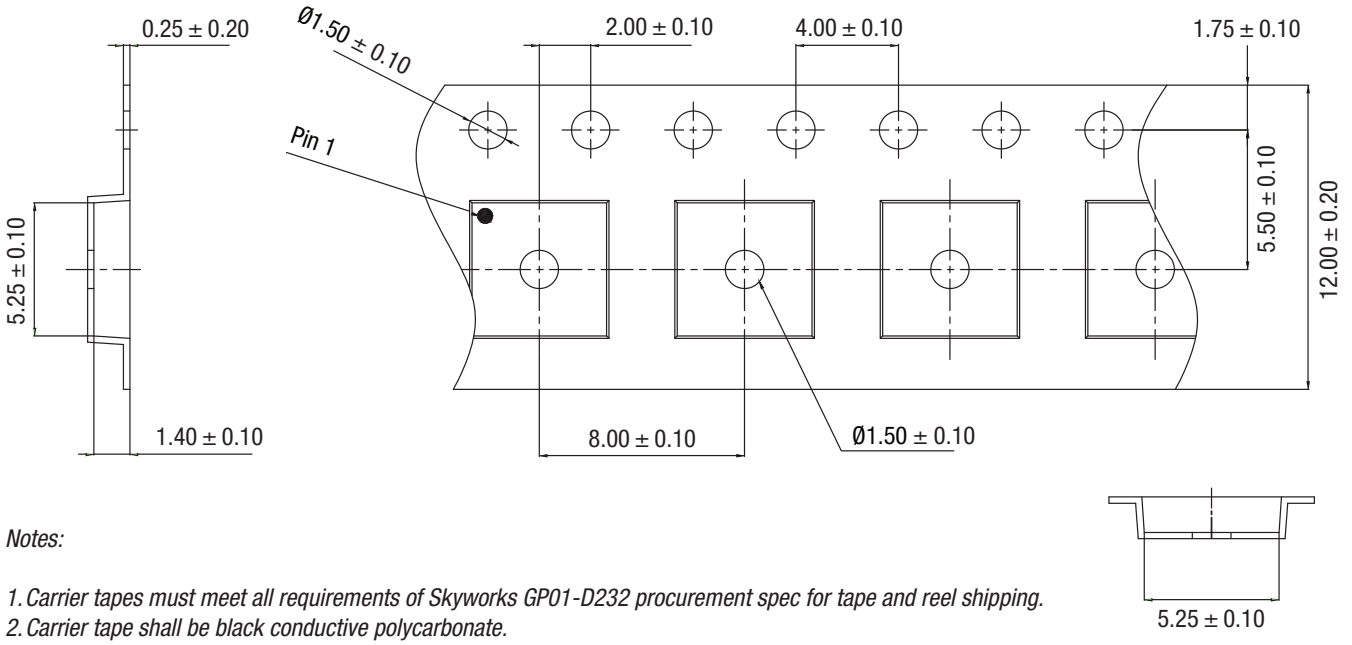


Figure 19. Package Dimensions



Notes:

1. Carrier tapes must meet all requirements of Skyworks GP01-D232 procurement spec for tape and reel shipping.
2. Carrier tape shall be black conductive polycarbonate.
3. Cover tape shall be transparent conductive material.
4. ESD-surface resistivity shall be ≤ 1 × 10^{10} Ω/square per EJA, JEDEC TNR specification.
5. All measurements are in millimeters.

203997-020

Figure 20. Tape and Reel Information

Ordering Information

Part Number	Description	Evaluation Board Part Number
SKYA21050	750 to 770 MHz Linear Power Amplifier	SKYA21050-EK1

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