DATA SHEET

SKY65111-348LF: 600 to 1100 MHz ISM Band Two-Watt InGaP HBT Power Amplifier

Applications

- Automatic meter readers
- Radio Frequency Identification (RFID)

Features

- Optimized for 600 to 1100 MHz operation
- Output power greater than 33 dBm @915 MHz
- 3.5 V nominal operating voltage
- Integrated analog power control voltage:
  - V_{APC} = 2.5 V to 2.8 V in high power mode
- < 10 µA in standby mode
- High Power Added Efficiency (PAE) at maximum output power
- Three-stage Power Amplifier (PA), 16-pin Micro-Leadframe Package Quad (MLPQ), 3.0 x 3.0 x 0.75 mm, (MSL1 @ 260 °C per JEDEC J–STD–020)
- For RoHS and other product compliance information, see the Skyworks Certificate of Conformance.

Description

The SKY65111-348LF is a high-performance three-stage, high-power amplifier IC designed for use in the 600 to 1100 MHz ISM band. The device has an integrated analog power control voltage for achieving required output power.

The device is manufactured using an advanced InGaP HBT process. The SKY65111-348LF is packaged in a thermally enhanced, ultrasmall, micro lead frame package.

For sales information and purchasing availability, see Skyworks online.

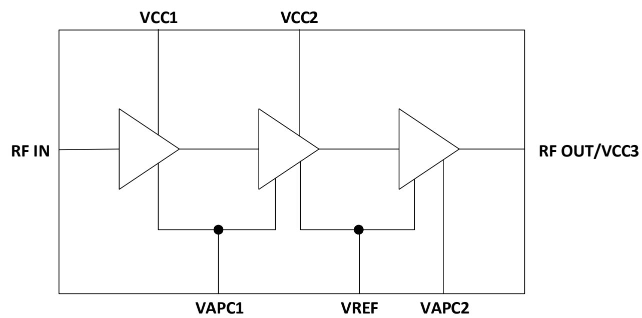


Figure 1. Functional Block Diagram

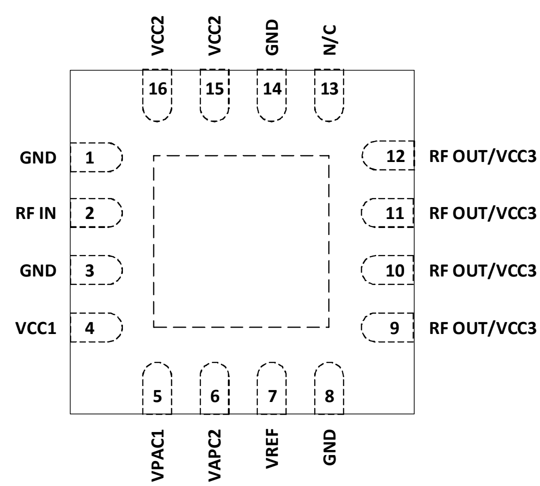


Figure 2. Pinout (Top View)

Pin Assignments

Table 1. Pin Assignments

Pin	Symbol	Description
1, 3, 8, 14	GND	Connect this pin to the printed circuit board common via with lowest possible impedance.
2	RF IN	RF input port.
4	$V_{CC}1$	DC power supply input to the first gain stage.
5	$V_{APC}1$	Power control voltage input to the first and second gain stages.
6	$V_{APC}2$	Power control voltage input to the third gain stage.
7	V_{REF}	Control voltage input to bias control circuit.
9, 10, 11, 12	RF OUT/ $V_{CC}3$	RF output ports and dc supply voltage inputs to third gain stage.
13	NC	No connection. Do not connect this pin to ground.
15, 16	$V_{CC}2$	DC power supply input to the second gain stage.

Electrical and Mechanical Specifications

Table 2. Absolute Maximum Ratings[1]

Characteristic	Value
Supply voltage (V_{CC} and V_{REF})	5.5 V
Power control voltage ($V_{APC}1$ and $V_{APC}2$)	3.0 V
RF input power	10 dBm
Operating temperature	–40 °C to +85 °C
Storage temperature	–65 °C to +150 °C
ESD CDM (Charge Device Model), Class C0B	150 V
ESD HBM (Human Body Model), Class 0	200 V

1. Exposure to maximum rating conditions for extended periods may reduce device reliability. Exceeding any of the limits listed here may result in permanent damage to the device.

***ESD Handling:** Industry-standard ESD handling precautions must be adhered to at all times to avoid damage to this device.*

Table 3. General dc Electrical Specifications

Parameter	Symbol	Condition	Min.	Typ.	Max.	Unit
Supply voltage	V_{CC}		2.5	3.5	5	V
Power control voltage: High power mode	V_{APC}		2.5	2.7	2.8	V
Power control voltage: Standby mode				0	0.1	
Power control current	IV_{APC}				5	mA
Leakage current		P_{IN} < –30 dBm, V_{APC}1, 2 = 0.1 V			10	µA
Thermal resistance	R_{TH}			50		° C/W

Table 4. Assured Performance [1]

V_{CC} = 3.5 V, V_{REF} = 3.5 V, V_{APC} = 2.7 V, T_A = 25 °C

Parameter	Symbol	Condition	Specification	Unit
Critical gain	$\lvert S_{21} \rvert$	902 to 928 MHz, –30 dBm input	36 min.	dB
Saturated power	P_{SAT}	915 MHz	30 min.	dBm

1. Assured performance is as measured in the application's PC board as defined in this data sheet.

Table 5. General RF Transmit Electrical Specifications

V_{CC} = 3.5 V, V_{REF} = 3.5 V, V_{APC} = 2.7 V, P_{IN} = –30 dBm, T_A = 25 °C

Parameter	Symbol	Condition	Min.	Typ.	Max.	Unit
Frequency range	F		902		928	MHz
Gain	S_{21}	Small signal		40		dB
Gain variation over frequency	$\lvert \Delta S_{21} \rvert$	Small signal		0.3		dB
Input return loss	$\lvert S_{11} \rvert$	Small signal		12		dB
Output return loss	$\lvert S_{22} \rvert$	Small signal		15		dB
Quiescent current	I_{CQ}	(No RF signal)		0.25		A
Output $P_{1\ dB}$	$P_{1\ dB}$	CW		29.5		dBm
Current consumption	I_{CC}	Output $P_{1\ dB}$		0.7		A
Saturated power @ 915 MHz	P_{SAT}	V_{CC} = 3.5 V, V_{REF} = 3.5 V, V_{APC}1, 2 = 2.7 V		33		dBm
Power added efficiency	PAE	P_{SAT}		50		%
Second harmonic	F_2	Output $P_{1\ dB}$		–28		dBm
Third harmonic	F_3	Output $P_{1\ dB}$		–38		dBm
Ruggedness		Output VSWR = 8:1, All phase angles, V_{CC} = 5 V, P_{IN} = –5 dBm, V_{APC} = 2.7 V V_{REF} = 5 V	No module damage or permanent performance degradation			
Stability		Output VSWR = 8:1, All phase angles, V_{CC} = 5 V, P_{IN} = –10 dBm, V_{APC} = 2.7 V V_{REF} = 5 V		–36		dBm

Table 6. General RF Transmit Electrical Specifications

V_{CC} = 3.5 V, V_{REF} = 3.5 V, V_{APC} = 2.7 V, P_{IN} = –30 dBm, T_A = 25 °C

Parameter	Symbol	Condition	Min.	Typ.	Max.	Unit
Frequency range	F		600		1100	MHz
Gain	S_{21}	Small signal		39.5		dB
Gain variation over frequency	$\|\Delta S_{21}\|$	Small signal		1.0		dB
Input return loss	$\|S_{11}\|$	Small signal		11		dB
Output return loss	$\|S_{22}\|$	Small signal		8		dB
Output $P_{1\ dB}$	$P_{1\ dB}$	CW		27		dBm
Quiescent current	I_{CQ}	(No RF signal)		0.25		A
Current consumption	I_{CC}	Output $P_{1\ dB}$		0.7		A
Second harmonic	F_2	Output $P_{1\ dB}$		–17		dBm
Third harmonic	F_3	Output $P_{1\ dB}$		–35		dBm
Ruggedness		Output VSWR = 8:1, All phase angles, V_{CC} = 5 V, P_{IN} = –5 dBm, V_{APC} = 2.7 V V_{REF} = 5 V	No module damage or permanent performance degradation			
Stability		Output VSWR = 8:1, All phase angles, V_{CC} = 5 V, P_{IN} = –10 dBm, V_{APC} = 2.7 V, V_{REF} = 5 V		–36		dBm
Saturated power @ 800 MHz	P_{SAT}	V_{CC} = 3.5 V, V_{REF} = 3.5 V, V_{APC}1, 2 = 2.7 V		32		dBm
Power added efficiency @ 800 MHz	PAE	P_{SAT}		45		%
Saturated power @ 1100 MHz	P_{SAT}	V_{CC} = 3.5 V, V_{REF} = 3.5 V, V_{APC}1, 2 = 2.7 V		30		dBm
Power added efficiency @ 1100 MHz	PAE	PSAT		40		%

Typical Performance Characteristics, Large Signal, 800 to 1100 MHz

V_{CC} = 2.5 V, 3.5 V, and 5.0 V, V_{APC} 1, 2 = 2.6 V, 2.7 V, and 2.8 V, T_A = –40 to +85 °C, characteristic impedance (Zo) = 50 Ω, unless otherwise noted

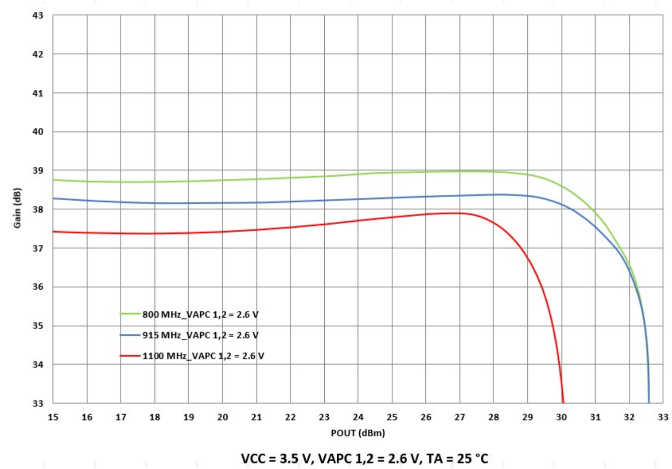


Figure 3. Gain (dB) vs. POUT (dBm) and Freq. (MHz)

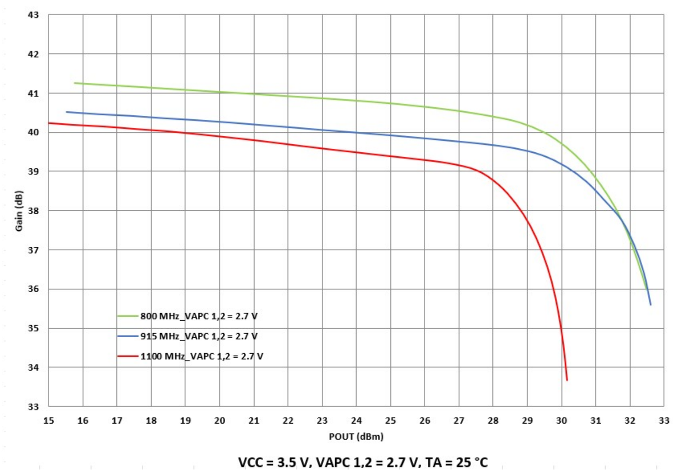


Figure 4. Gain (dB) vs. POUT (dBm) and Freq. (MHz)

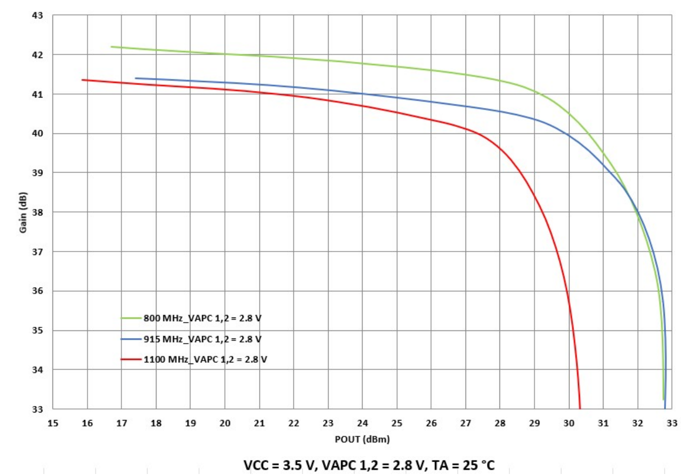


Figure 5. Gain (dB) vs. POUT (dBm) and Freq. (MHz)

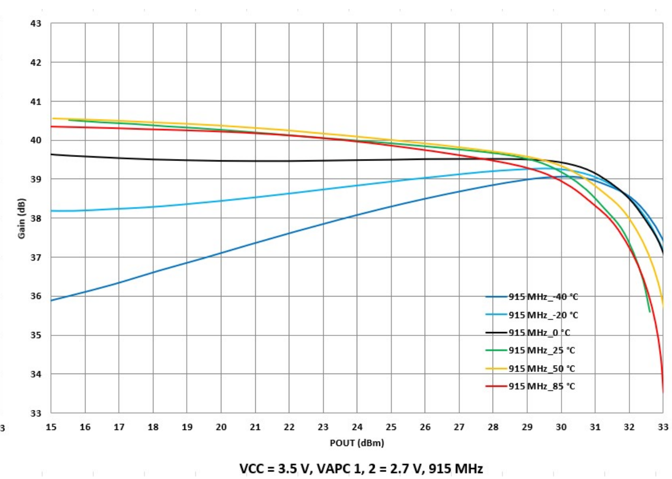


Figure 6. Gain (dB) vs. POUT (dBm) and Temp. (° C)

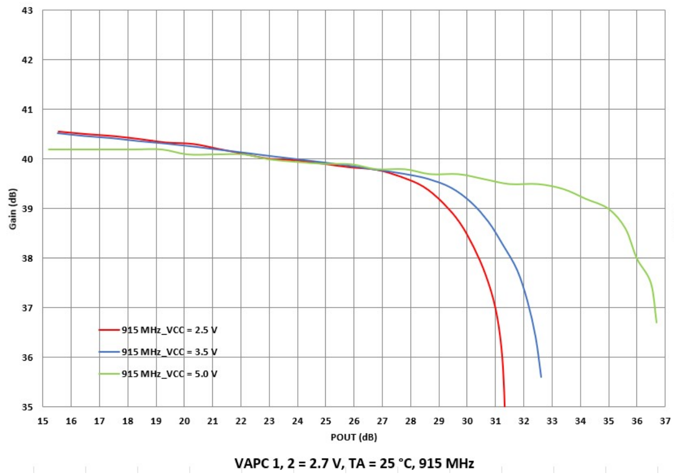


Figure 7. Gain (dB) vs. POUT (dBm) and VCC (V)

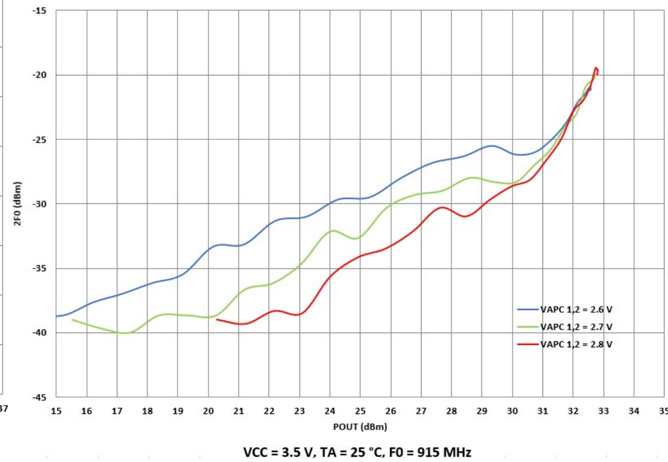


Figure 8. Second Harmonic 2F0 (dBm) vs. POUT (dBm) and VAPC 1, 2 (V)

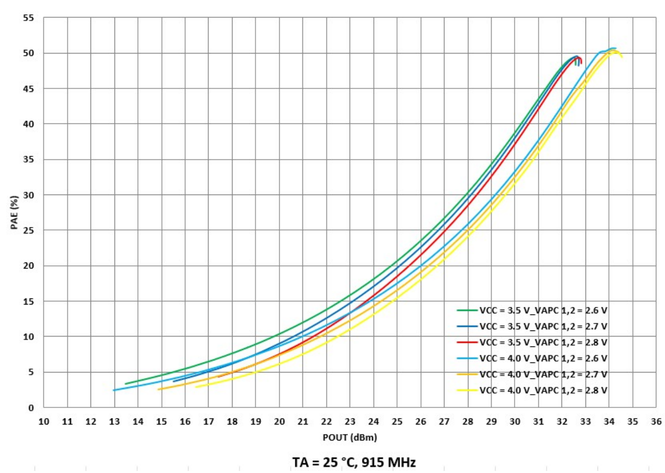


Figure 9. PAE (%) vs. POUT (dBm), VCC (V) and VAPC 1, 2 (V)

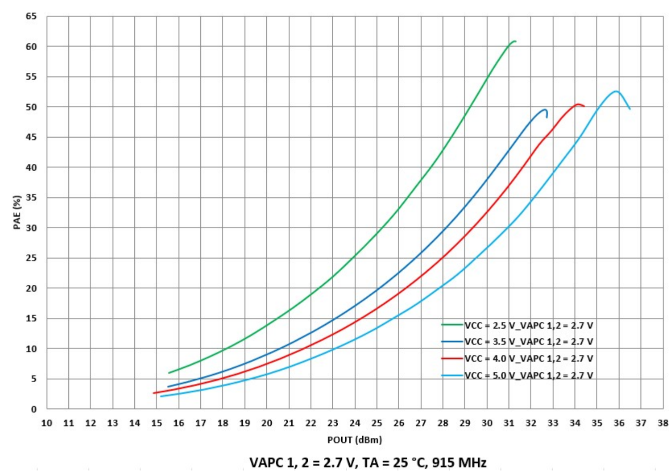


Figure 10. PAE (%) vs. POUT (dBm) and VCC (V)

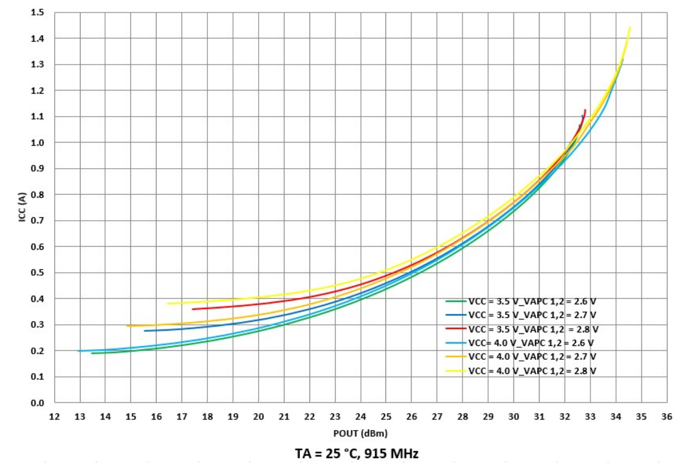


Figure 11. ICC (A) vs. POUT (dBm), VCC (V) and VAPC 1, 2 (V)

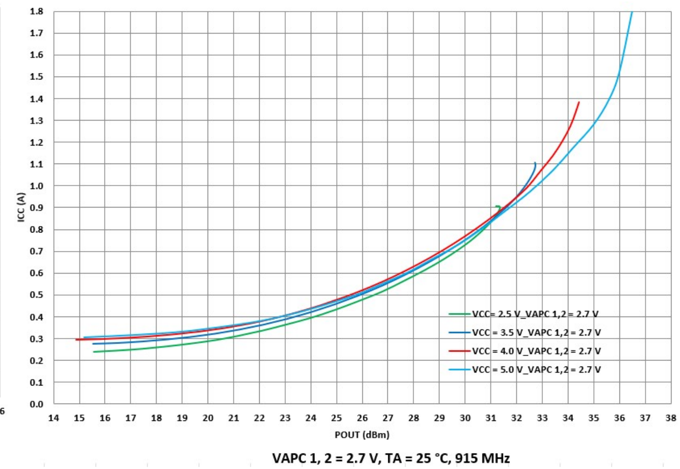


Figure 12. ICC (A) vs. POUT (dBm) and VCC (V)

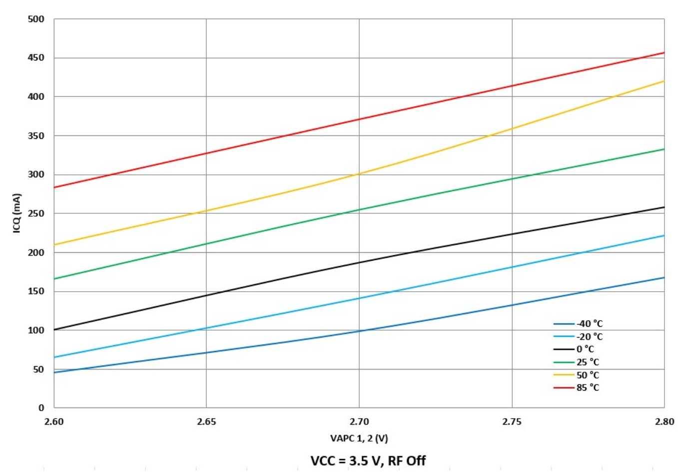


Figure 13. ICQ (mA) vs. VAPC 1, 2 (V) and Temp. (° C)

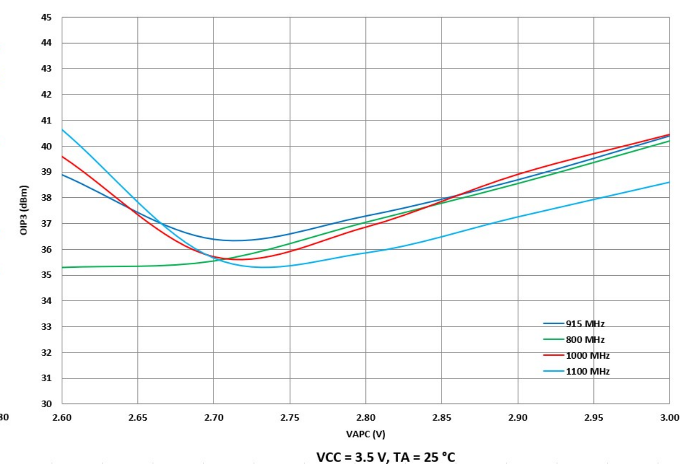


Figure 14. OIP3 (dBm) vs. VAPC 1, 2 (V) and Freq. (MHz)

Typical Performance Characteristics, Small Signal, 800 to 1100 MHz

V_{CC}=3.5 V, V_{APC} 1, 2 = 2.7V, T_A = –40 to +85 °C, P_{IN} = –30 dBm, characteristic impedance (Zo) = 50 Ω, unless otherwise noted

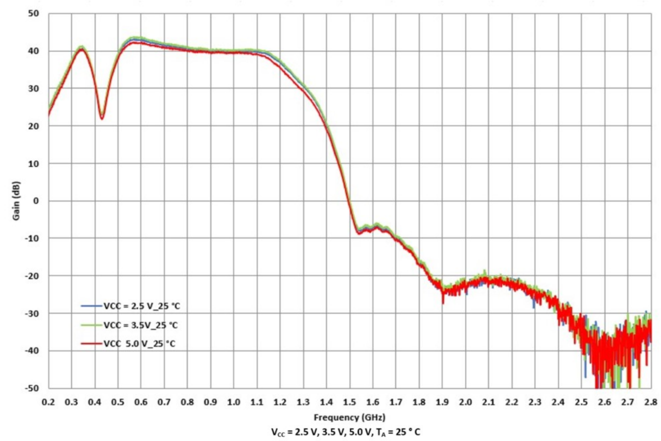


Figure 15. Gain (dB) vs. Freq. (MHz) and VCC (V)

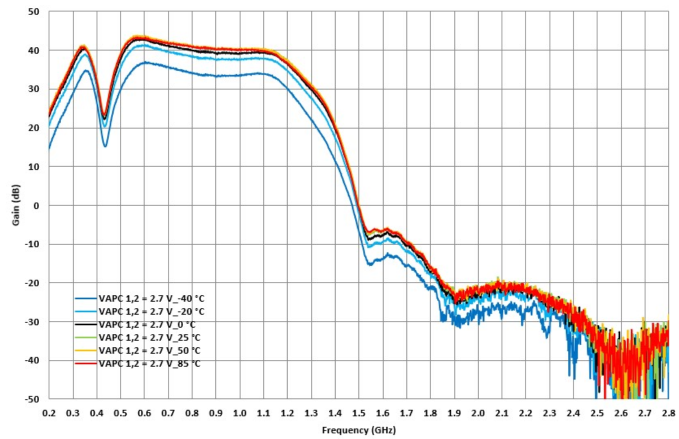


Figure 16. Gain (dB) vs. Freq. (MHz) and Temp. (° C)

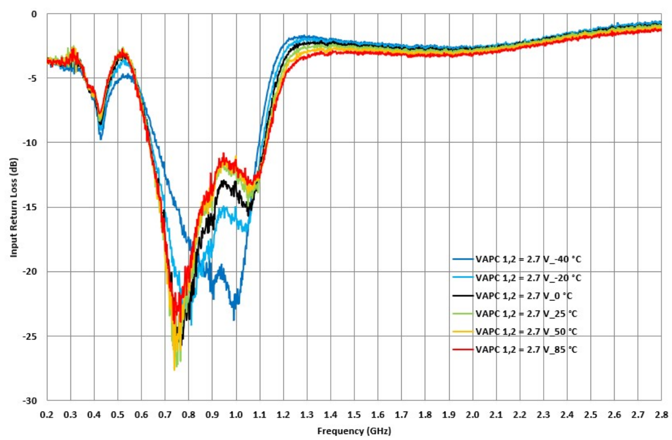


Figure 17. Input Return Loss (dB) vs. Freq. (MHz) and Temp. (° C)

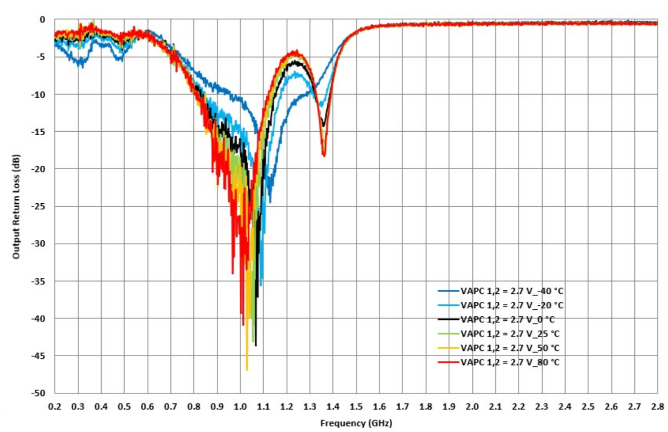


Figure 18. Output Return Loss (dB) vs. Freq. (MHz) and Temp. (° C)

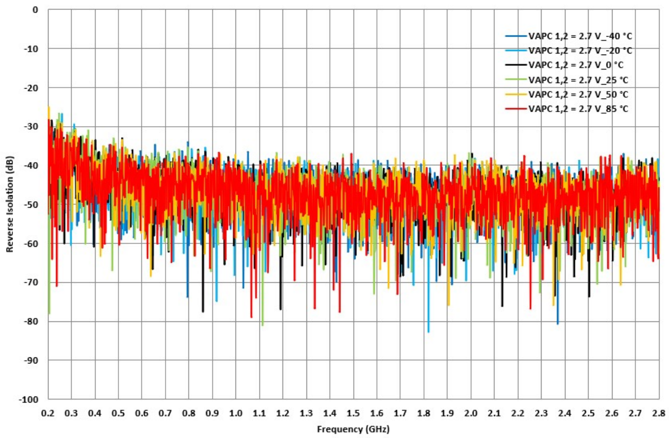


Figure 19. Reverse Isolation (dB) vs. Freq. (MHz) and Temp. (° C)

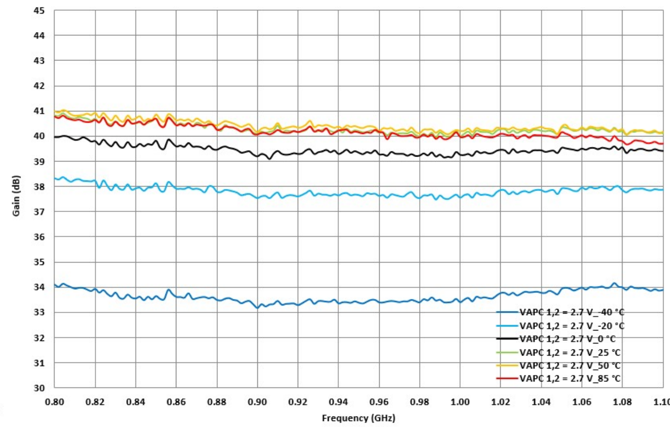


Figure 20. Gain (dB) vs. Freq. (MHz) and Temp. (° C)

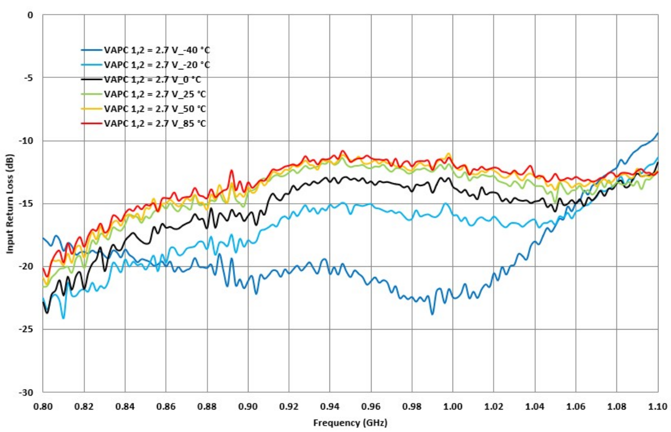


Figure 21. Input Return Loss (dB) vs. Freq. (MHz) and Temp. (° C)

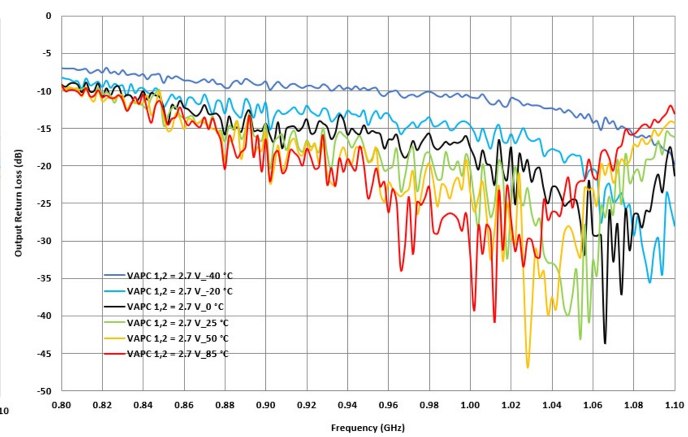


Figure 22. Output Return Loss (dB) vs. Freq. (MHz) and Temp. (° C)

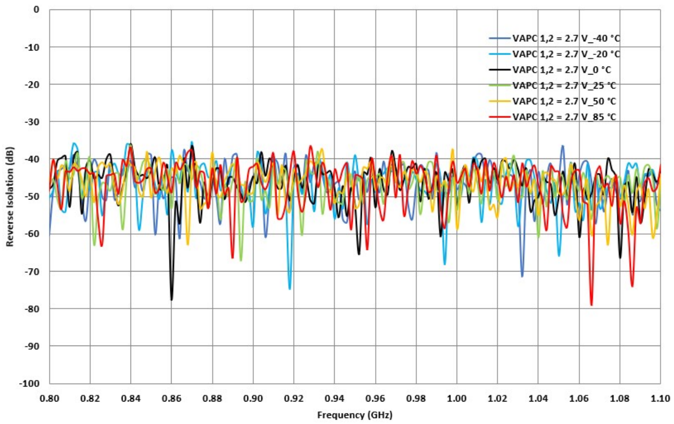


Figure 23. Reverse Isolation (dB) vs. Freq. (MHz) and Temp. (° C)

Typical Performance Characteristics, CDMA IS-95A ACPR Performance

V_{CC} = 2.5 V to 5.0 V, VAPC 1, 2 = 2.7V, T_A = +25 °C, characteristic impedance (Zo) = 50 Ω, unless otherwise noted

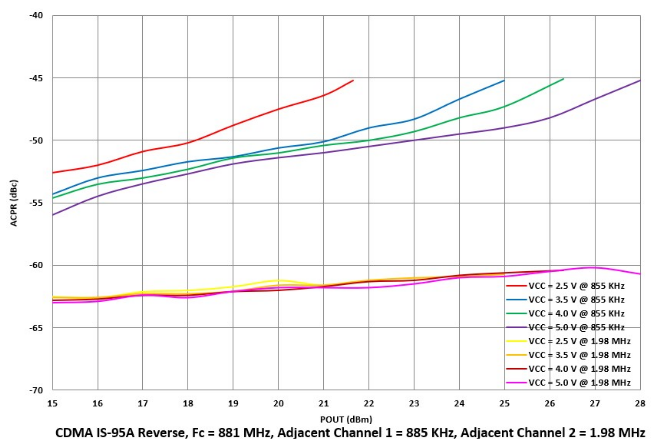


Figure 24. ACPR (dBc) versus POUT (dBm) and VCC (V)

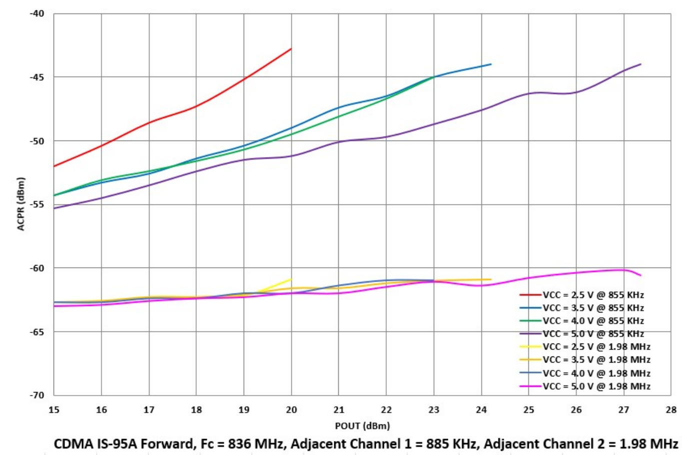


Figure 25. ACPR (dBc) versus POUT (dBm) and VCC (V)

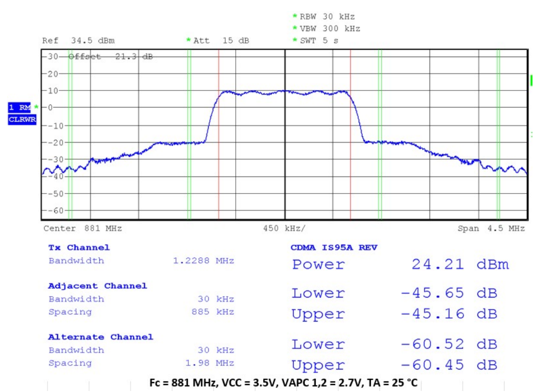


Figure 26. ACPR, CDMA IS-95A Reverse

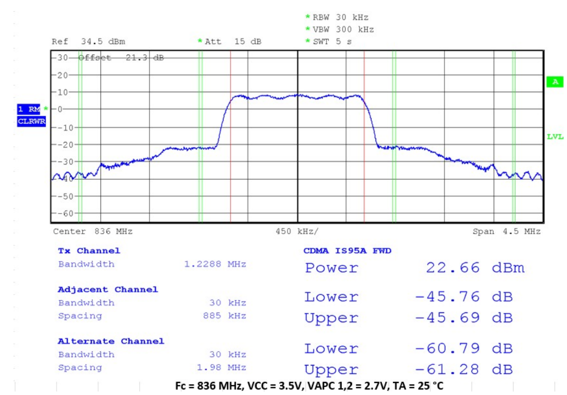


Figure 27. ACPR, CDMA IS-95A Forward

Typical Performance Characteristics, Response Time

V_{CC} = 3.5 V, V_{APC} 1, 2 = 2.7 V/0 V, T_A = +25 °C, PIN = –15 dBm, 915 MHz, unless otherwise noted

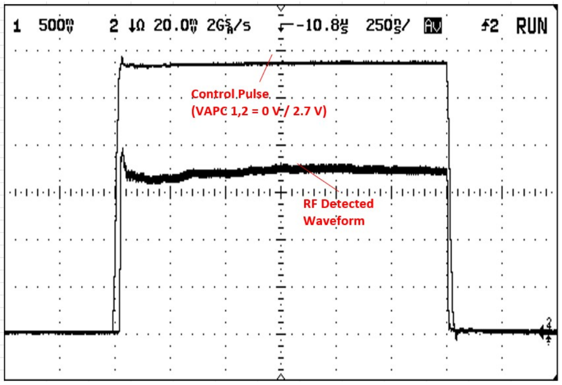


Figure 28. Rise and Fall Response Time

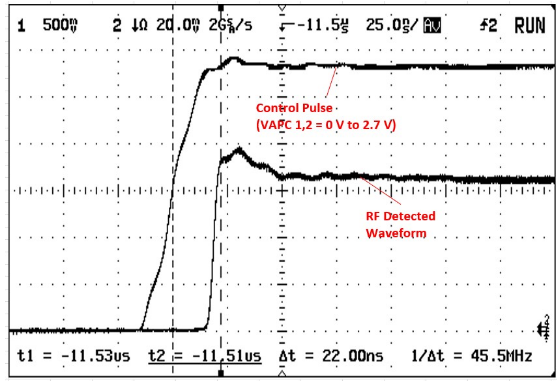


Figure 29. Rise Response Time (50% Ctrl, 90% RF)

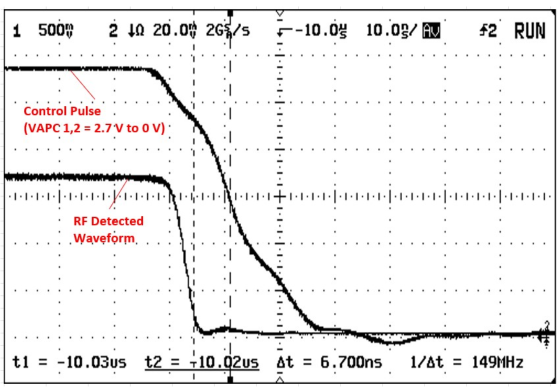


Figure 30. Fall Response Time (50% Ctrl, 10% RF)

Application Circuit

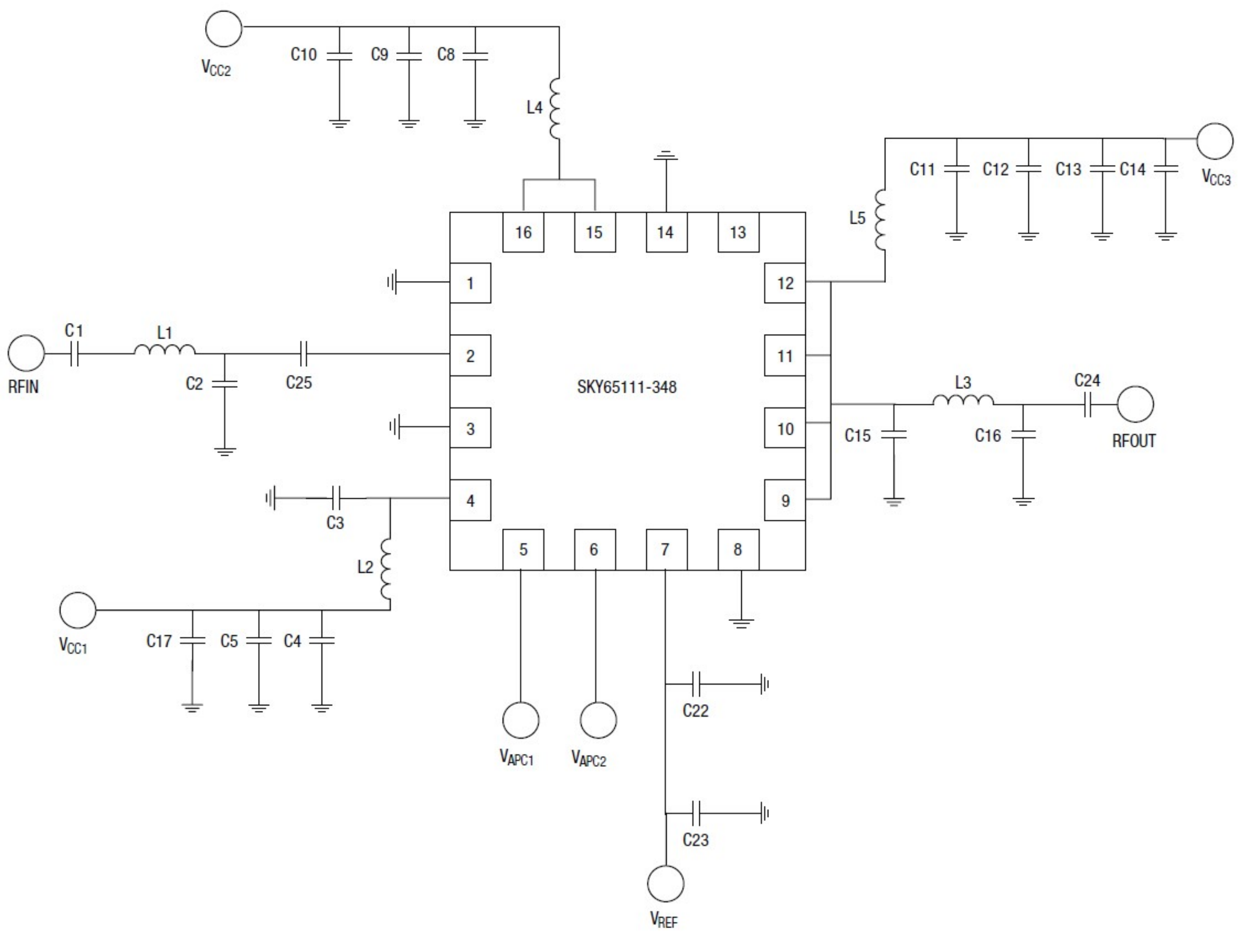


Figure 31. Application Circuit

BOM for Application Circuit

Table 7. Recommended Evaluation Board Component Values

Component	Value	Size	Manufacturer	Part Number
C1	100 pF	0402	Murata	GRM1555C1H101JA01
C2	0.5 pF	0402	Murata	GRM1555C1H0R5JZ35E
C3	4.7 pF	0402	Murata	GRM1555C1H4R7JZ35E
C4	100 pF	0402	Murata	GRM1555C1H101JA01
C5	1000 pF	0402	Murata	GRM155R71H102KA01
C8	100 pF	0402	Murata	GRM1555C1H101JA01
C9	1000 pF	0402	Murata	GRM155R71H102KA01
C10	10 µF	0402	AVX	TAJA106M006R
C11	100 pF	0402	Murata	GRM1555C1H101JA01
C12	1000 pF	0402	Murata	GRM155R71H102KA01
C13	10 nF	0402	Murata	GRM155R71E103KA01
C14	10 µF	1206	AVX	TAJA106M006R
C15	15 pF	0402	Murata	GJM1555C1H150JB01E
C16	6.8 pF	0402	Murata	GJM1555C1H6R8CB01E
C17	10 µF	1206	AVX	TAJA106M006R
C22	1000 pF	0402	Murata	GRM155R71H102KA01
C23	100 pF	0402	Murata	GRM1555C1H101JA01
C24	100 pF	0402	Murata	GRM1555C1H101JA01
C25	27 pF	0402	Murata	GRM1555C270JZ35E
L1	1 nH	0402	Taiyo Yuden	HK1005-1N0S
L2	1.2 nH	0402	Taiyo Yuden	HK1005-1N2S
L3	1.8 nH	0402	Taiyo Yuden	HK1005-1N8S
L4	1 nH	0402	Taiyo Yuden	HK1005-1N0S
L5	10 nH	0603	Coilcraft	0603HC-10NXJB

Component Placement Diagram

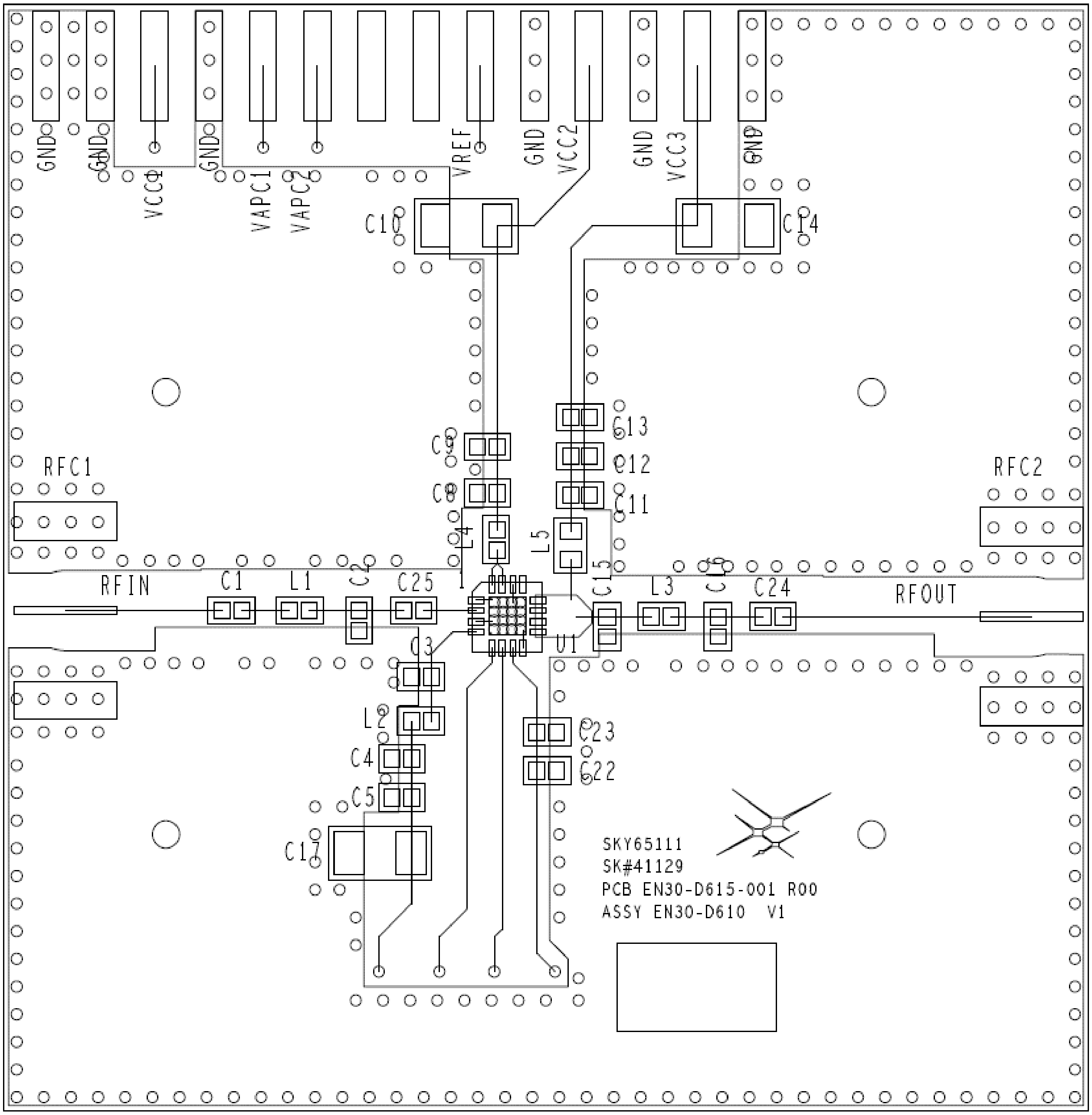


Figure 32. Component Placement Diagram

Application Circuit Notes

Ground (Pins 1, 3, 8, 14). Attach all ground pins to the RF ground plane with the largest diameter and lowest inductance via that the layout will allow. Multiple small vias are also acceptable and will work well under the device if solder migration is an issue. It is extremely important that the device paddle be sufficiently grounded for both thermal and stability reasons. See the enclosed package footprint.

RF input (Pin 2). A lumped element matching structure for good in-band return loss has been realized on the RF input, Pin 2. This structure is comprised of a dc blocking capacitor (C1), low pass LC filter (L1, C2) and at the device input, a series capacitor (C25). This combination of devices yields a return loss better than –11 dB over the entire 600 to 1100 MHz band of interest. The placement of C1 is not critical; it can be moved as close to L1, C2, and C25 as desired. C25 should be placed as close to the device pin as possible to replicate performance as measured on the applications board.

VCC1 (Pin 4). VCC1 is the collector bias for the first amplifier stage in the SKY65111-348LF. Multiple bypass capacitors, C3 to C5, C17, and a series inductor, L2, have been utilized to ensure stability both in and out of the useable bandwidth of the device. The length of transmission line between L2 and Pin 4 is not critical; L2 can be placed as close to the pin as possible if desired. However, placement of L2 farther away from Pin 4 than shown on the applications circuit is not recommended. C3 should also be placed in the approximate location shown on the applications circuit, but placement is not critical.

VAPC1 (Pin 5). VAPC1 is the bias control voltage input for amplifier stages 1 and 2. Nominal operating range is between 2.5 V dc and 2.8 V dc. VAPC1 may also be set to 0 V dc, to force stages 1 and 2 into standby mode.

VAPC2 (Pin 6). VAPC2 is the bias control voltage for amplifier stage 3. Nominal operating range is between 2.5 V dc and 2.8 V dc. VAPC2 can also be set to 0 V, if the intent is to place amplifier stage 3 into standby mode to reduce current consumption.

Note: *In most applications, VAPC1 and VAPC2 pins are directly tied together and biased from the same control voltage. VAPC1 and VAPC2 may also be split if independent control is desired.*

VREF (Pin 7). VREF is the bias reference voltage for amplifier stages 2 and 3. VREF should be operated over the same voltage range as VCC, with a nominal voltage of 3.5 V dc. Bypassing of VREF is accomplished with C22 and C23 which should be placed as close to the device pin as possible.

RFOUT, VCC3 (Pins 9 to 12). RFOUT and VCC3 are the inputs for the power supply connection to the stage 3 collectors, as well as the RF output port. These pins should be tied together to enable current sharing. Bias is applied to the RF output through L5, a high current-rated 10 nH inductor. Capacitors C11 through C14 provide proper RF bypassing, and should be placed closely to L5, as shown in the applications circuit. Output matching for optimal power gain is accomplished using capacitors C15, L3, and C16. C15 should be placed approximately 141 mils (3.6 mm) from the RF output.

Pin 13. Pin 13 has no connection and should be left open in the circuit.

VCC2 (Pins 15 and 16). VCC2 is the collector bias input for the second amplifier stage in the device. Multiple bypass capacitors, C8 to C10, have been used to ensure stability, both in and out of the usable bandwidth of the device. C8 should be placed close to L4, as shown in the application board layout.

Application Board Biasing Procedure

1. Connect dc ground.
2. Connect all VCC and VREF lines to 3.5 V supply.
3. With the RF off, apply 2.7 V dc to VAPC 1, 2 control pins. Verify the ICQ current is approximately 250 mA.
4. Apply RF signal data –30 dBm level and observe that the output level is approximately 10 dBm or the gain of the device is approximately 40 dB.

Note: *It is important that VCC1, VCC2, VCC3, and VREF voltage source be adjusted such that 3.5 V is measured at the board. The high collector currents will drop collector voltage significantly if long leads are used. Adjust bias voltage to compensate.*

Recommended Solder Reflow Profiles

For information on recommended solder reflow processes, see the Skyworks application note.

Package and Handling Information

Instructions on the shipping container label regarding exposure to moisture after the container seal is broken must be followed. Otherwise, problems related to moisture absorption may occur when the part is subjected to high temperature during solder assembly.

The SKY65111-348LF is rated to Moisture Sensitivity Level 1 (MSL1) at 260 °C. It can be used for lead or lead-free soldering. For additional information, refer to the Skyworks Application Note, "PCB Design & SMT Assembly/ Rework Guidelines for MCM-L Packages," document number 101752.

Care must be taken when attaching this product, whether it is done manually or in a production solder reflow environment. Production quantities of this product are shipped in a standard tape and reel format.

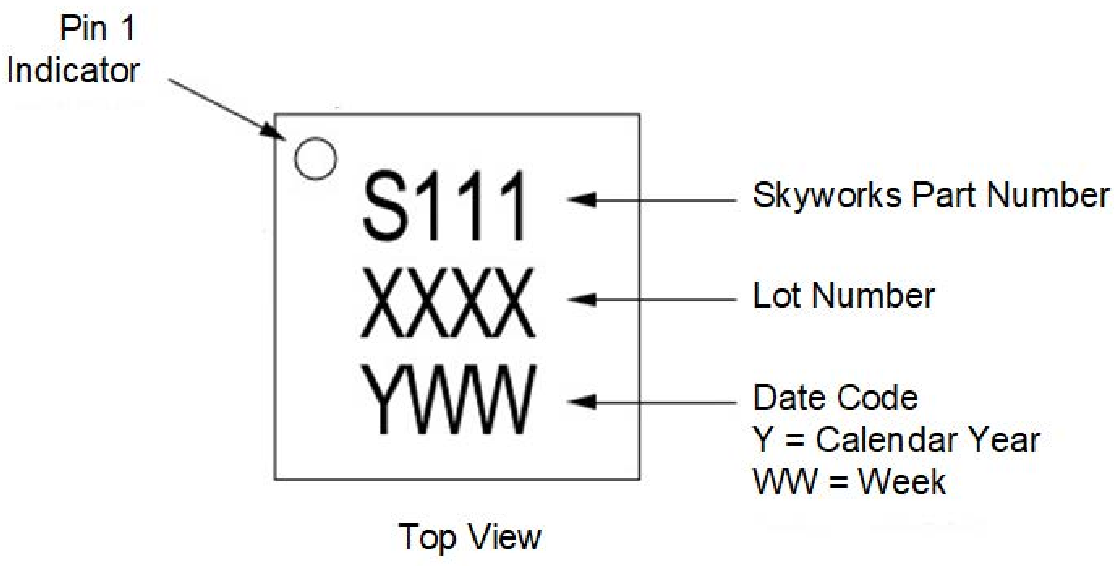
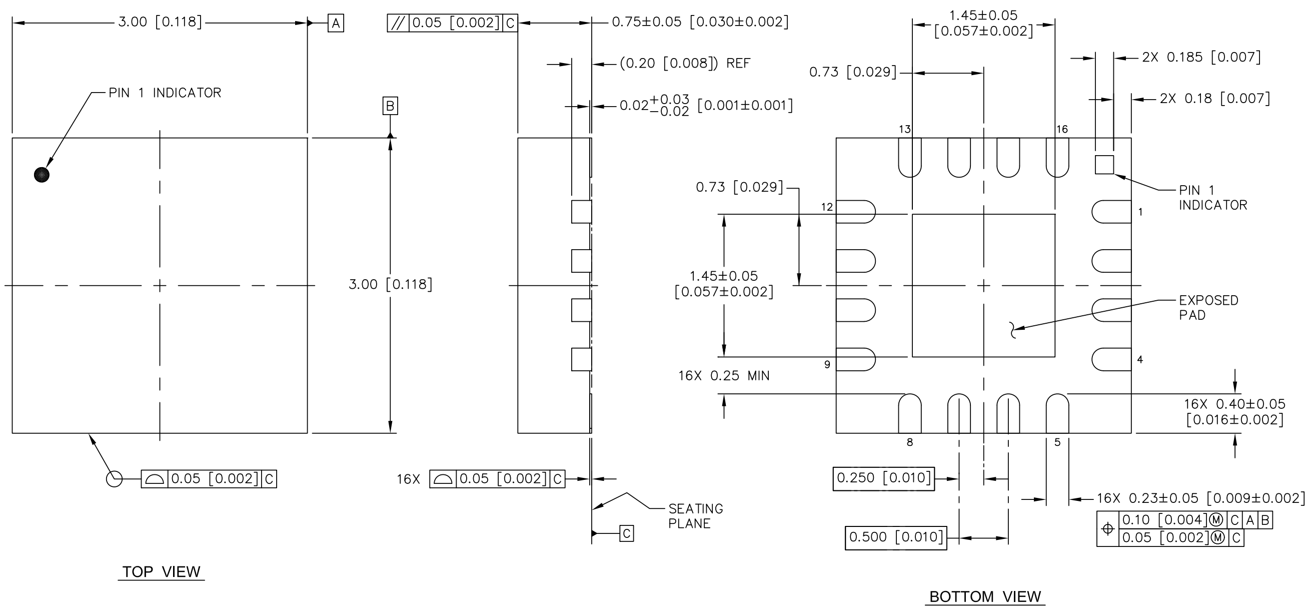


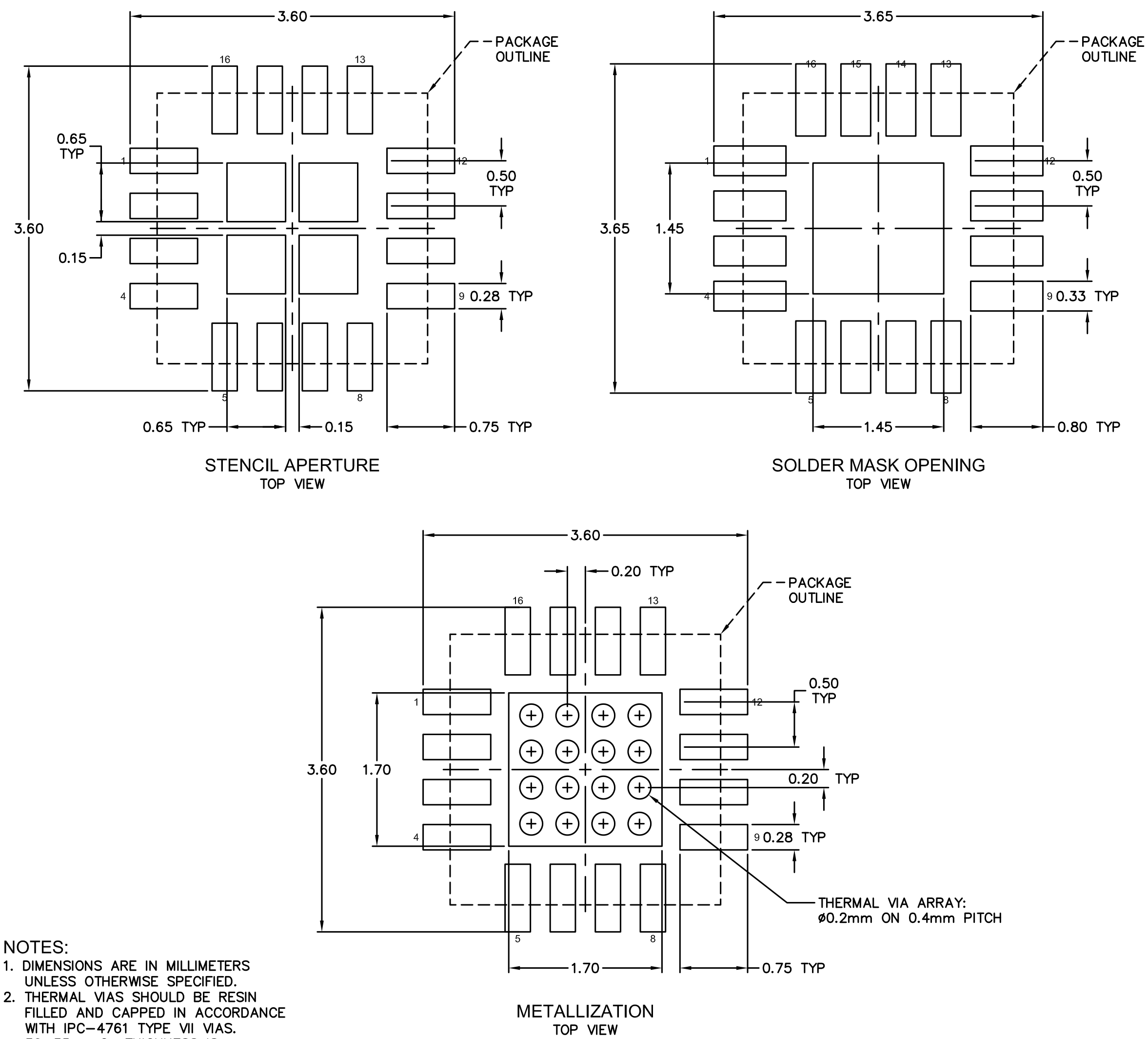
Figure 33. Typical Part Marking



NOTES:
1. DIMENSIONING AND TOLERANCING PER ASME Y14.5M – 1994.
2. DIMENSIONS ARE IN MILLIMETERS AND [INCHES]. CONTROLLING DIMENSION IN MILLIMETERS.
3. COPLANARITY APPLIES TO EXPOSED HEAT SINK SLUG AS WELL AS THE TERMINALS.
4. −348 PACKAGE TYPE.
5. PLATING REQUIREMENTS PER SOURCE CONTROL DRAWING: SQ03–0462.

TOLERANCING UNLESS OTHERWISE SPECIFIED
X.XXXX (4 PLC): ± 0.0005mm
X.XXX (3 PLC): ± 0.005mm
X.XX (2 PLC): ± 0.02mm
ANGULAR: ± 1/2°

Figure 34. Package Dimensions



NOTES:
1. DIMENSIONS ARE IN MILLIMETERS UNLESS OTHERWISE SPECIFIED.
2. THERMAL VIAS SHOULD BE RESIN FILLED AND CAPPED IN ACCORDANCE WITH IPC–4761 TYPE VII VIAS. 30–35um Cu THICKNESS IS RECOMMENDED.

Figure 35. PCB Layout Footprint

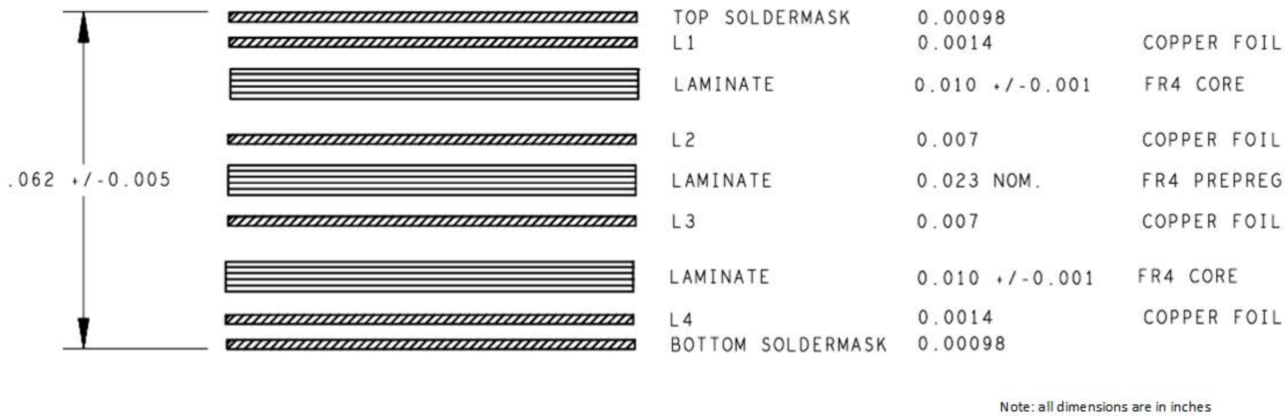


Figure 36. Evaluation Board Stack-Up

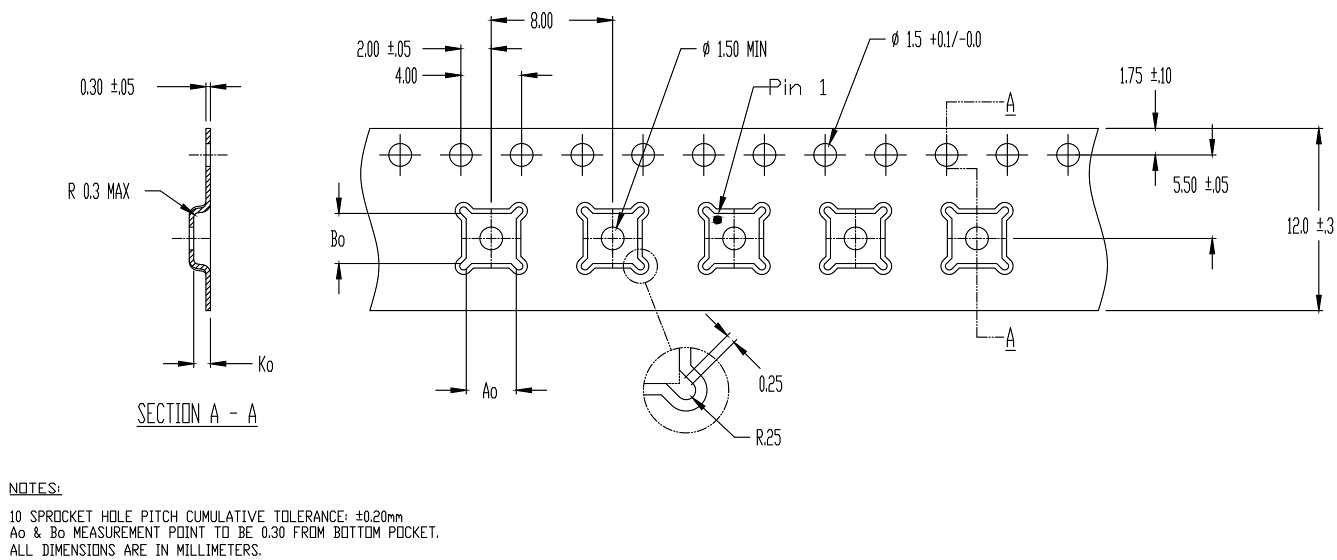


Figure 37. Tape and Reel Information

Ordering Information

Part Number	Description	Evaluation Board Part Number
SKY65111-348LF	600 to 1100 MHz ISM Band Two-Watt InGaP HBT Power Amplifier	SKY65111-348LFEK1