Mitigating False Turn-On in Power MOSFETs Using Current Mode Gate Drivers: Advancements in Gate Drive Control

Matthew Segada – Skyworks Solutions
Matthew.Segada@skyworksinc.com

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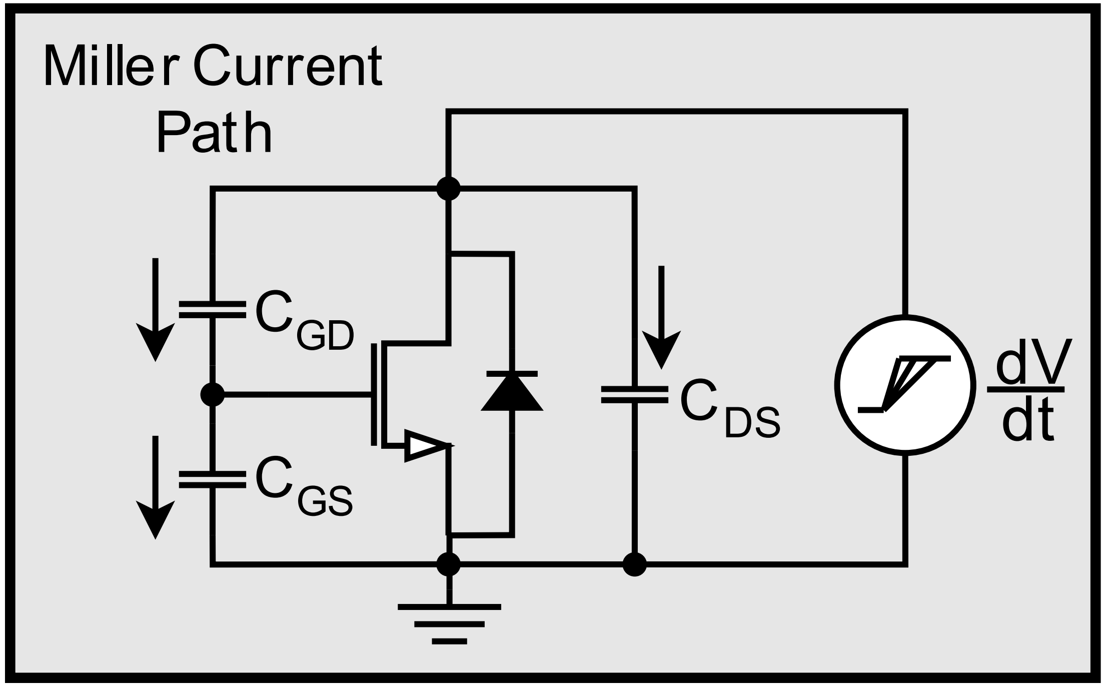
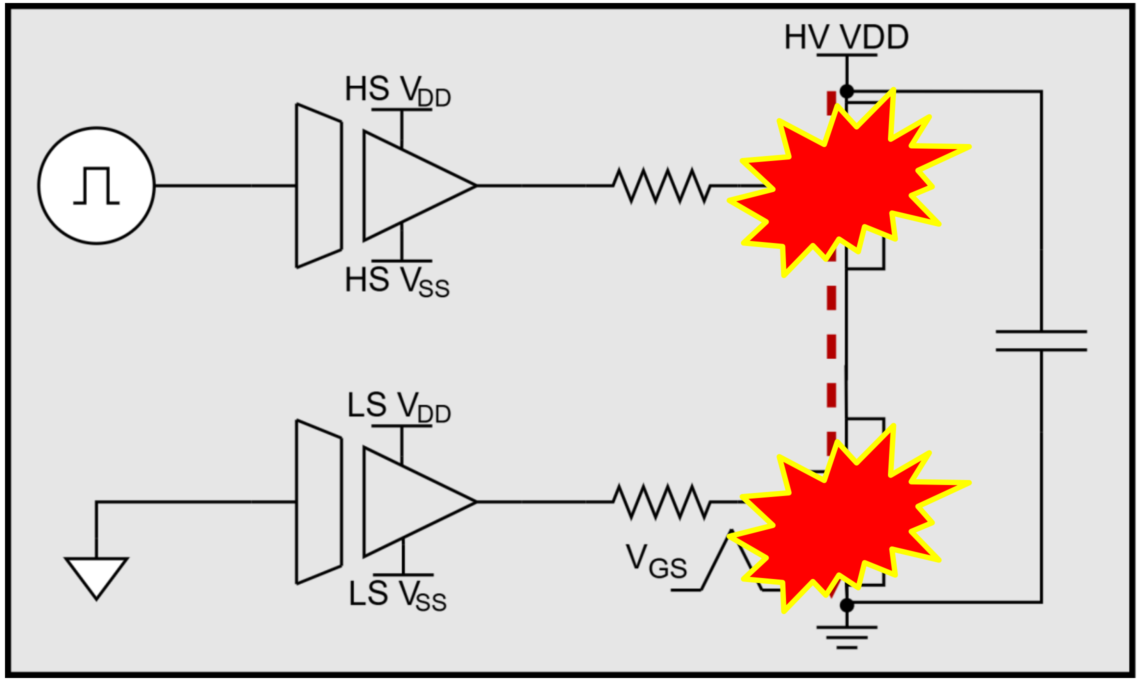
Miller Capacitance and Parasitic Turn-On



- Miller capacitance (C_{GD}) causes a current to flow through C_{GD} + C_{GS}
- Approximately: $dV_{GS} \approx \frac{C_{GD}}{C_{GS}} dV_{DS}$
  - See appendix for derivation
- Capacitance ratio of $\frac{C_{GD}}{C_{GS}}$ determines susceptibility of parasitic turn-on (PTO)
- If $V_{GS} > V_{GS(TH)}$ then PTO can occur

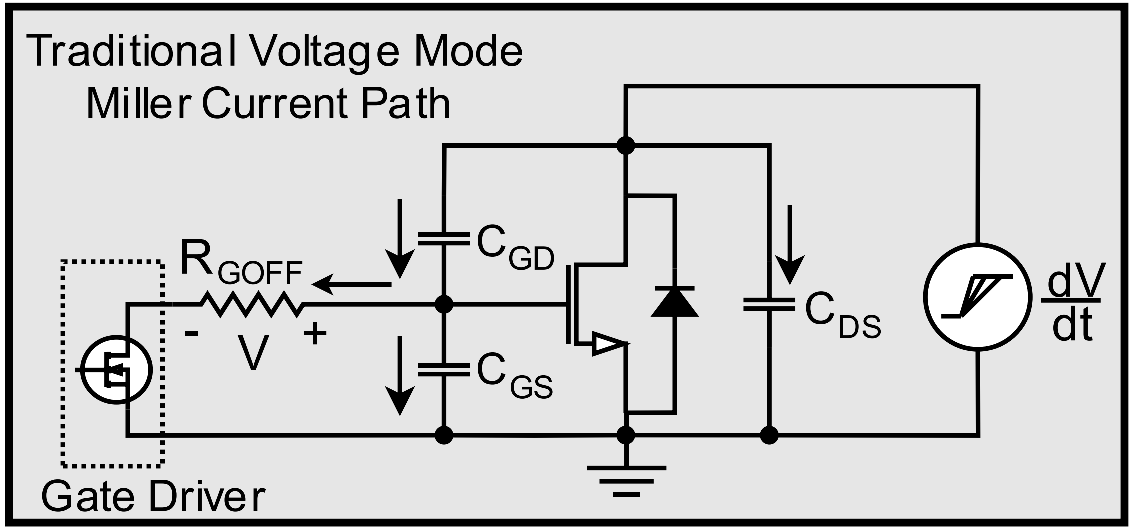
Parasitic Turn On



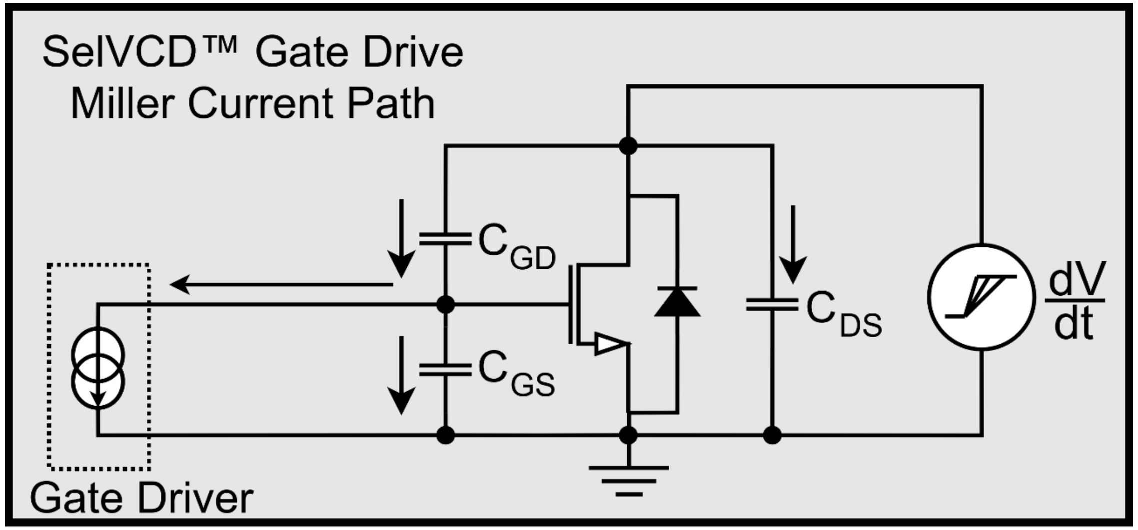
- PTO can cause fires
- Power supply design needs to consider all operating modes/conditions
- Power supply revisions are costly, especially if power supplies are already in the field

Miller Effect & Gate Drivers

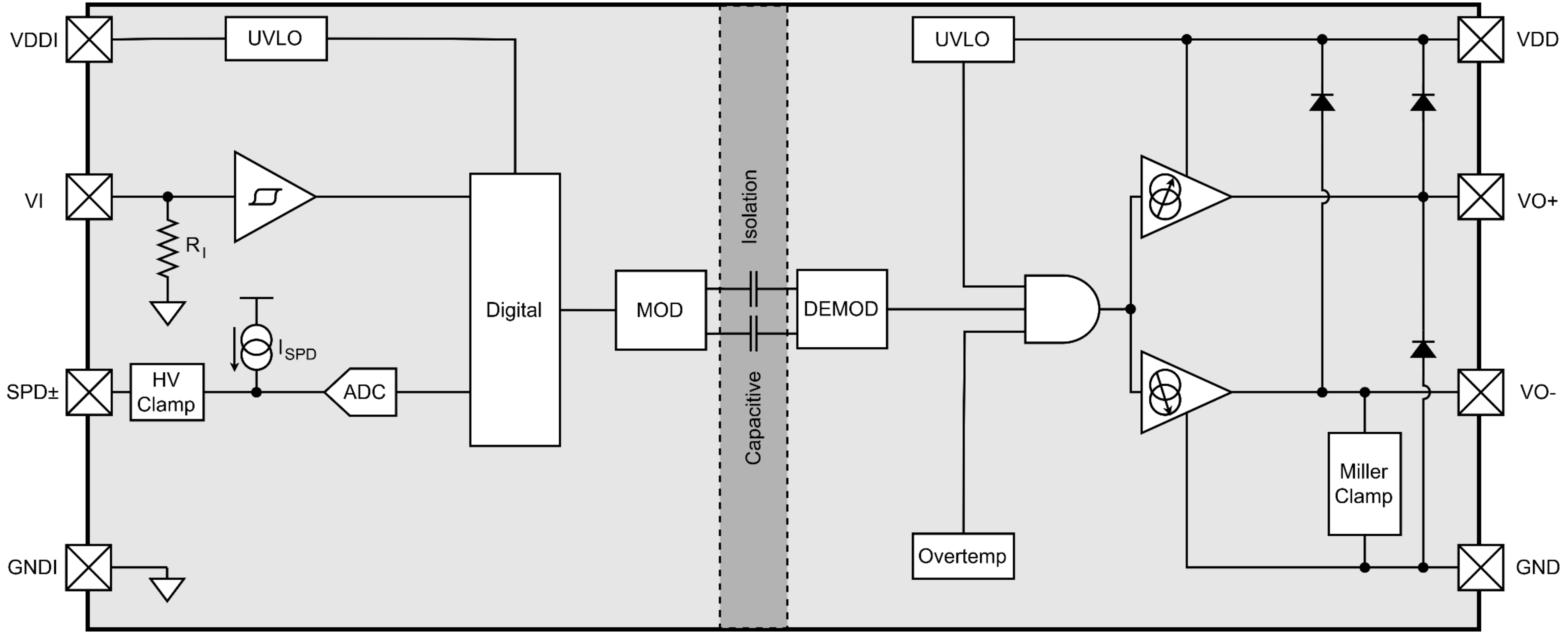
R_{GOFF} Impedes flow



Current source has direct path

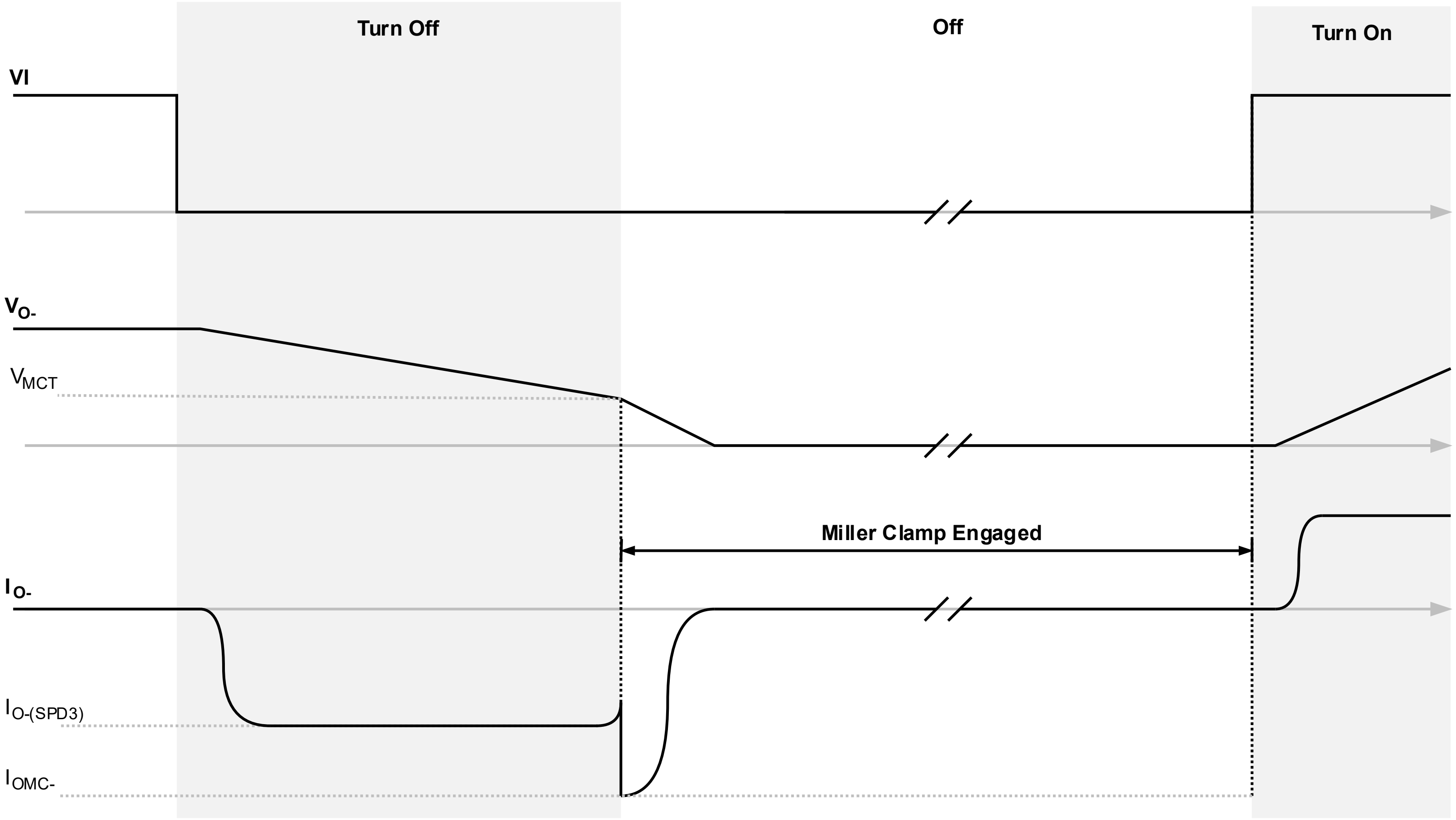


Inside a Current Mode Gate Driver



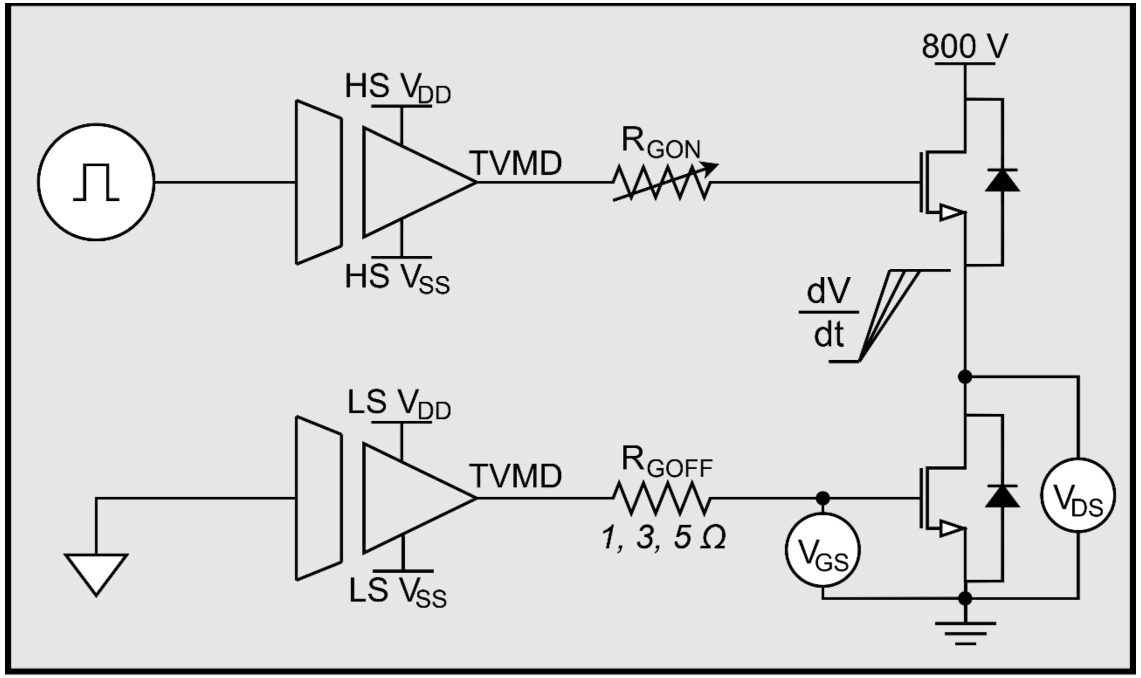
- SPD± pin controls output current for V_{OH} and V_{OL}
  - Analog voltage input or resistor
- Output die demodulates SPD± information over channel
- Output current sources change the source/sink current
- Miller clamp is setting the sinking current source to max current sink

Miller Clamp Engagement Waveform

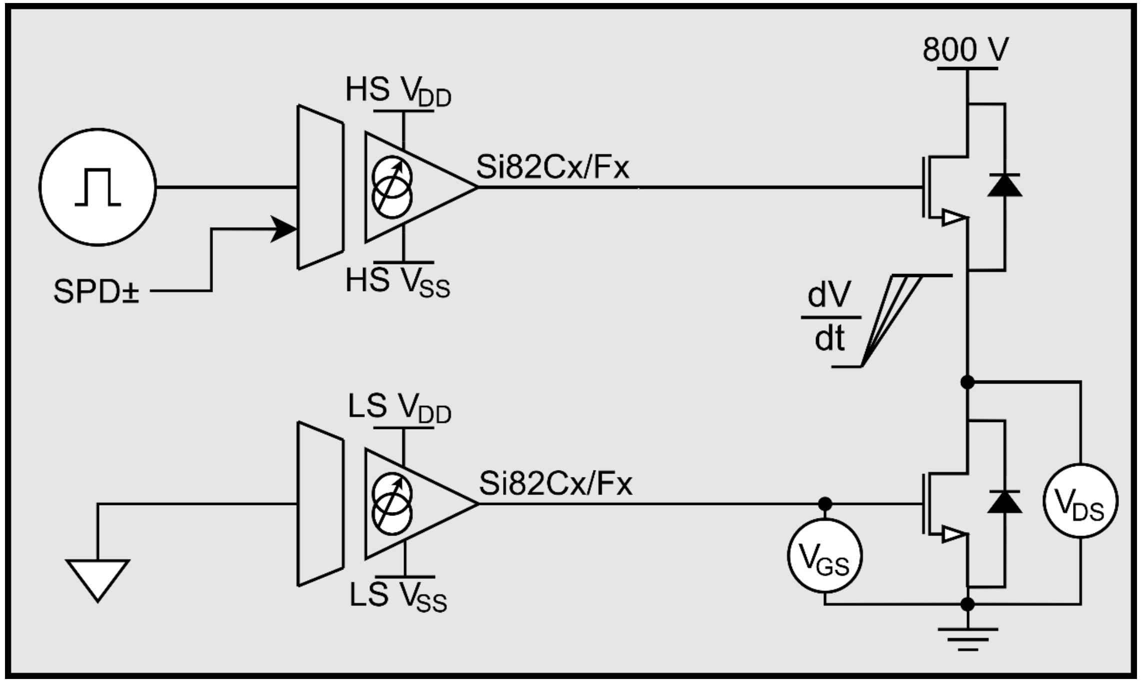


Test Setup – 1200V 16 mΩ SiCFET

Traditional Voltage Mode Driver
6 A – R_{ON-} = 0.7 Ω

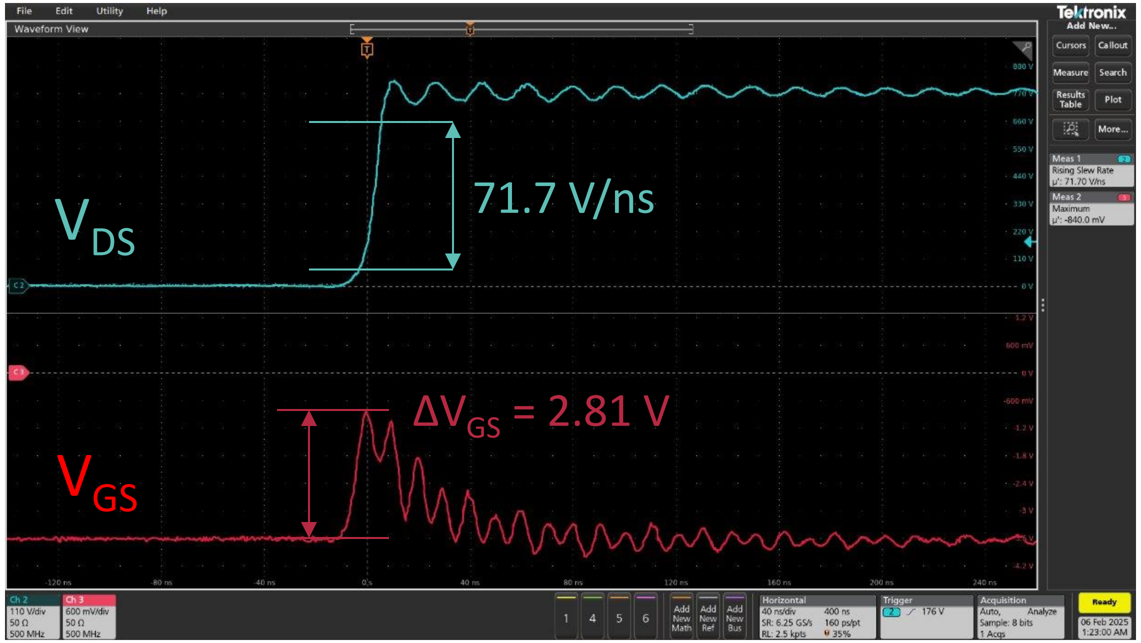


SelVCD™ Gate Driver
4 A

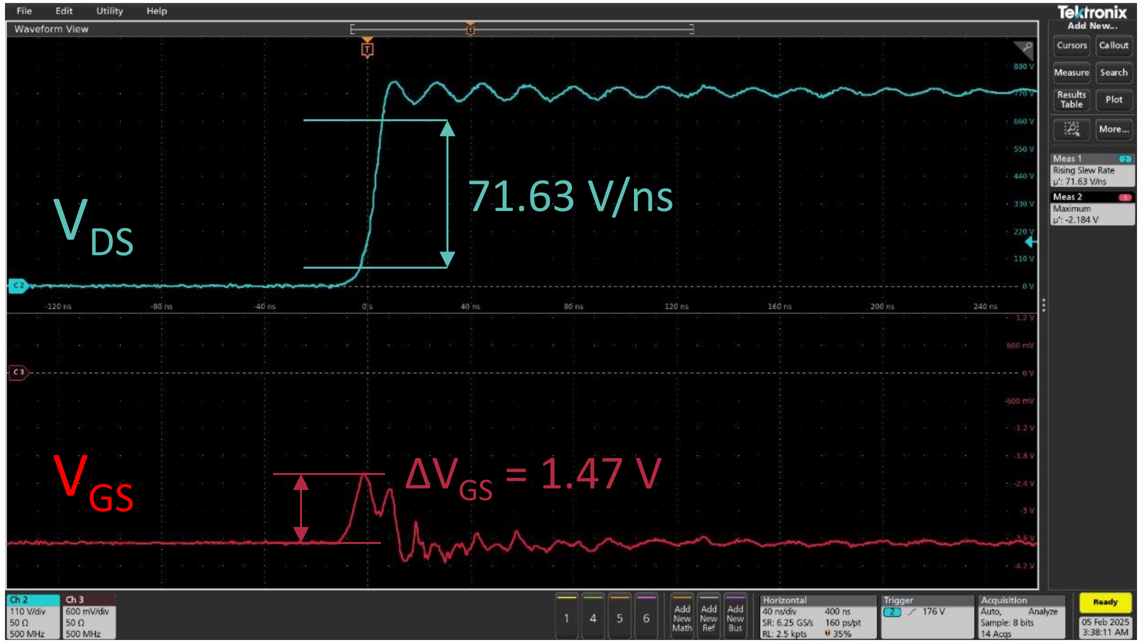


Low Side V_{DS} and V_{GS} Waveforms

TVMD R_{GOFF} = 3 Ω

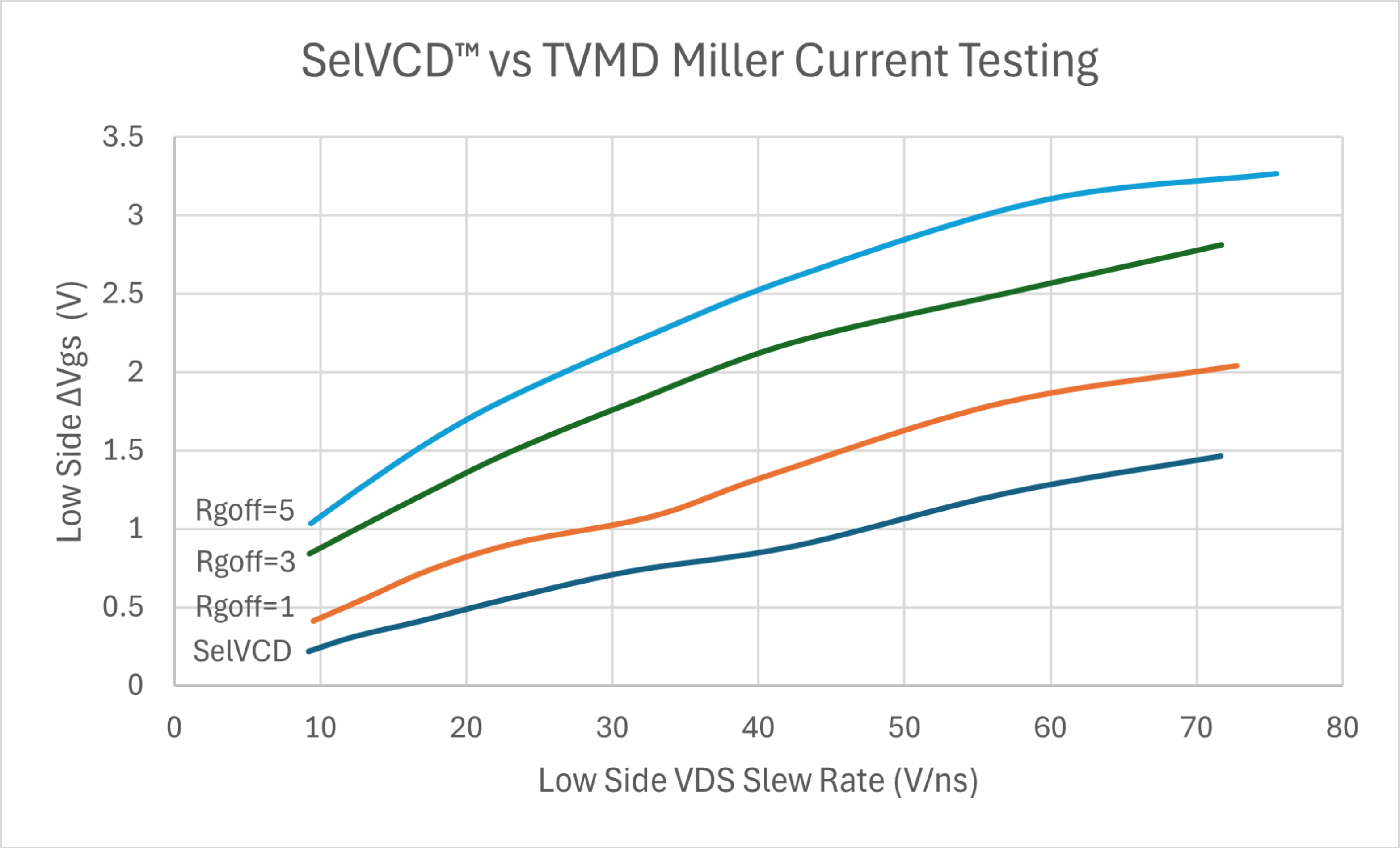


SeIVCD™



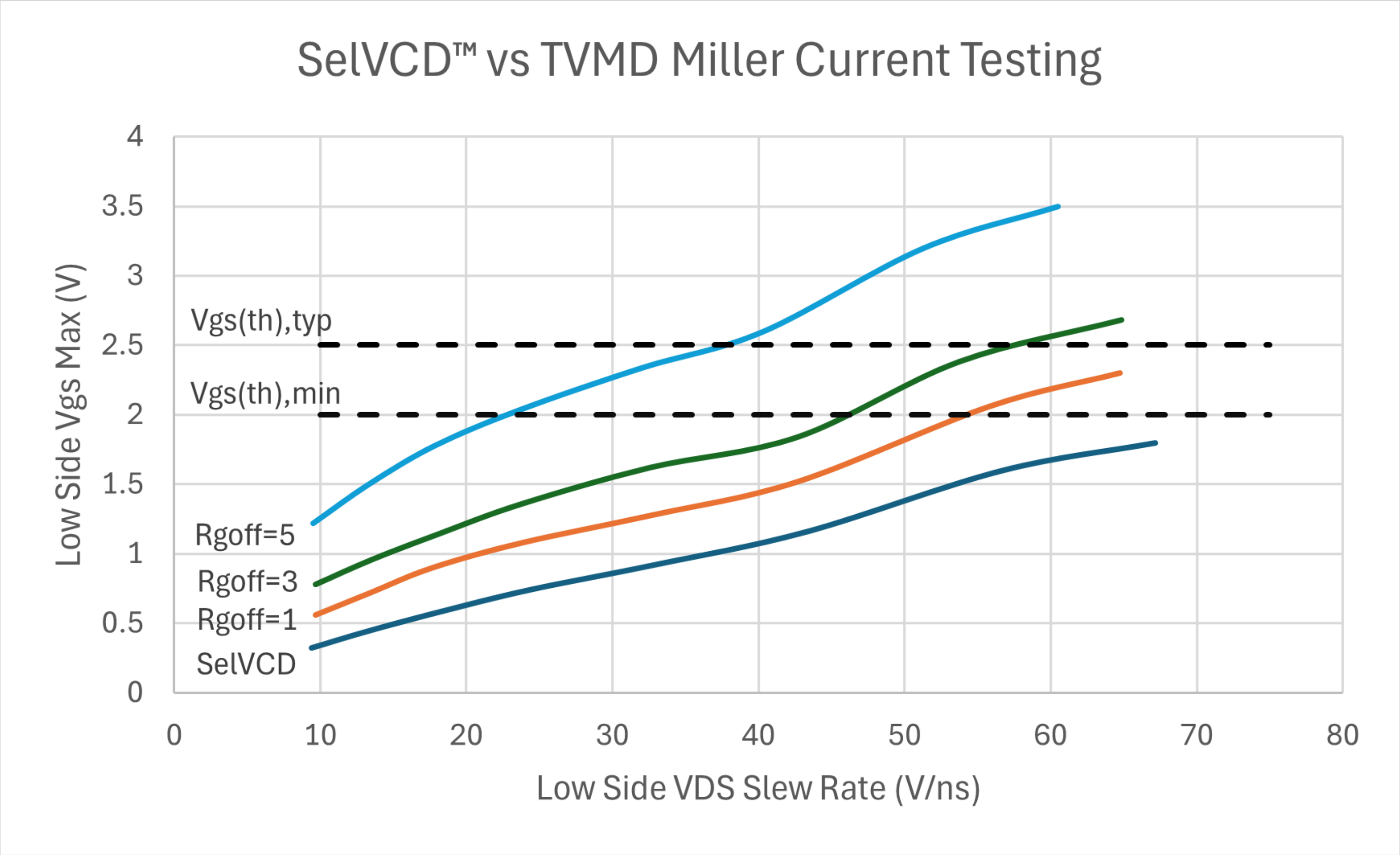
$V_{GS,ON}$ = 15 V, $V_{GS,OFF}$ = -3.5 V

ΔV_{GS} vs V_{DS} Slew Rate Results – Negative Bias



$V_{GS,ON}$ = 15 V, $V_{GS,OFF}$ = -3.5 V

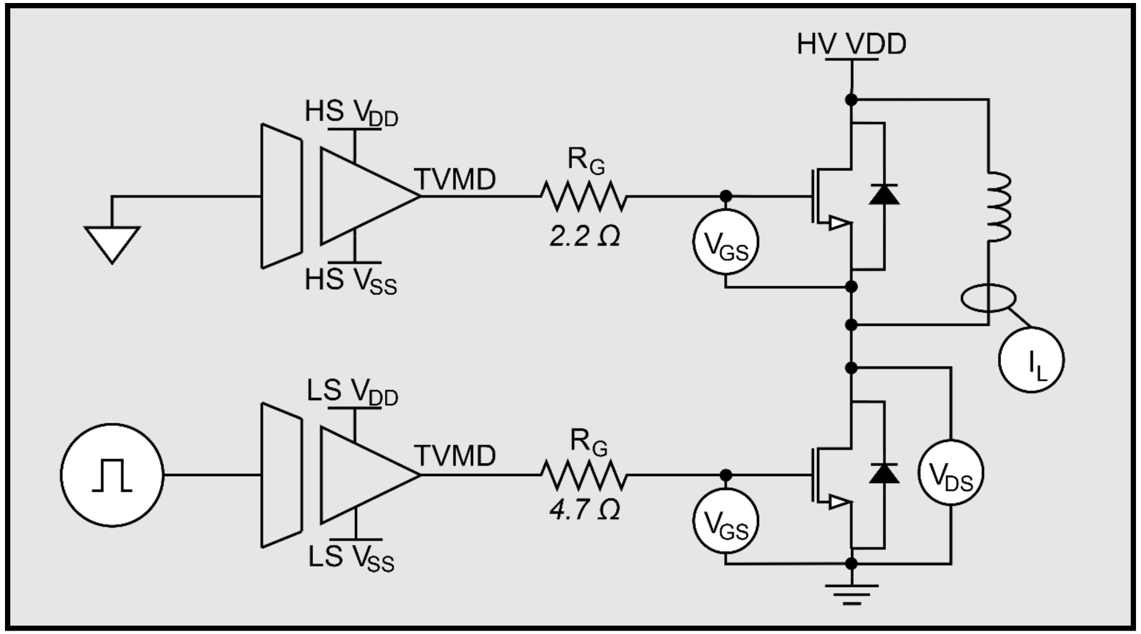
V_{GS} vs V_{DS} Slew Rate Results – 0 V Bias



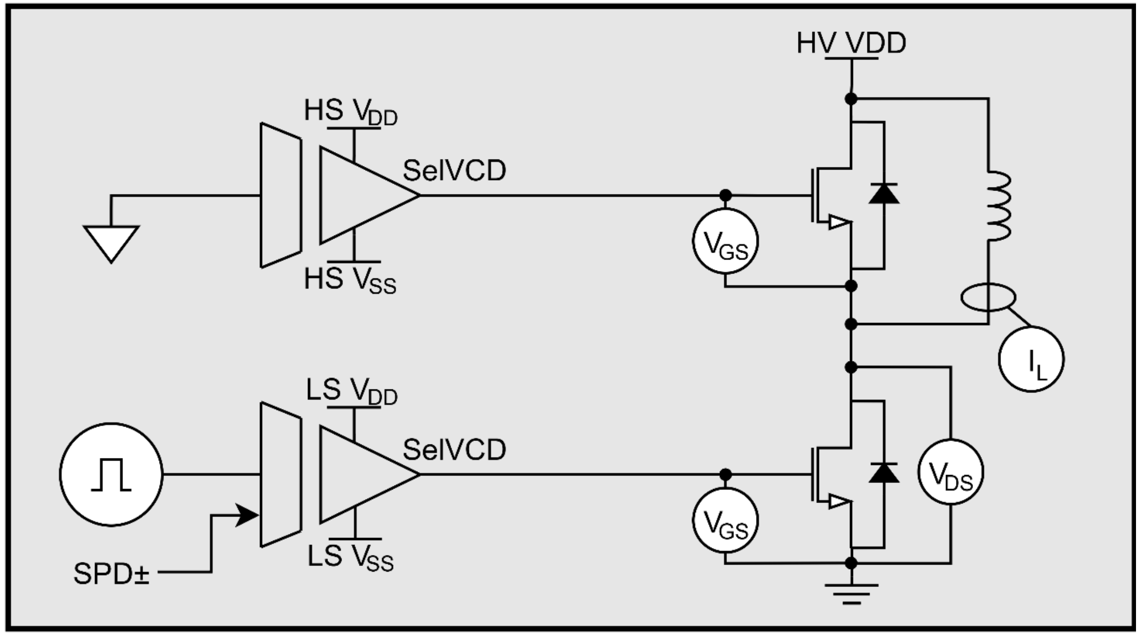
$V_{GS,ON}$ = 15 V, $V_{GS,OFF}$ = 0 V

750 V SiC - Customer Test Setup V_{GS} = +18.5/0 V

Si82E39ABE-IS3

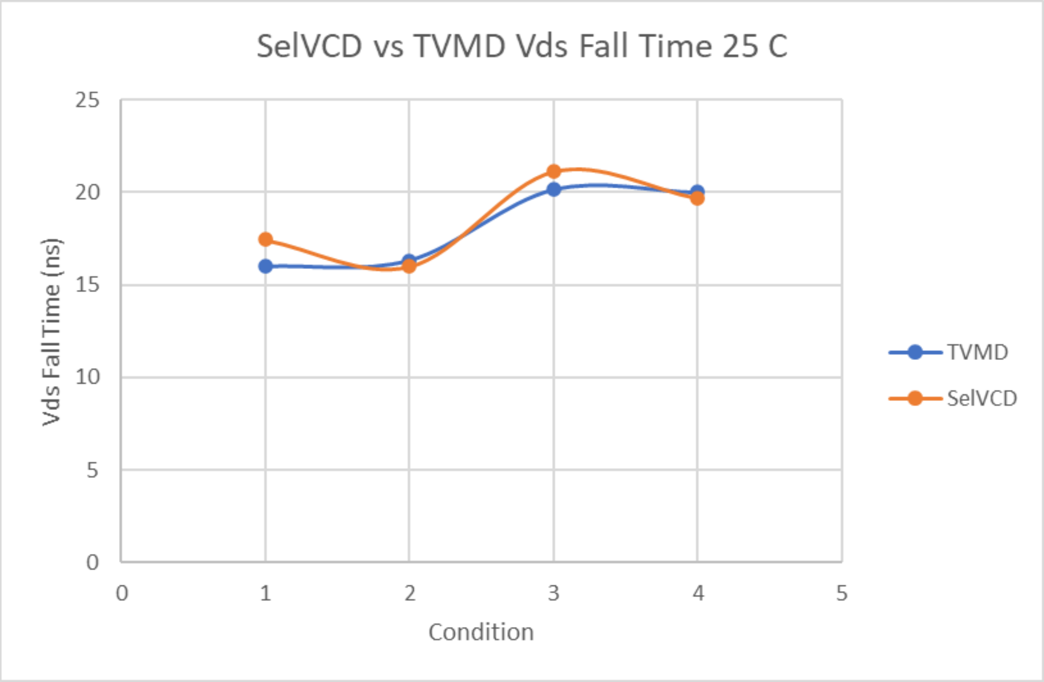


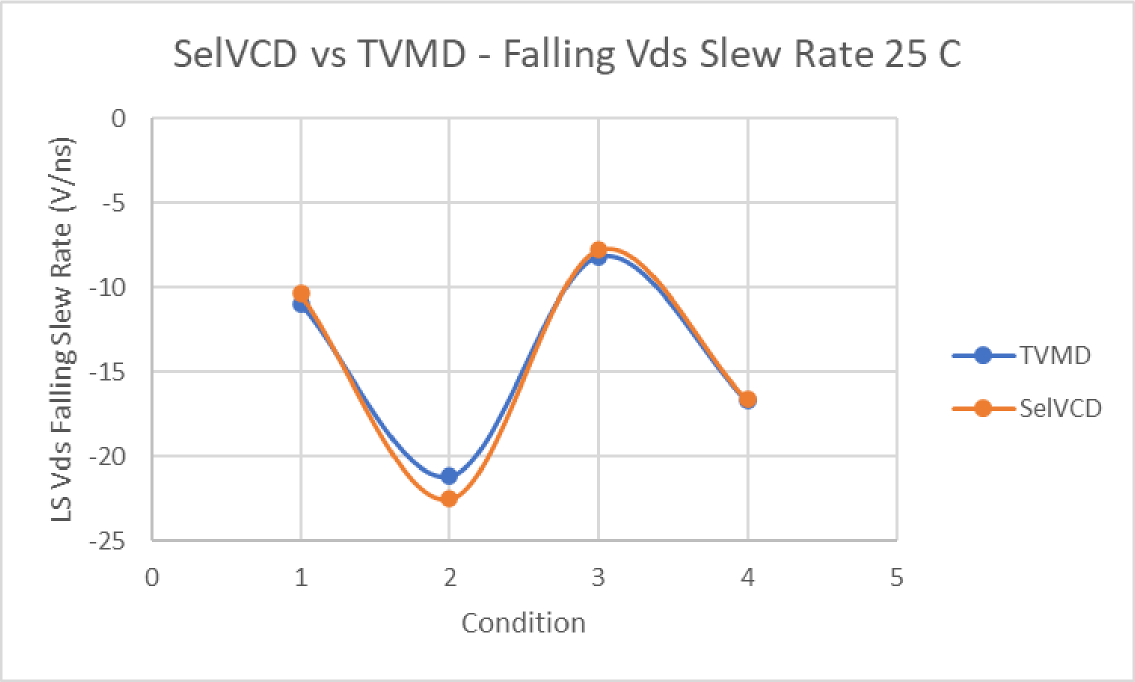
Si82F39AEE-IS3



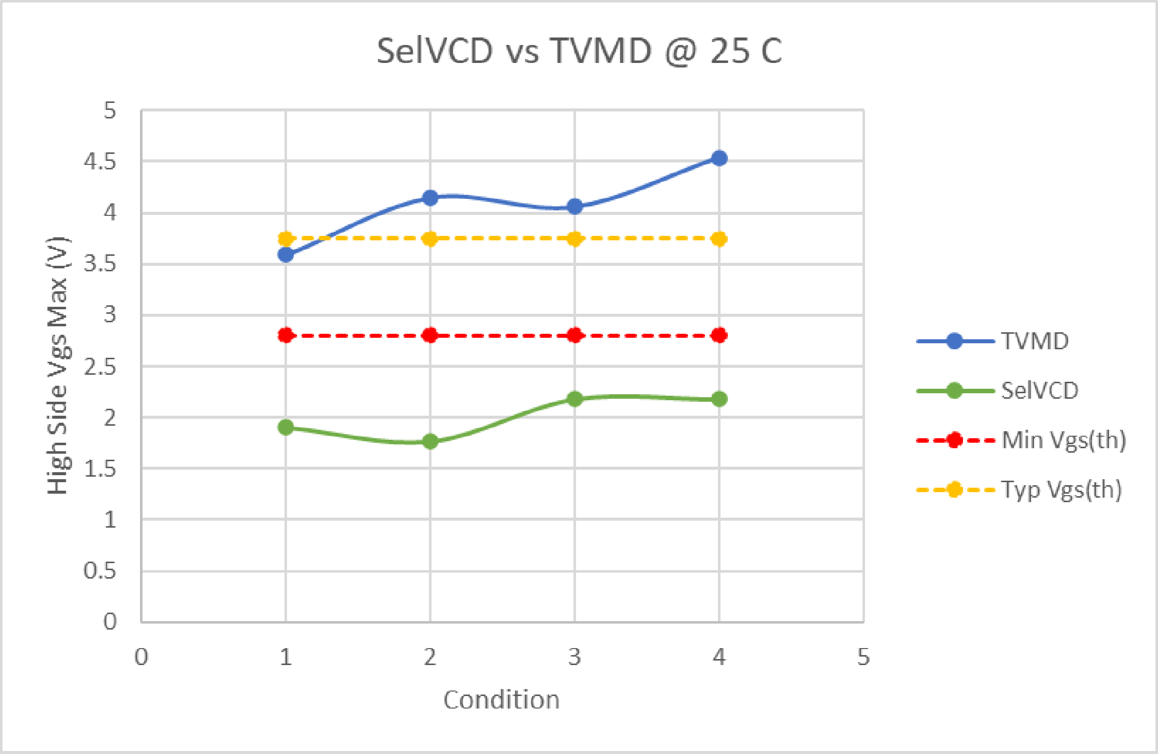
TVMD vs SelVCD Customer Comparison

- Condition 1 = 227 V 25 A
- Condition 2 = 455 V 25 A
- Condition 3 = 227 V 45 A
- Condition 4 = 455 V 45 A





High Side V_{GS} Max



- Condition 1 = 227 V 25 A
- Condition 2 = 455 V 25 A
- Condition 3 = 227 V 45 A
- Condition 4 = 455 V 45 A
- Current R_G selections result in max HS V_{GS} significantly above min $V_{GS(th)}$
- SelVCD stays well below $V_{GS(th)}$

Conclusions

- SelVCD™ minimizes the risk of parasitic turn-on
- Allows removal of negative gate-drive bias, providing additional safety margin
  - Lowers BOM cost
  - Frees up valuable board space
  - Improves overall system efficiency
- Traditional voltage-mode drivers may require a Miller clamp, adding pins and increasing BOM/cost
  - SelVCD achieves this with no extra pins or added components

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Matthew Segada – Skyworks Solutions
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Appendix – Derivation

- Capacitive voltage divider equation: $\frac{V_{out}}{V_{in}} = \frac{C_1}{C_1+C_2}$
  - In the case of the Miller effect, $C_1 = C_{GD}$ and $C_2 = C_{GS}$
  - $\frac{V_{\mathrm{GS}}}{V_{\mathrm{DS}}} = \frac{\mathrm{C}_{\mathrm{GD}}}{C_{\mathrm{GS}}+C_{\mathrm{GD}}}$, however $C_{GD} << C_{GS}$ so the following simplification can be made: $\frac{V_{\mathrm{GS}}}{V_{\mathrm{DS}}} = \frac{\mathrm{C}_{\mathrm{GD}}}{C_{\mathrm{GS}}}$
  - The main contribution to PTO, is the mostly constant slope from V_{DS}. Only need to consider the slew rate of the rising and falling edges: $\frac{\mathrm{d}V_{\mathrm{GS}}}{\mathrm{d}V_{\mathrm{DS}}} = \frac{\mathrm{C}_{\mathrm{GD}}}{C_{\mathrm{GS}}} \Rightarrow \mathrm{dV}_{\mathrm{GS}} \approx \frac{\mathrm{C}_{\mathrm{GD}}}{C_{\mathrm{GS}}}\mathrm{dV}_{\mathrm{DS}}$